

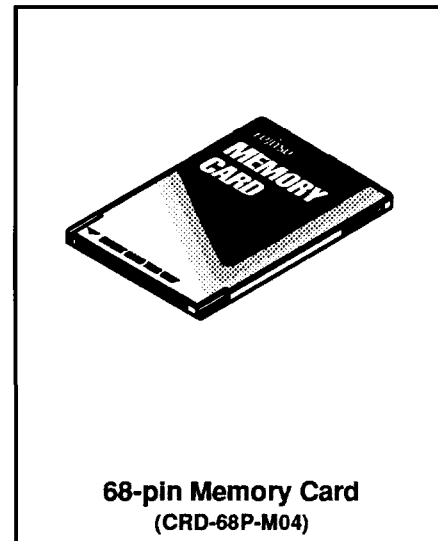
# MB98A9061x, MB9071x, MB9081x, and 9091x-20 Low Power SRAM Memory Card 64K, 128K, 256K, and 512k-Byte

The Fujitsu MB98A9061x, MB98A9071x, MB98A9081x and MB98A9091x are Static Random Access Memory (SRAM) cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuitry is protected by two metal panels, one at the top and the bottom of the card, to reduce chip damage from electrostatic discharge.

When the SRAM card is not powered by its system, an on-board, replaceable lithium battery (coin-type) is used to retain data. When the lithium battery must be replaced, two rechargeable batteries that are built into the SRAM card, maintain data. (See the BLOCK DIAGRAM for location of batteries.)

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. This new series (MB98A9061x-20 etc.) of SRAM cards consume less power than the MB98A9060x-20 series, thus extending system battery life and performance.

In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specification, SRAM cards offer additional EEPROM memory for storing attribute data. The attribute memory is an SRAM memory card option. (See page 2 for a description of the three available options.)



- PCMCIA and JEIDA industry standard for 68-pin memory card
- Credit card size: 85.6 mm (length) x 54.0 mm (width) x 3.3 mm (thick).
- PCMCIA/JEIDA industry standard, two-piece 68-pin connector (with a two-row built-in 68-pin receptacle)
- Low operating and standby power consumption
- Replaceable lithium battery
- Built-in, rechargeable batteries for data retention during lithium battery replacement
- Battery voltage detect and write protect function

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	-0.5 to +6.0	V
Input Voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
Output Voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Temperature Under Bias	$T_{BIAS}$	-10 to +60 <sup>1</sup>	°C
Storage Temperature	$T_{STG}$	-20 to +65 <sup>2</sup>	°C

Notes: <sup>1</sup> This value does not apply to the replaceable battery.  
<sup>2</sup> This value does not apply to the replaceable battery and data retention.

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

**MB98A9061x-20**  
**MB98A9071x-20**  
**MB98A9081x-20**  
**MB98A9091x-20**

## ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the  $\overline{\text{REG}}$  pin on the card interface. Option descriptions as follows:

### Option 1: Attribute memory is not supported. $\overline{\text{REG}}$ Pin : Not Connected

Part Number	Main Memory		Attribute Memory		Memory Organization*
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90611	MB84256A x 2 pcs.	200 ns	N/A	N/A	64K x 8 bits/32K x 16 bits
MB98A90711	MB84256A x 4 pcs.	200 ns	N/A	N/A	128K x 8 bits/64K x 16 bits
MB98A90811	MB84256A x 8 pcs.	200 ns	N/A	N/A	256K x 8 bits/128K x 16 bits
MB98A90911	MB84256A x 16 pcs.	200 ns	N/A	N/A	512K x 8 bits/256K x 16 bits

### Option 2: Attribute memory in a separate location is not supported

When the  $\overline{\text{REG}}$  line is asserted, "FF" is output to the data bus to indicate that attribute memory may be stored in the main memory.

Part Number	Main Memory		Attribute Memory		Memory Organization*
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90612	MB84256A x 2 pcs.	200 ns	N/A	N/A	64K x 8 bits/32K x 16 bits
MB98A90712	MB84256A x 4 pcs.	200 ns	N/A	N/A	128K x 8 bits/64K x 16 bits
MB98A90812	MB84256A x 8 pcs.	200 ns	N/A	N/A	256K x 8 bits/128K x 16 bits
MB98A90912	MB84256A x 16 pcs.	200 ns	N/A	N/A	512K x 8 bits/256K x 16 bits

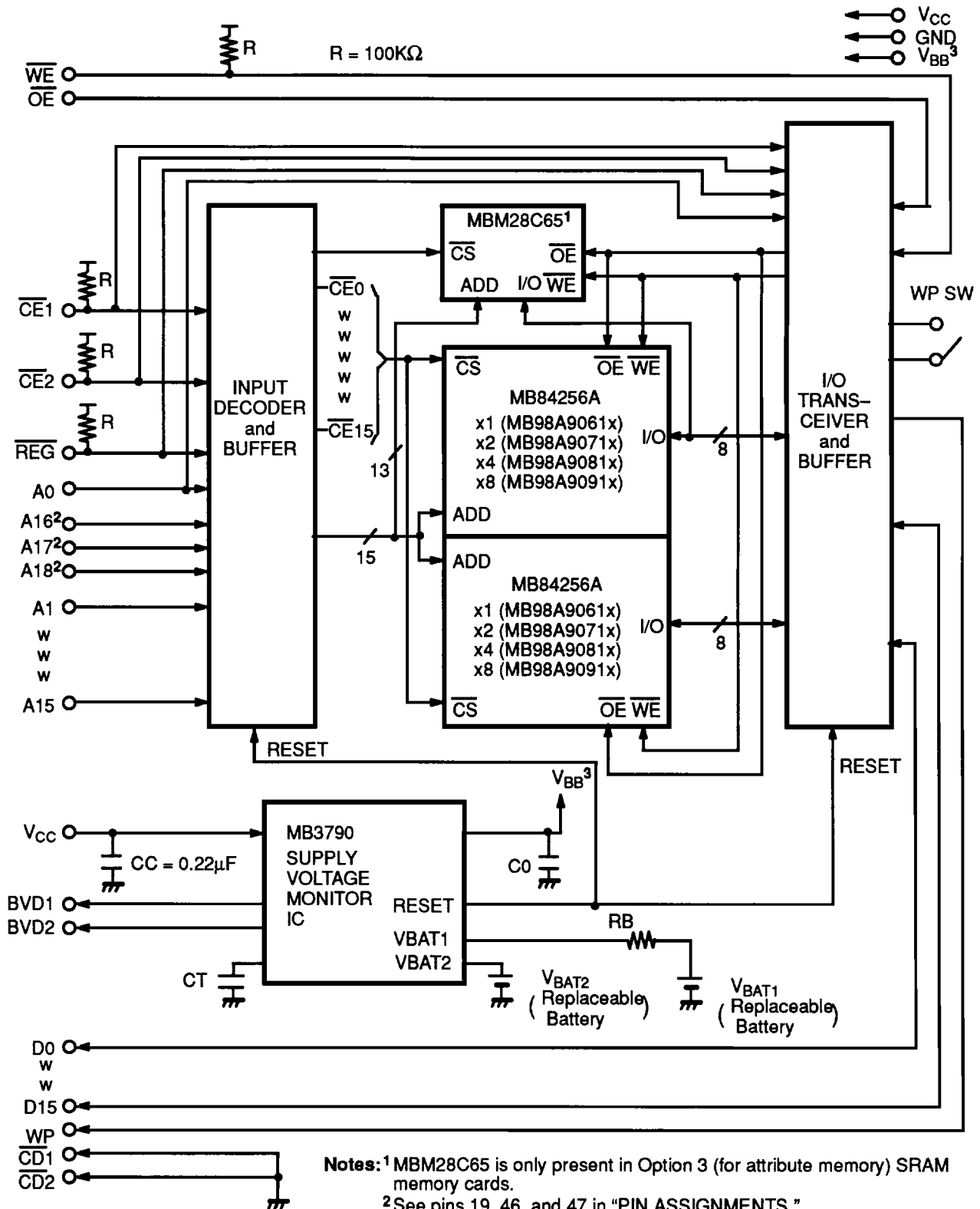
### Option 3: Attribute memory is supported. The data is stored in an 8K-bit EEPROM.

When the  $\overline{\text{REG}}$  line is asserted, data stored in EEPROM is output to the data bus.

Part Number	Main Memory		Attribute Memory		Memory Organization*
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90613	MB84256A x 2 pcs.	200 ns	MBM28C65 x 1 pc.	300 ns	64K x 8 bits/32K x 16 bits
MB98A90713	MB84256A x 4 pcs.	200 ns	MBM28C65 x 1 pc.	300 ns	128K x 8 bits/64K x 16 bits
MB98A90813	MB84256A x 8 pcs.	200 ns	MBM28C65 x 1 pc.	300 ns	256K x 8 bits/128K x 16 bits
MB98A90913	MB84256A x 16 pcs.	200 ns	MBM28C65 x 1 pc.	300 ns	512K x 8 bits/256K x 16 bits

Note: \*To be configured by user.

Figure 1. MB98A9061x, MB98A9071x, MB98A9081x, and MB98A9091x BLOCK DIAGRAM



**MB98A9061x-20**  
**MB98A9071x-20**  
**MB98A9081x-20**  
**MB98A9091x-20**

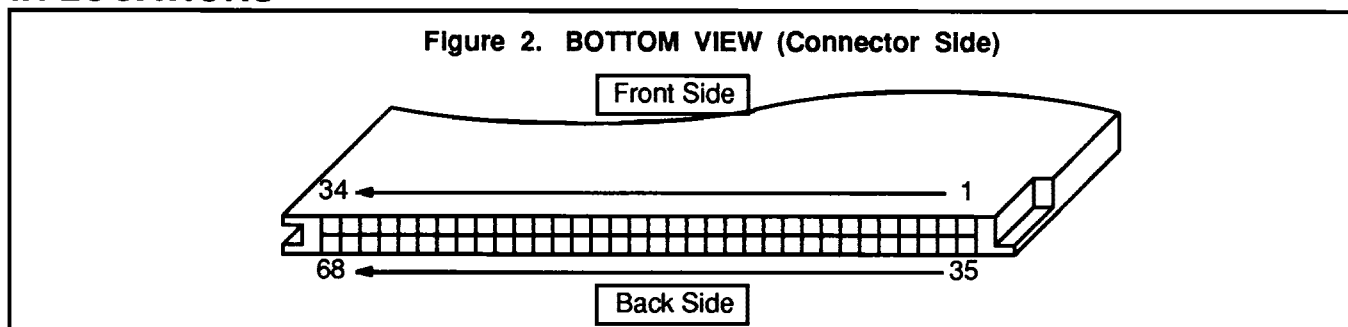
## PIN ASSIGNMENTS

MB98A9061x	MB98A9061x	MB98A9061x	Pin No.		MB98A9061x	MB98A9061x	MB98A9061x
GND	GND	GND	1	35	GND	GND	GND
D3	D3	D3	2	36	CD1	CD1	CD1
D4	D4	D4	3	37	D11	D11	D11
D5	D5	D5	4	38	D12	D12	D12
D6	D6	D6	5	39	D12	D12	D12
D7	D7	D7	6	40	D14	D14	D14
CE1	CE1	CE1	7	41	D15	D15	D15
A10	A10	A10	8	42	CE	CE	CE
OE	OE	OE	9	43	NC	NC	NC
A11	A11	A11	10	44	NC	NC	NC
A9	A9	A9	11	45	NC	NC	NC
A8	A8	A8	12	46	NC	NC	NC
A13	A13	A13	13	47	NC	NC	NC
A14	A14	A14	14	48	NC	NC	NC
WE	WE	WE	15	49	NC	NC	NC
NC	NC	NC	16	50	NC	NC	NC
V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	17	51	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
NC	NC	NC	18	52	NC	NC	NC
NC	NC	NC	19	53	NC	NC	NC
A15	A15	A15	20	54	NC	NC	NC
A12	A12	A12	21	55	NC	NC	NC
A7	A7	A7	22	56	NC	NC	NC
A6	A6	A6	23	57	NC	NC	NC
A5	A5	A5	24	58	NC	NC	NC
A4	A4	A4	25	59	NC	NC	NC
A3	A3	A3	26	60	NC	NC	NC
A2	A2	A2	27	61	REG	REG	REG
A1	A1	A1	28	62	BVD2	BVD2	BVD2
A0	A0	A0	29	63	BVD1	BVD1	BVD1
D0	D0	D0	30	64	D8	D8	D8
D1	D1	D1	31	65	D9	D9	D9
D2	D2	D2	32	66	D10	D10	D10
WP	WP	WP	33	67	CD2	CD2	CD2
GND	GND	GND	34	68	GND	GND	GND

## PIN DESCRIPTIONS

Symbol	Pin Name	Input/Output	Function
A0 to A18	Address Input	Input	Address Inputs, A0–A18.
D0 to D15	Data Input/Output	Input/Output	Data Inputs/Outputs. The data bus size (8-bit or 16-bit) selected with CE1 and CE2.
CE1	Card Enable for Lower Byte	Input	Active Low. –Lower byte (D0–D7) is selected for read/write function of SRAM cards.
CE2	Card Enable for Upper Byte	Input	Active Low. –Upper byte (D8–D15) is selected for read/write function of SRAM cards.
REG	Attribute Memory Select	Input	Active Low. –Attribute memory is selected for read/write function of identification data of SRAM cards. (NC or "FF" data or attribute data.
OE	Output Enable	Input	Active Low. –Output enable for SRAM cards.
WE	Write Enable	Input	Active Low. –Write enable for SRAM cards.
CD1, CD2	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	Write controller for SRAM cards. This pin outputs the On/Off status of "WP Switch".
BVD1	Battery Voltage Detect 1	Output	These pins indicate the battery condition of the SRAM cards. a) BVD1 = BVD2 = $V_{OH}$ –Battery voltage is a safe level. b) BVD2 = $V_{OL}$ , BVD1 = $V_{OH}$ –Battery voltage is lower than 2.65V. Battery should be replaced c) BVD1 = BVD2 = $V_{OL}$ –Battery voltage is lower than 2.37V.
BVD2	Battery Voltage Detect 2	Output	
VCC	Power Supply	–	Power Supply Voltage. (+5.0V $\pm$ 5%)
GND	Ground	–	System Ground
NC	Not Connected	–	

## PIN LOCATIONS



MB98A9061x-20  
 MB98A9071x-20  
 MB98A9081x-20  
 MB98A9091x-20

## FUNCTION TRUTH TABLE

### MAIN MEMORY FUNCTION<sup>1</sup> (REG = V<sub>IH</sub>)

$\overline{CE2}$	$\overline{CE1}$	A0 (Byte)	$\overline{OE}$	$\overline{WE}$	WP	Mode	Data Input/Output		WP SW.
							D15-D8	D7-D0	
H	H	X	X	X	L	Standby	High-Z		NP
H	L	L	L	H	L	Read (x8)	High-Z	D <sub>OUT</sub> (Lower Byte)	NP
H	L	H	L	H	L	Read (x8)	High-Z	D <sub>OUT</sub> (Upper Byte)	NP
H	L	L	H <sup>2</sup>	L	L	Write (x8)	High-Z	D <sub>IN</sub> (Lower Byte)	NP
H	L	H	H <sup>2</sup>	L	L	Write (x8)	High-Z	D <sub>IN</sub> (Upper Byte)	NP
L	H	X	L	H	L	Read (x8)	D <sub>OUT</sub> (Upper Byte)	High-Z	NP
L	H	X	H <sup>2</sup>	L	L	Write (x8)	D <sub>IN</sub> (Upper Byte)	High-Z	NP
L	L	X	L	H	L	Read (x16)	D <sub>OUT</sub>		NP
L	L	X	H	L	L	Write (x16)	D <sub>IN</sub>		NP
X	X	X	H	H	L	Output Disable	High-Z		NP

H	H	X	X	X	H	Standby	High-Z		P
H	L	L	L	H	H	Read (x8)	High-Z	D <sub>OUT</sub> (Lower Byte)	P
H	L	H	L	H	H	Read (x8)	High-Z	D <sub>OUT</sub> (Upper Byte)	P
H	L	L	H <sup>2</sup>	L	H	Output Disable	High-Z		P
H	L	H	H <sup>2</sup>	L	H	Output Disable	High-Z		P
L	H	X	L	H	H	Read (x8)	D <sub>OUT</sub> (Upper Byte)	High-Z	P
L	H	X	H <sup>2</sup>	L	H	Output Disable	High-Z		P
L	L	X	L	H	H	Read (x16)	D <sub>OUT</sub>		P
L	L	X	H	L	H	Output Disable	High-Z		P
X	X	X	H	H	H	Output Disable	High-Z		P

**Notes:**<sup>1</sup> H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Either V<sub>IL</sub> or V<sub>IH</sub>, WP SW = Write Protect Switch, NP = Non-protect, P = Protect  
<sup>2</sup>H-level is recommended though it is functionable at L-level.

**FUNCTION TRUTH TABLE** (Continued)

**ATTRIBUTE MEMORY FUNCTION<sup>1</sup> (REG = V<sub>IL</sub>)<sup>2</sup>**

$\overline{\text{CE}}2$	$\overline{\text{CE}}1$	A0 (Byte)	$\overline{\text{OE}}$	$\overline{\text{WE}}$	WP	Mode	Data Input/Output		WP SW
							D15–D8	D7–D0	
H	H	X	X	X	L	Standby	High-Z		NP
H	L	L	L	H	L	Read (x8)	High-Z	D <sub>OUT</sub> <sup>3</sup> (Lower Byte)	NP
H	L	H	L	H	L	Read (x8)	High-Z	H	NP
H	L	L	H	L	L	Write (x8)	High-Z	D <sub>IN</sub> (Lower Byte)	NP
H	L	H	H	L	L	Write (x8)	High-Z	X	NP
L	H	X	L	H	L	Read (x8)	H	High-Z	NP
L	H	X	H	L	L	Write (x8)	High-Z	High-Z	NP
L	L	X	L	H	L	Read (x16)	H	D <sub>OUT</sub> <sup>3</sup> (Lower Byte)	NP
L	L	X	H	L	L	Write (x16)	X	D <sub>IN</sub> (Lower Byte)	NP
X	X	X	H	H	L	Output Disable	High-Z		NP

H	H	X	X	X	H	Standby	High-Z		P
H	L	L	L	H	H	Read (x8)	High-Z	D <sub>OUT</sub> <sup>3</sup> (Lower Byte)	P
H	L	H	L	H	H	Read (x8)	High-Z	H	P
H	L	L	H	L	H	Output Disable	High-Z		P
H	L	H	H	L	H	Output Disable	High-Z		P
L	H	X	L	H	H	Read (x8)	H	High-Z	P
L	H	X	H	L	H	Output Disable	High-Z		P
L	L	X	L	H	H	Read (x16)		D <sub>OUT</sub> <sup>3</sup> (Lower Byte)	P
L	L	X	H	L	H	Output Disable	High-Z		P
X	X	X	H	H	H	Output Disable	High-Z		P

**Notes:**<sup>1</sup> H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Either V<sub>IL</sub> or V<sub>IH</sub>, WP SW = Write Protect Switch, NP = Non-protect, P = Protect

<sup>2</sup>NC for MB98A90611, MB98A90711, MB98A90811, and MB98A90911.

<sup>3</sup>H-level is output for MB98A90612, MB98A90712, MB98A90812, and MB98A90912.

**MB98A9061x-20**  
**MB98A9071x-20**  
**MB98A9081x-20**  
**MB98A9091x-20**

## ADDRESS CONFIGURATIONS<sup>1</sup> (MAIN MEMORY)

8-BIT BUS ORGANIZATION ( $\overline{CE1} = V_{IL}, \overline{CE2} = V_{IH}$ )

A18 to A0	$\overline{CE2}$	$\overline{CE1}$	D15-D8	D7-D0
000 0000 0000 0000 0000	H	L	-----	0 Add.
000 0000 0000 0000 0001	H	L	-----	1 Add.
000 0000 0000 0000 0010	H	L	-----	2 Add.
000 0000 0000 0000 0011	H	L	-----	3 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 1100	H	L	-----	524284 Add.
111 1111 1111 1111 1101	H	L	-----	524285 Add.
111 1111 1111 1111 1110	H	L	-----	524286 Add.
111 1111 1111 1111 1111	H	L	-----	524287 Add.

8-BIT BUS ORGANIZATION ( $\overline{CE1} = V_{IH}, \overline{CE2} = V_{IL}$ )<sup>2</sup>

A18 to A0	$\overline{CE2}$	$\overline{CE1}$	D15-D8	D7-D0
000 0000 0000 0000 000X	L	H	1 Add.	-----
000 0000 0000 0000 001X	L	H	3 Add.	-----
000 0000 0000 0000 010X	L	H	5 Add.	-----
000 0000 0000 0000 011X	L	H	7 Add.	-----
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 100X	L	H	524281 Add.	-----
111 1111 1111 1111 101X	L	H	524283 Add.	-----
111 1111 1111 1111 110X	L	H	524285 Add.	-----
111 1111 1111 1111 111X	L	H	524287 Add.	-----

16-BIT BUS ORGANIZATION ( $\overline{CE1} = V_{IL}, \overline{CE2} = V_{IL}$ )

A18 to A0	$\overline{CE2}$	$\overline{CE1}$	D15-D8	D7-D0
000 0000 0000 0000 000X	L	L	1 Add.	0 Add.
000 0000 0000 0000 001X	L	L	3 Add.	2 Add.
000 0000 0000 0000 010X	L	L	5 Add.	4 Add.
000 0000 0000 0000 011X	L	L	7 Add.	6 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 100X	L	L	524281 Add.	524280 Add.
111 1111 1111 1111 101X	L	L	524283 Add.	524282 Add.
111 1111 1111 1111 110X	L	L	524285 Add.	524284 Add.
111 1111 1111 1111 111X	L	L	524287 Add.	524286 Add.

Notes:<sup>1</sup>H =  $V_{IH}$ , L =  $V_{IL}$ , X = Either 0 or 1.

<sup>2</sup>Even addresses are not available in this mode.

## RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.75	5.0	5.25	V
Ground	GND		0		V
Input High Voltage	$V_{IH}$	2.4		$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3		0.8	V
Ambient Temperature*	$T_A$	0		55	°C

Note: \*This value does not apply to the replaceable lithium battery. See  $V_{BAT1}$  in Figure 1.

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Standby Supply Current <sup>1</sup>	$\overline{CE1}, \overline{CE2} \geq V_{CC} - 0.2V$	$I_{SB1}$			0.5	mA
	$\overline{CE1}, \overline{CE2} = V_{IH}$	$I_{SB2}$			5.0	mA
Active Supply Current	$V_{IN} = V_{IH}$ or $V_{IL}$ $\overline{CE1}, \overline{CE2} = V_{IL}, I_{OUT} = 0$ mA	$I_{CC1}$			110	mA
Operating Supply Current	$V_{IN} = V_{IH}$ or $V_{IL}$ , Cycle = Min. Duty = 100%, $I_{OUT} = 0$ mA $\overline{OE} = V_{IH}$ during Write Cycle	$I_{CC2}$			190	mA
Input Leakage Current <sup>2</sup>	$V_{IN} = 0$ V to $V_{CC}$	$I_{LI}$	-10		10	μA
Output Leakage Current <sup>3</sup>	$V_{OUT} = 0$ V to $V_{CC}$ , $\overline{CE1}, \overline{CE2} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	$I_{LVO}$	-10		10	μA
Output High Voltage <sup>4</sup>	$I_{OH} = -1.0$ mA	$V_{OH}$	2.4			V
Output Low Voltage	$I_{OL} = 2.1$ mA	$V_{OL}$			0.4	V

Notes: <sup>1</sup>This value does not apply to recharge current from system or replaceable lithium battery to rechargeable battery.

<sup>2</sup>This value does not apply to  $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{REG}$  and  $\overline{WE}$ .

<sup>3</sup>This value does not apply to  $\overline{BVD1}$ ,  $\overline{BVD2}$ ,  $\overline{CD1}$ ,  $\overline{CD2}$  and  $\overline{WP}$ .

<sup>4</sup>This value does not apply to  $\overline{BVD1}$ ,  $\overline{BVD2}$ ,  $\overline{CD1}$ , and  $\overline{CD2}$ .

## CAPACITANCE ( $T_A = 25^\circ\text{C}$ , $f = 1$ MHz, $V_{IN} = V_{I/O} = \text{GND}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance <sup>1</sup>	$C_{IN}$			50	pF
I/O Capacitance <sup>2</sup>	$C_{OUT}$			50	pF

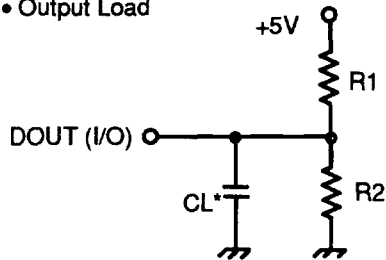
Notes: <sup>1</sup>This value does not apply to  $\overline{CE1}$ ,  $\overline{CE2}$ ,  $\overline{REG}$  and  $\overline{WE}$ .

<sup>2</sup>This value does not apply to  $\overline{BVD1}$ ,  $\overline{BVD2}$ ,  $\overline{CD1}$ , and  $\overline{CD2}$ .

MB98A9061x-20  
 MB98A9071x-20  
 MB98A9081x-20  
 MB98A9091x-20

Figure 3. AC TEST CONDITIONS

• Output Load



• Input Pulse Levels: 0.6V to 2.6V

• Input Pulse Rise and Fall Times: 5ns (transition between 0.8V and 2.4V)

• Timing Reference Levels

Input:  $V_{IL} = 0.8V$ ,  $V_{IH} = 2.4V$   
 Output:  $V_{OL} = 0.8V$ ,  $V_{OH} = 2.0V$

\* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load I	1.8k $\Omega$	990 $\Omega$	100pF	All parameters except $t_{CLZ}$ , $t_{OLZ}$ , $t_{CHZ}$ , $t_{OHZ}$ , $t_{RCLZ}$ , $t_{ROLZ}$ , $t_{RCHZ}$ , $t_{ROHZ}$ , $t_{WLZ}$ and $t_{WHZ}$
Load II	1.8k $\Omega$	990 $\Omega$	5pF	$t_{CLZ}$ , $t_{OLZ}$ , $t_{CHZ}$ , $t_{OHZ}$ , $t_{RCLZ}$ , $t_{RCHZ}$ , $t_{ROHZ}$ , $t_{WLZ}$ , and $t_{WHZ}$

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY READ CYCLE

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	$t_{RC}$	200		ns
Address Access Time	$t_{AA}$		200	ns
Card Enable Access Time	$t_{CE}$		200	ns
Output Enable Access Time	$t_{OE}$		100	ns
Output Hold from Address Change	$t_{OH}$	5		ns
Card Enable to Output Low-Z <sup>1, 2</sup>	$t_{CLZ}$	5		ns
Output Enable to Output Low-Z <sup>1, 2</sup>	$t_{OLZ}$	5		ns
Card Enable to Output High-Z <sup>1, 2</sup>	$t_{CHZ}$		50	ns
Output Enable to Output High-Z <sup>1, 2</sup>	$t_{OHZ}$		50	ns

### ATTRIBUTE MEMORY READ CYCLE<sup>3</sup>

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	$t_{RRC}$	300		ns
Address Access Time	$t_{RAA}$		300	ns
Card Enable Access Time	$t_{RCE}$		300	ns
Output Enable Access Time	$t_{ROE}$		150	ns
Output Hold from Address Change	$t_{ROH}$	5		ns
Card Enable to Output Low-Z <sup>1, 2</sup>	$t_{RCLZ}$	5		ns
Output Enable to Output Low-Z <sup>1, 2</sup>	$t_{ROLZ}$	5		ns
Card Enable to Output High-Z <sup>1, 2</sup>	$t_{RCHZ}$		60	ns
Output Enable to Output High-Z <sup>1, 2</sup>	$t_{ROHZ}$		60	ns

Notes:<sup>1</sup> Transition is measured at the point of  $\pm 500$  mV from steady state voltage.

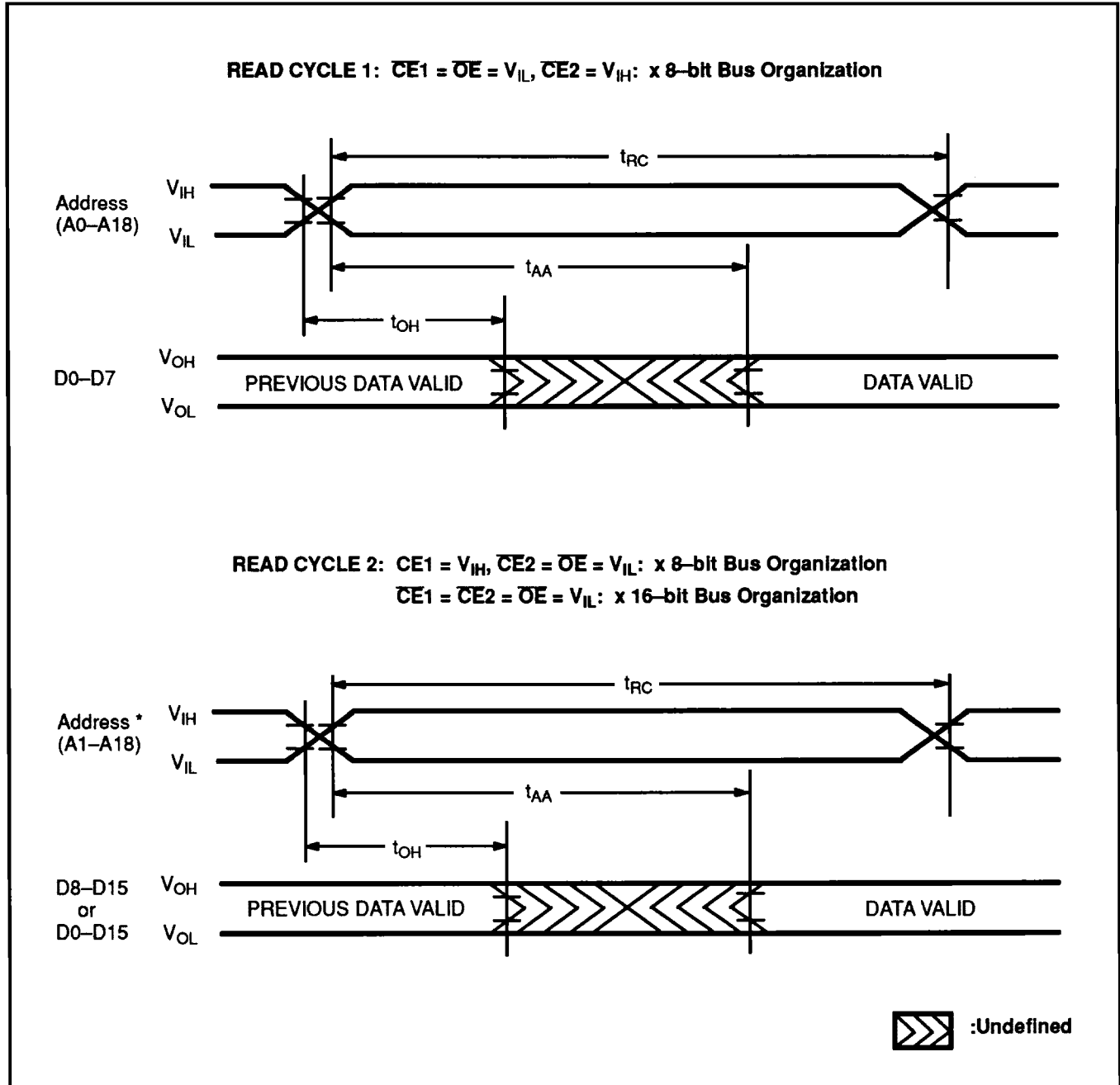
<sup>2</sup> This parameter is specified using Load II in Figure 2.

<sup>3</sup> This parameter is for MB98A90613, MB98A90713, MB98A90813, and MB98A90913.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM (WE = V<sub>IH</sub>, REG = V<sub>IH</sub>)



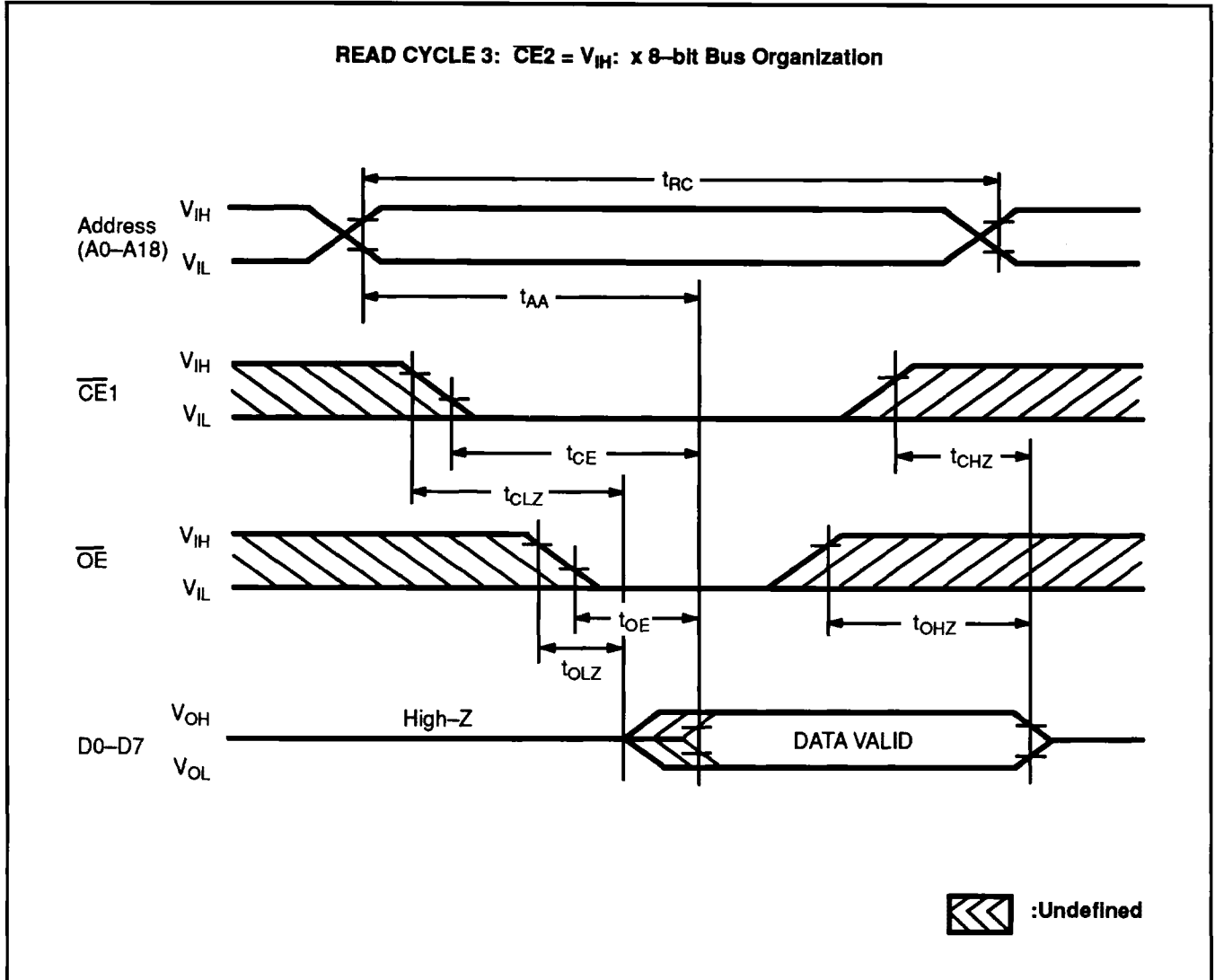
**Note:** \*A0 = Either V<sub>IH</sub> or V<sub>IL</sub>.

**MB98A9061x-20**  
**MB98A9071x-20**  
**MB98A9081x-20**  
**MB98A9091x-20**

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

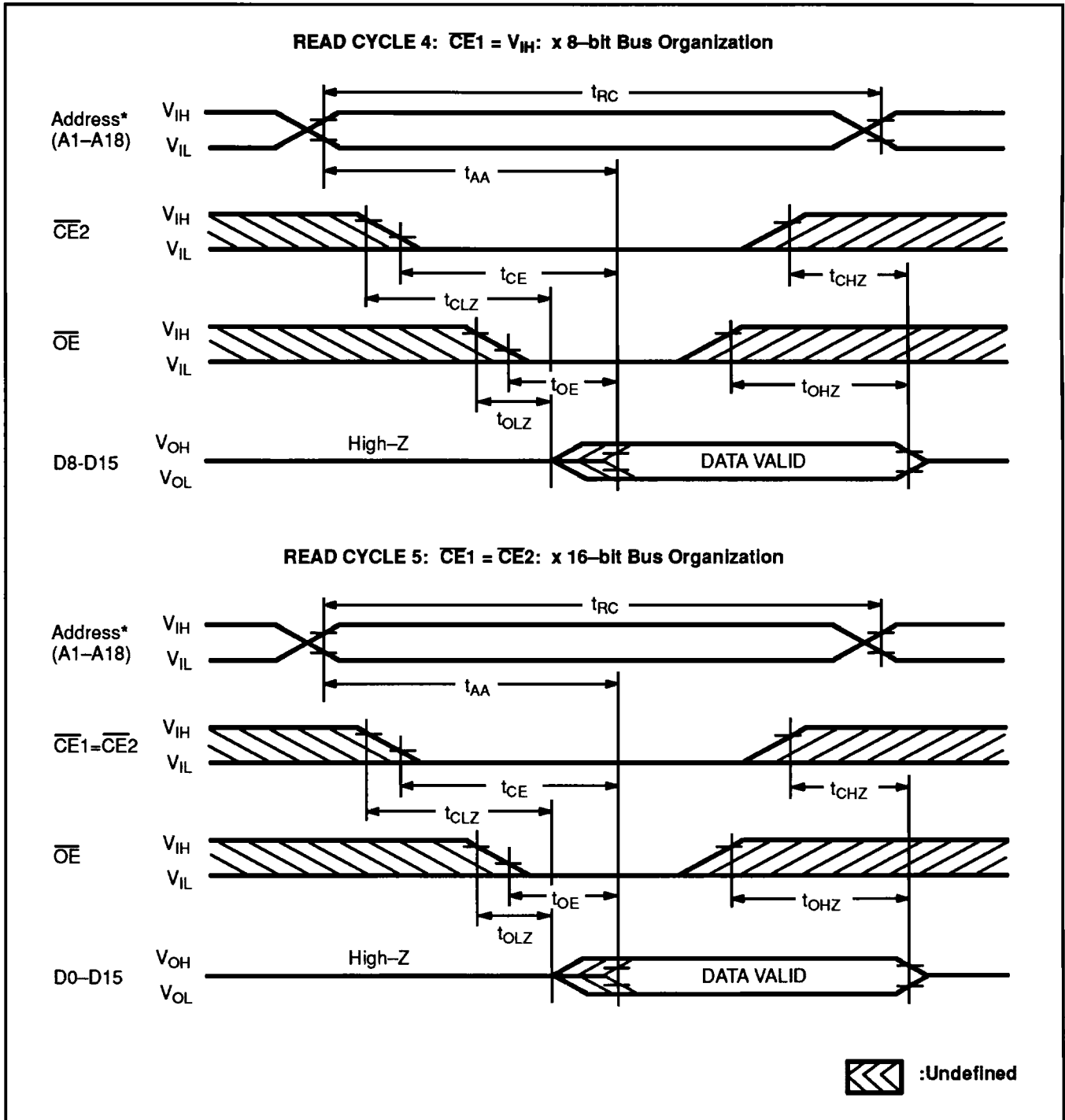
MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ ,  $\overline{REG} = V_{IH}$ )



## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ , $\overline{REG} = V_{IH}$ )

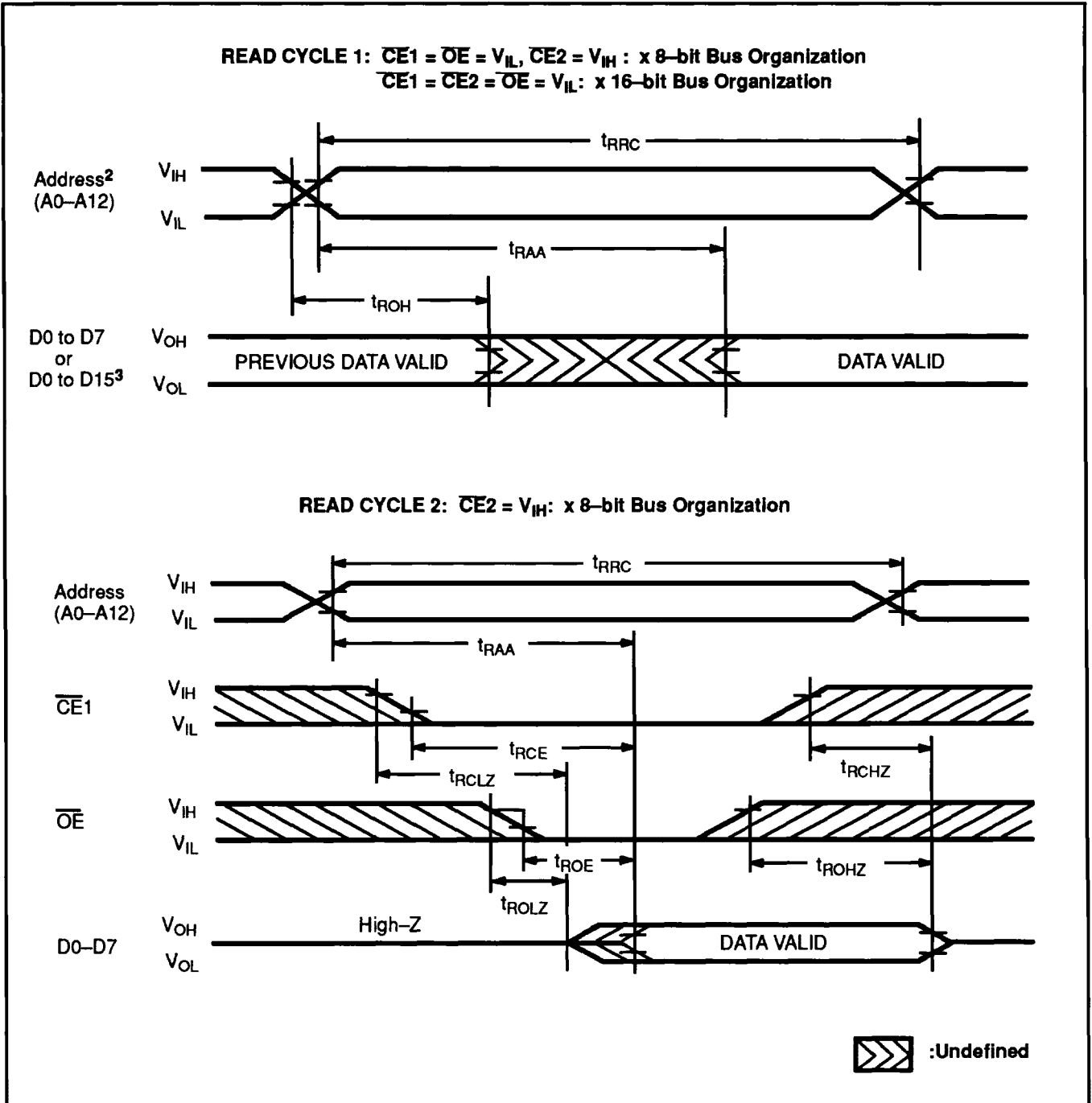


Note: \*A0 = Either  $V_{IH}$  or  $V_{IL}$ .

MB98A9061x-20  
 MB98A9071x-20  
 MB98A9081x-20  
 MB98A9091x-20

**AC CHARACTERISTICS** (Continued)  
 (Recommended operating conditions unless otherwise noted.)

**ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM** ( $\overline{WE} = V_{IH}$ ,  $\overline{REG} = V_{IL}$ )<sup>1</sup>



**Notes:**<sup>1</sup> This timing diagram is for MB98A90613, MB98A90713, MB98A90813, and MB98A90913. "FF" data is available on MB98A90612, MB98A90712, MB98A90812, and MB98A90912 only.

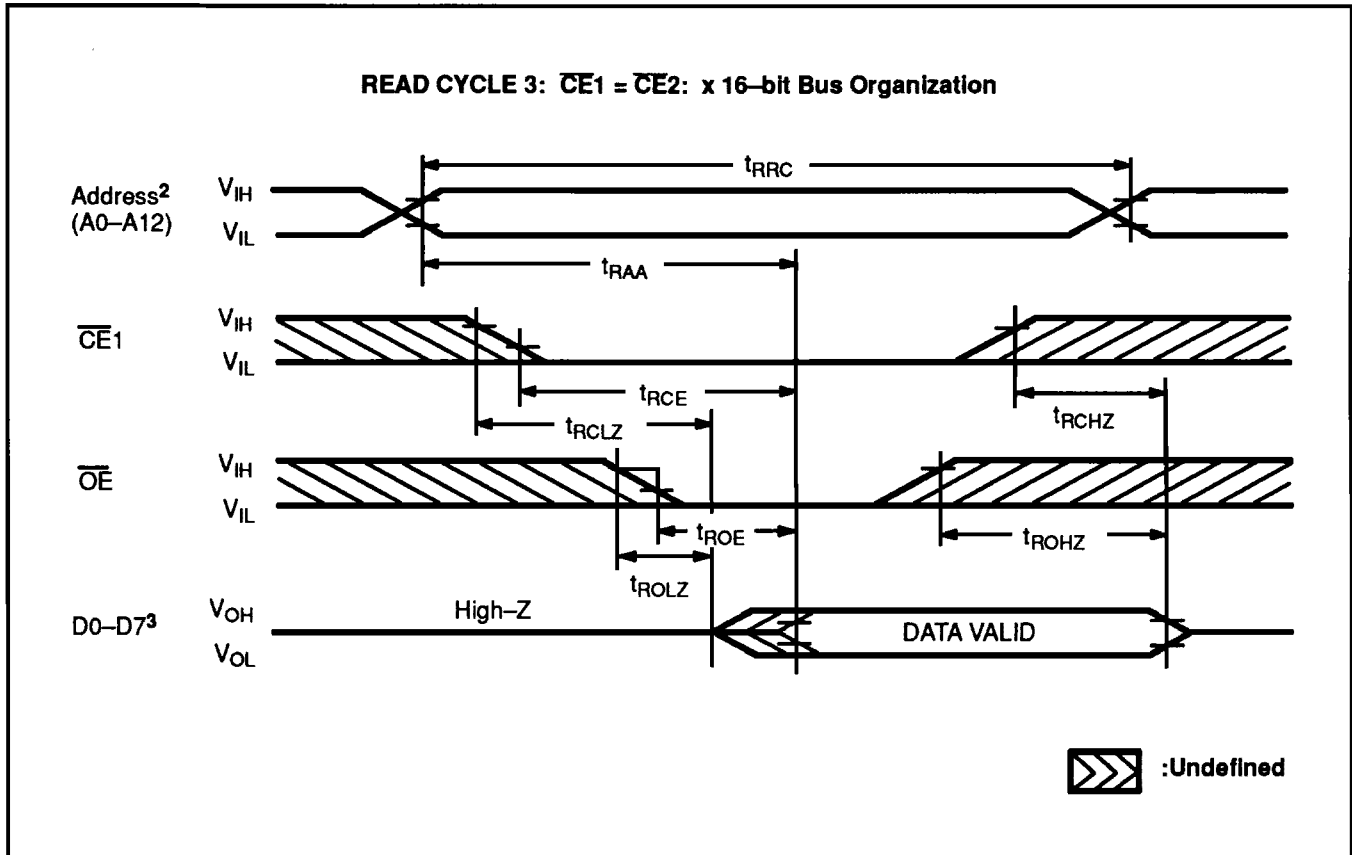
<sup>2</sup> A0 = Either  $V_{IH}$  or  $V_{IL}$  for a 16-bit bus organization.

<sup>3</sup> H-level is output from D8 to D15.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ , $\overline{REG} = V_{IL}$ )<sup>1</sup>



**Notes:**<sup>1</sup> This timing diagram is for MB98A90603, MB98A90713, MB98A90813, and MB98A90913. "FF" data is available on MB98A90612, MB98A90712, MB98A90812, and MB98A90912 only.

<sup>2</sup> A0 = Either  $V_{IH}$  or  $V_{IL}$ .

<sup>3</sup> H-level is output from D8 to D15.

MB98A9061x-20  
 MB98A9071x-20  
 MB98A9081x-20  
 MB98A9091x-20

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY WRITE CYCLE<sup>1</sup>

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	$t_{WC}$	200		ns
Address Valid to End of Write	$t_{AW}$	140		ns
Chip Select to End of Write	$t_{CW}$	140		ns
Data Valid to End of Write	$t_{DW}$	60		ns
Data H <sub>OL</sub> d Time	$t_{DH}$	30		ns
Write Pulse Width	$t_{WP}$	120		ns
Address Setup Time	$t_{AS}$	20		ns
Write Recovery Time	$t_{WR}$	30		ns
Output Enable to Output Low-Z <sup>2</sup>	$t_{OLZ}$	5		ns
Output Enable to Output High-Z <sup>2</sup>	$t_{OHZ}$		50	ns
Write Enable to Output Low-Z <sup>2,3</sup>	$t_{WLZ}$	5		ns
Write Enable to Output High-Z <sup>2,3</sup>	$t_{WHZ}$		50	ns
Output Enable Setup Time	$t_{OES}$	10		ns
Output Enable H <sub>OL</sub> d Time	$t_{OEH}$	10		ns

### ATTRIBUTE MEMORY WRITE CYCLE<sup>4</sup>

Parameter	Symbol	Min	Max	Unit
Byte Write Cycle Time	$t_{RWR}$		10	ms
Address Setup Time	$t_{RAS}$	20		ns
Chip Enable Setup Time	$t_{RCS}$	0		ns
Output Enable Setup Time	$t_{ROES}$	20		ns
Write Pulse Width	$t_{RWP}$	100		ns
Address H <sub>OL</sub> d Time	$t_{RAH}$	50		ns
Data Setup Time	$t_{RDS}$	50		ns
Data H <sub>OL</sub> d Time	$t_{RDH}$	20		ns
Chip Enable H <sub>OL</sub> d Time	$t_{RCH}$	0		ns
Output Enable H <sub>OL</sub> d Time	$t_{ROEH}$	20		ns
Write Recovery Time	$t_{RRE}$	50		ns
End of Write to Output Time	$t_{RRBO}$		100	ns
Number of Write per Byte	N	10000		Times
Write Enable H <sub>OL</sub> d Time	$t_{RWEH}$	10		ns

Notes: <sup>1</sup> If  $\overline{OE}$ ,  $\overline{CE1}$ , and  $\overline{CE2}$  are in the Read Mode during this period, then the I/O pins are in the output state and the input signals of the phase opposite to the outputs must be applied.

<sup>2</sup> Transition is measured at the point of  $\pm 500$  mV from steady state voltage.

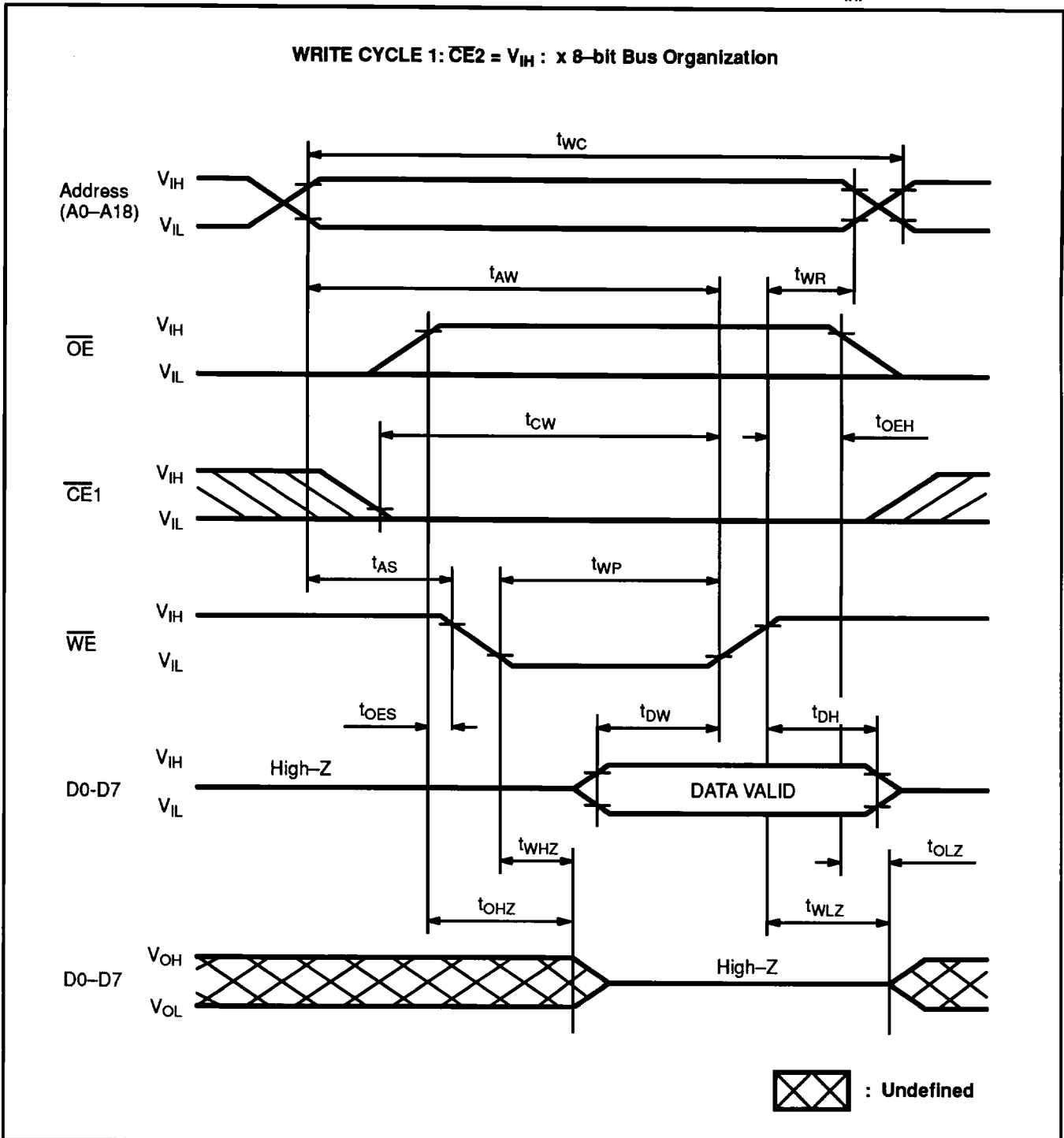
<sup>3</sup> This parameter is specified only during write cycle with  $\overline{OE} = V_{IL}$  and specified using Load II in Figure 2.

<sup>4</sup> This parameter is for MB98A90613, MB98A90713, MB98A90813, and MB98A90913.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$  = CONTROLLED,  $\overline{REG} = V_{IH}$ )

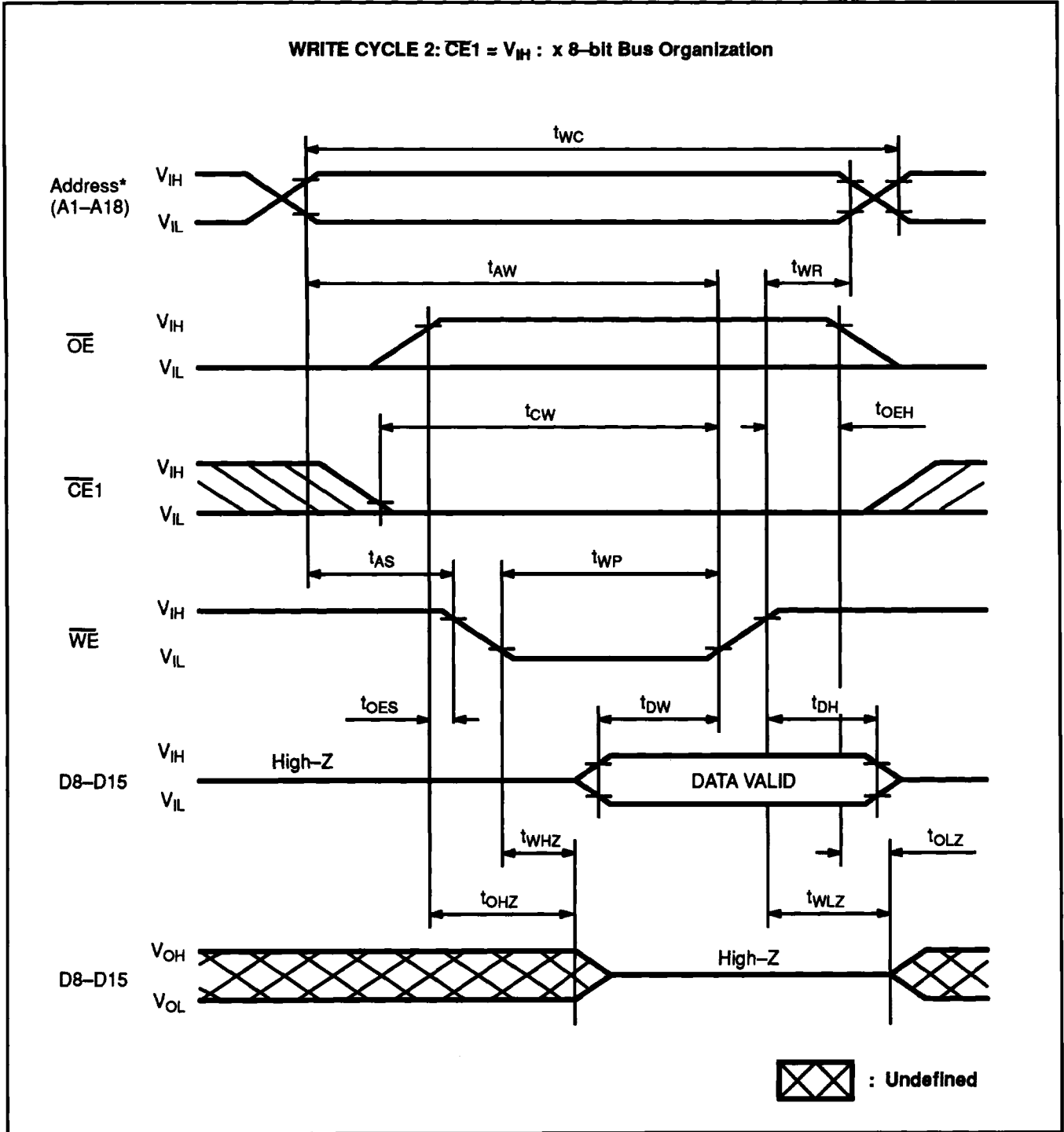


**MB98A9061x-20**  
**MB98A9071x-20**  
**MB98A9081x-20**  
**MB98A9091x-20**

**AC CHARACTERISTICS (Continued)**

(Recommended operating conditions unless otherwise noted.)

**MAIN MEMORY WRITE CYCLE TIMING DIAGRAM (WE = CONTROLLED, REG = V<sub>IH</sub>)**

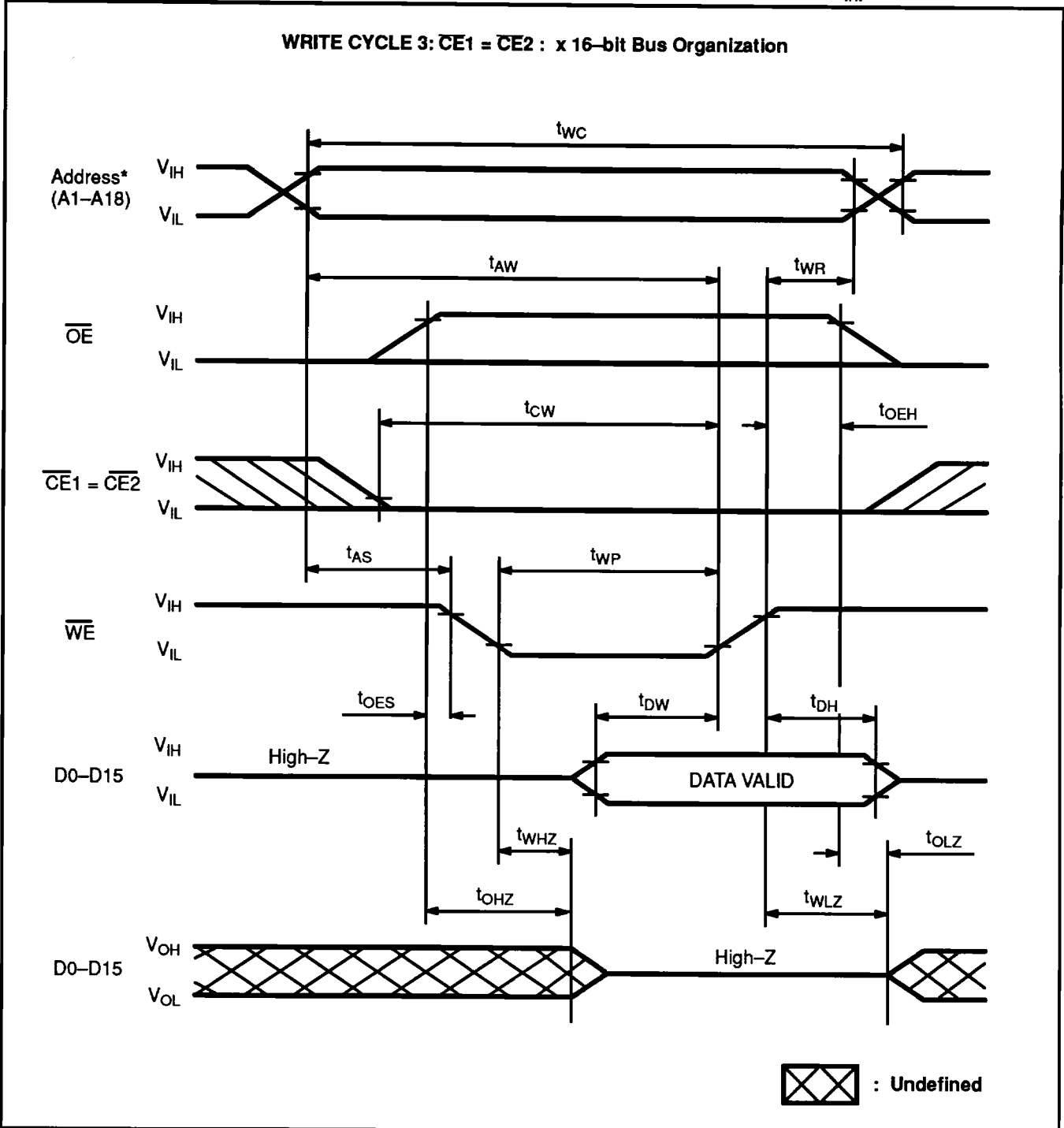


Note: \*A0 = Either V<sub>IH</sub> or V<sub>IL</sub>.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$  = CONTROLLED,  $\overline{REG} = V_{IH}$ )



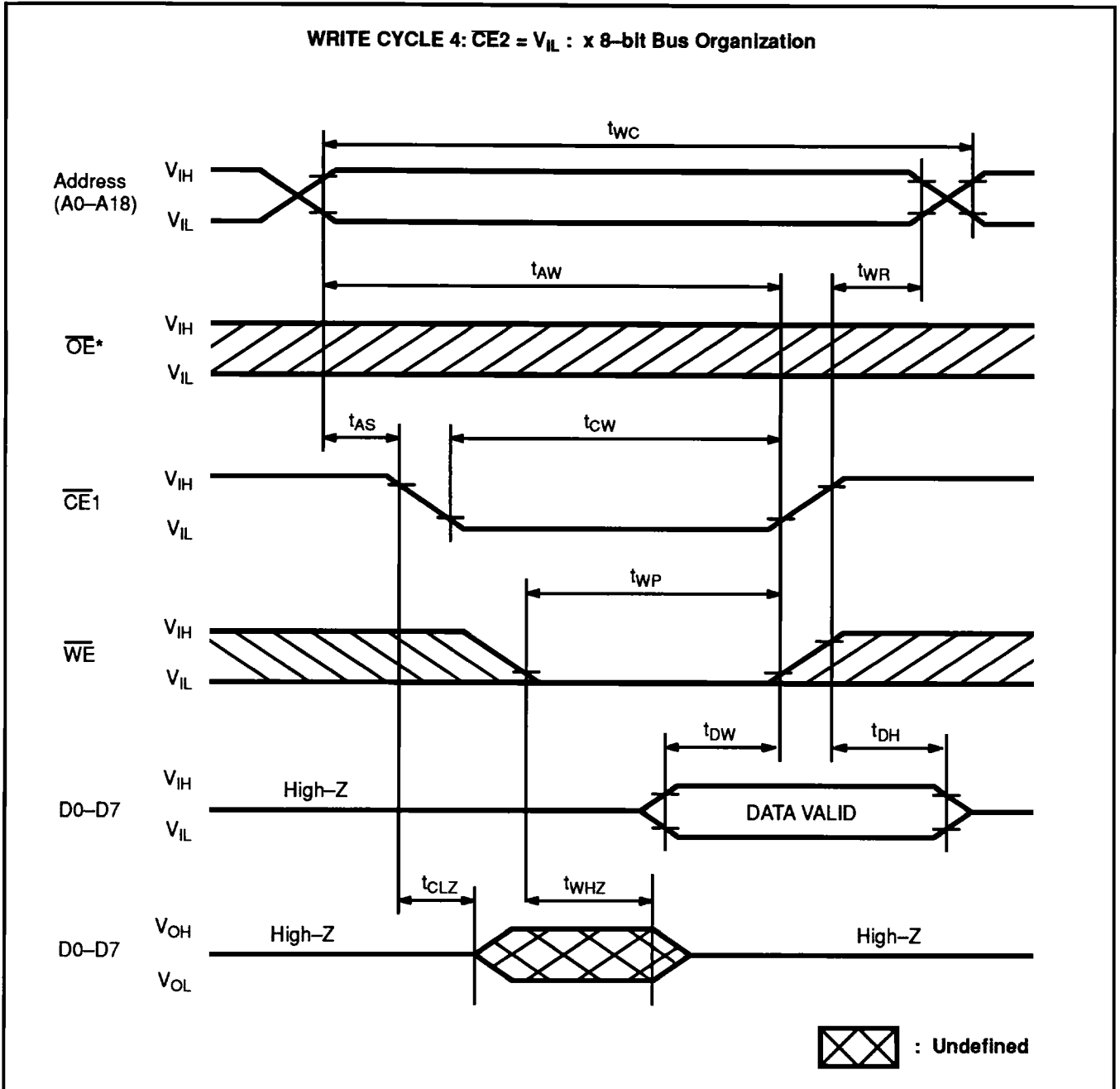
**Note:** \*A0 = Either  $V_{IH}$  or  $V_{IL}$ .

MB98A9061x-20  
 MB98A9071x-20  
 MB98A9081x-20  
 MB98A9091x-20

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ ,  $\overline{REG} = V_{IH}$ )

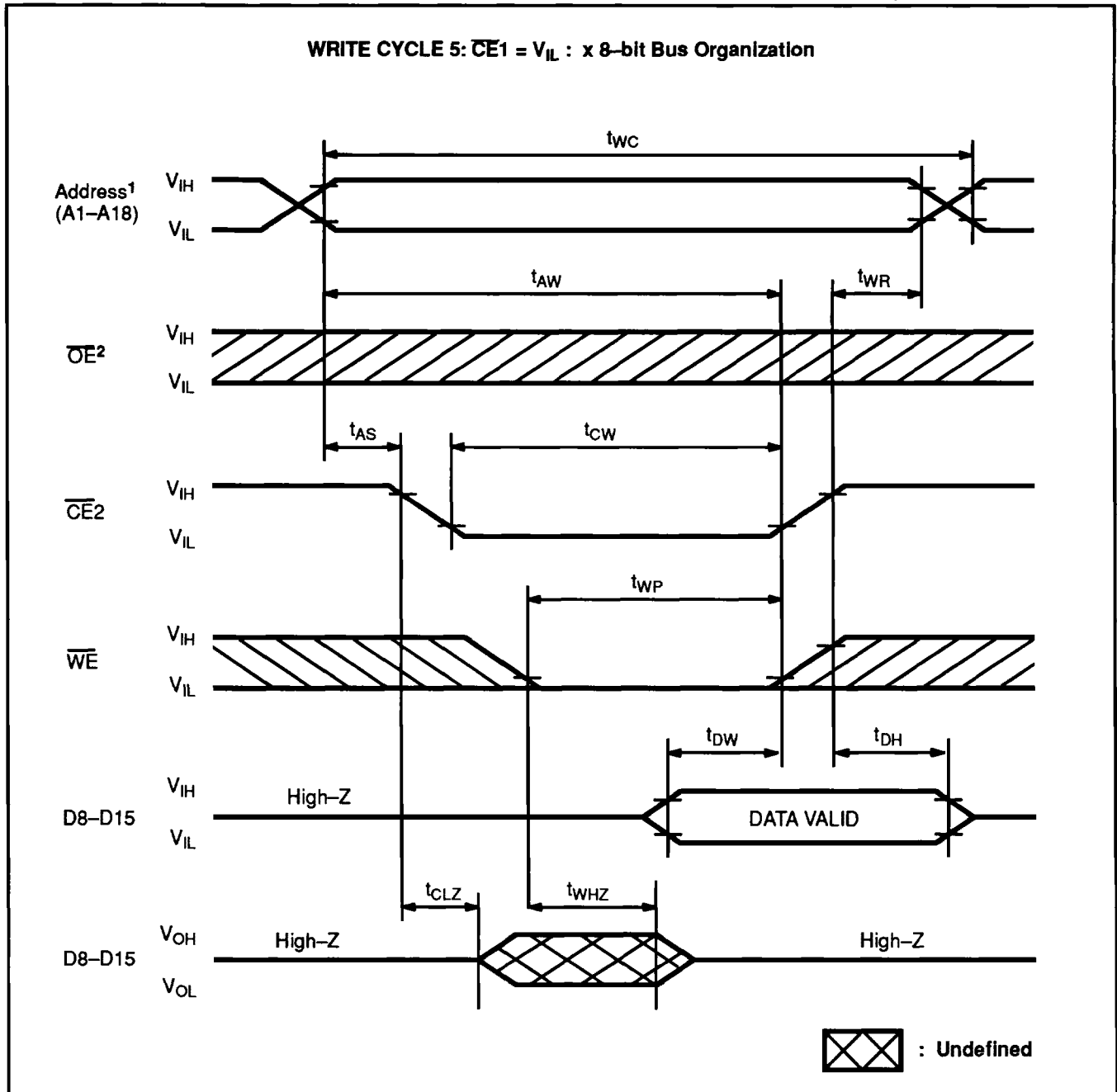


**Note:** \*H-level is recommended for stable operation though the card is operable at L-level.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ ,  $\overline{REG} = V_{IH}$ )



**Notes:**<sup>1</sup> A0 = Either  $V_{IH}$  or  $V_{IL}$ .

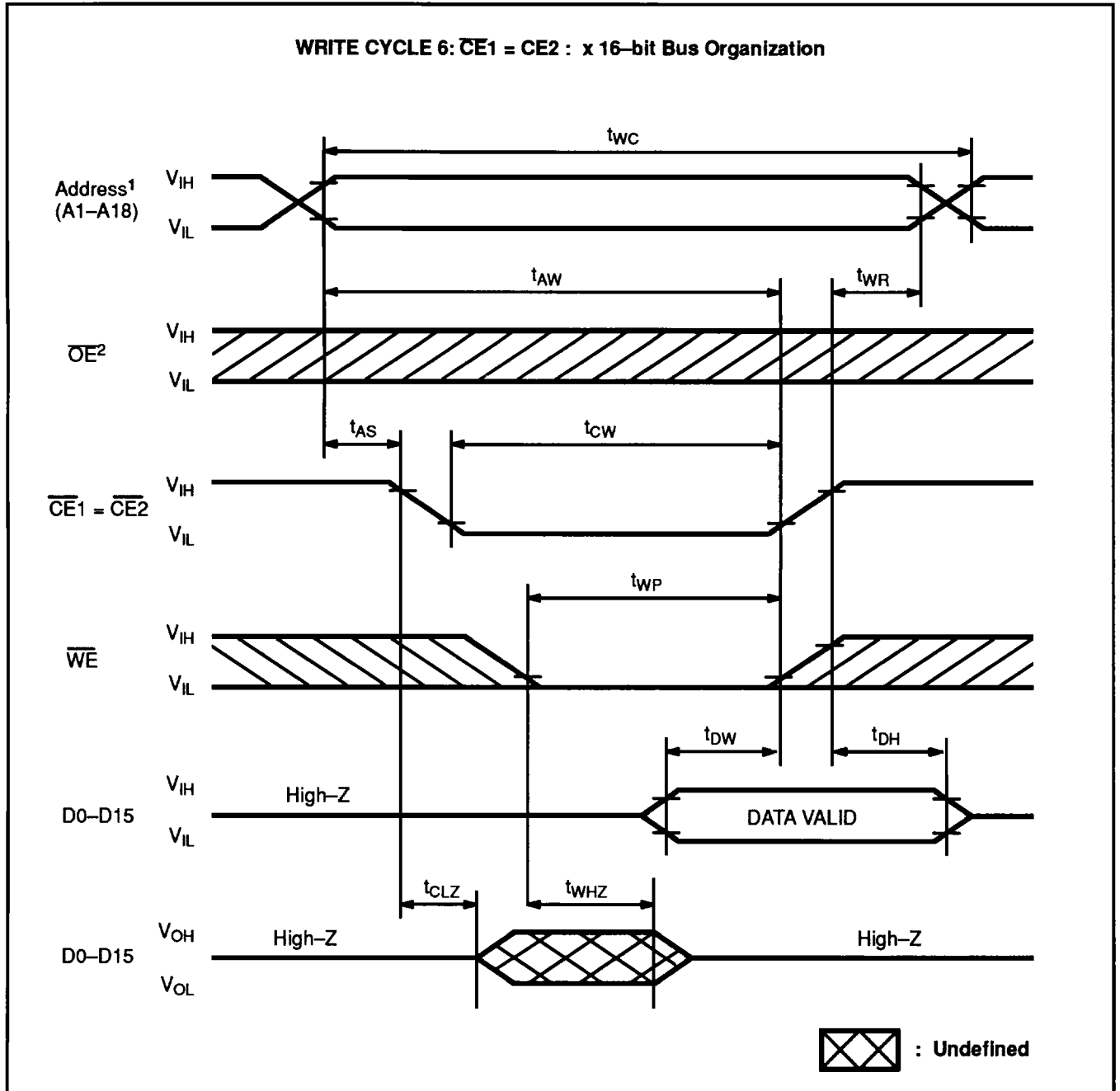
<sup>2</sup> H-level is recommended for stable operation though the card is operable at L-level.

MB98A9061x-20  
 MB98A9071x-20  
 MB98A9081x-20  
 MB98A9091x-20

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ ,  $\overline{REG} = V_{IH}$ )



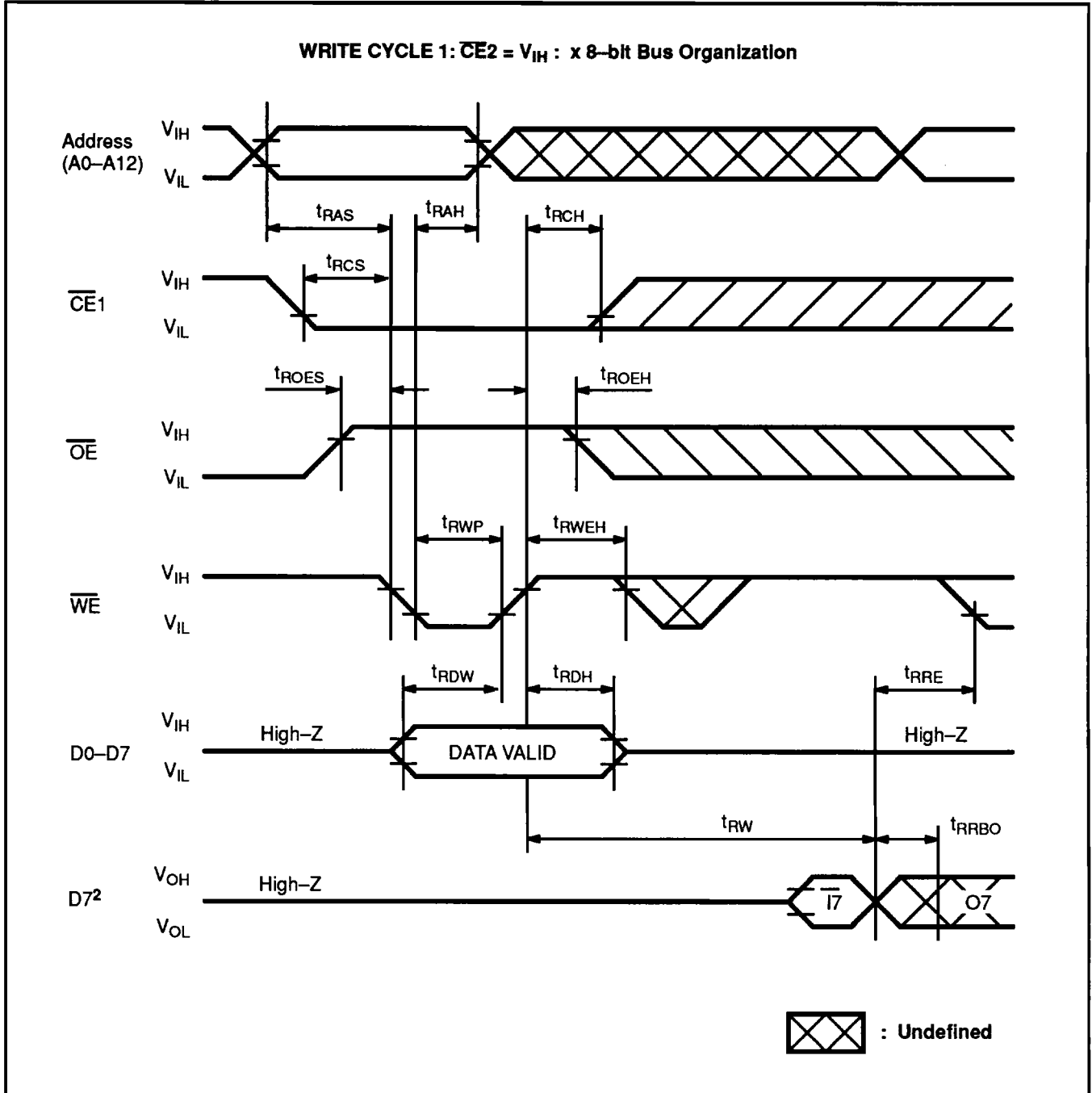
Notes: <sup>1</sup>A0 = Either  $V_{IH}$  or  $V_{IL}$ .

<sup>2</sup>H-level is recommended for stable operation though the card is operable at L-level.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$  = CONTROLLED,  $\overline{REG} = V_{IL}$ )<sup>1</sup>



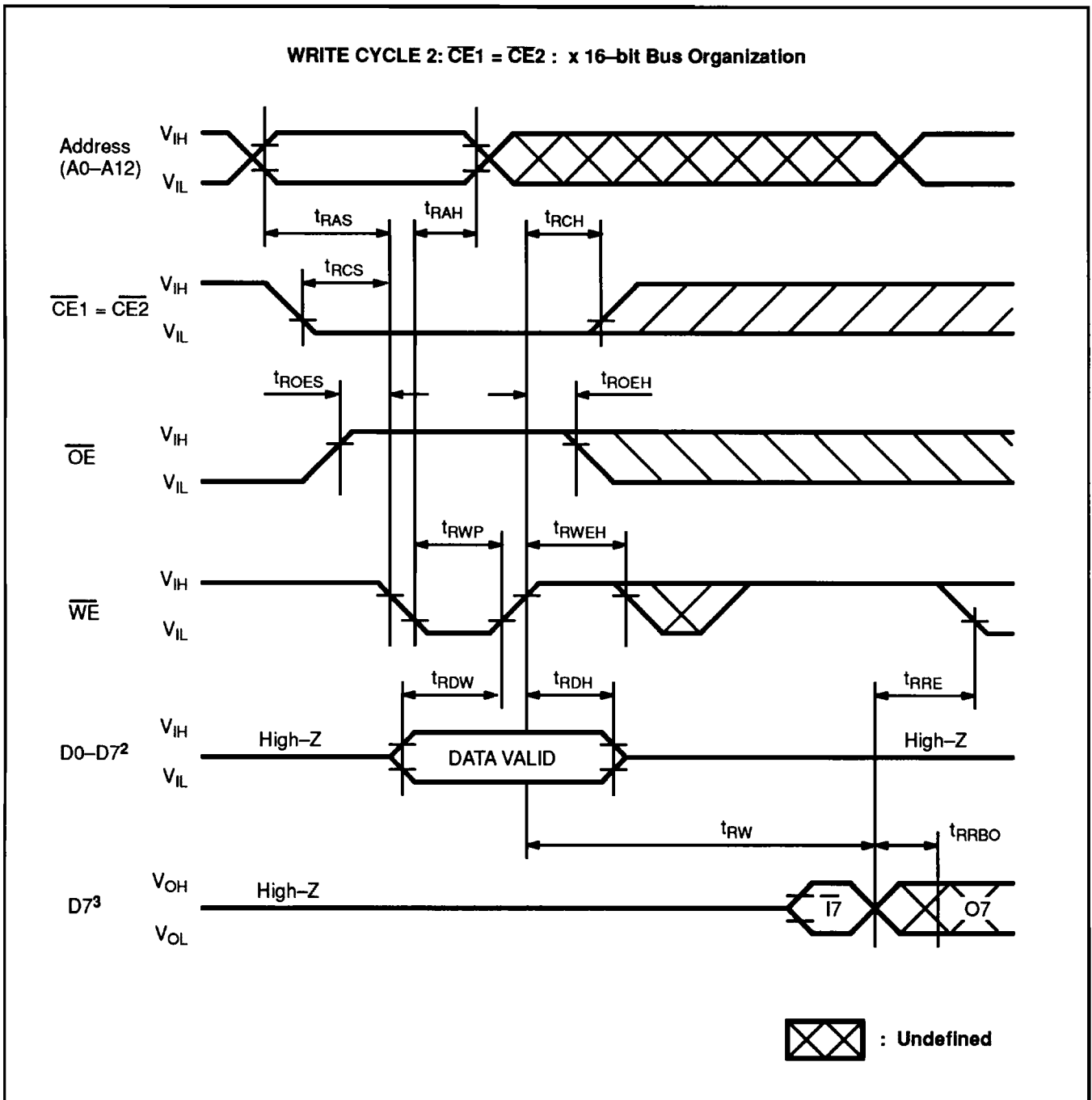
**Notes:**<sup>1</sup> This timing diagram is for MB98A90613, MB98A90713, MB98A90813, and MB98A90913. "FF" data is available on MB98A90612, MB98A90712, MB98A90812, and MB98A90912 only.

<sup>2</sup>Data polling operation.

**AC CHARACTERISTICS (Continued)**

(Recommended operating conditions unless otherwise noted.)

**ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$  = CONTROLLED,  $\overline{REG} = V_{IL}$ )<sup>1</sup>**



**Notes:**<sup>1</sup> This timing diagram is for MB98A90613, MB98A90713, MB98A90813, and MB98A90913. "FF" data is available on MB98A90612, MB98A90712, MB98A90812, and MB98A90912 only.

<sup>2</sup> H-level or L-level is output from D8 to D15.

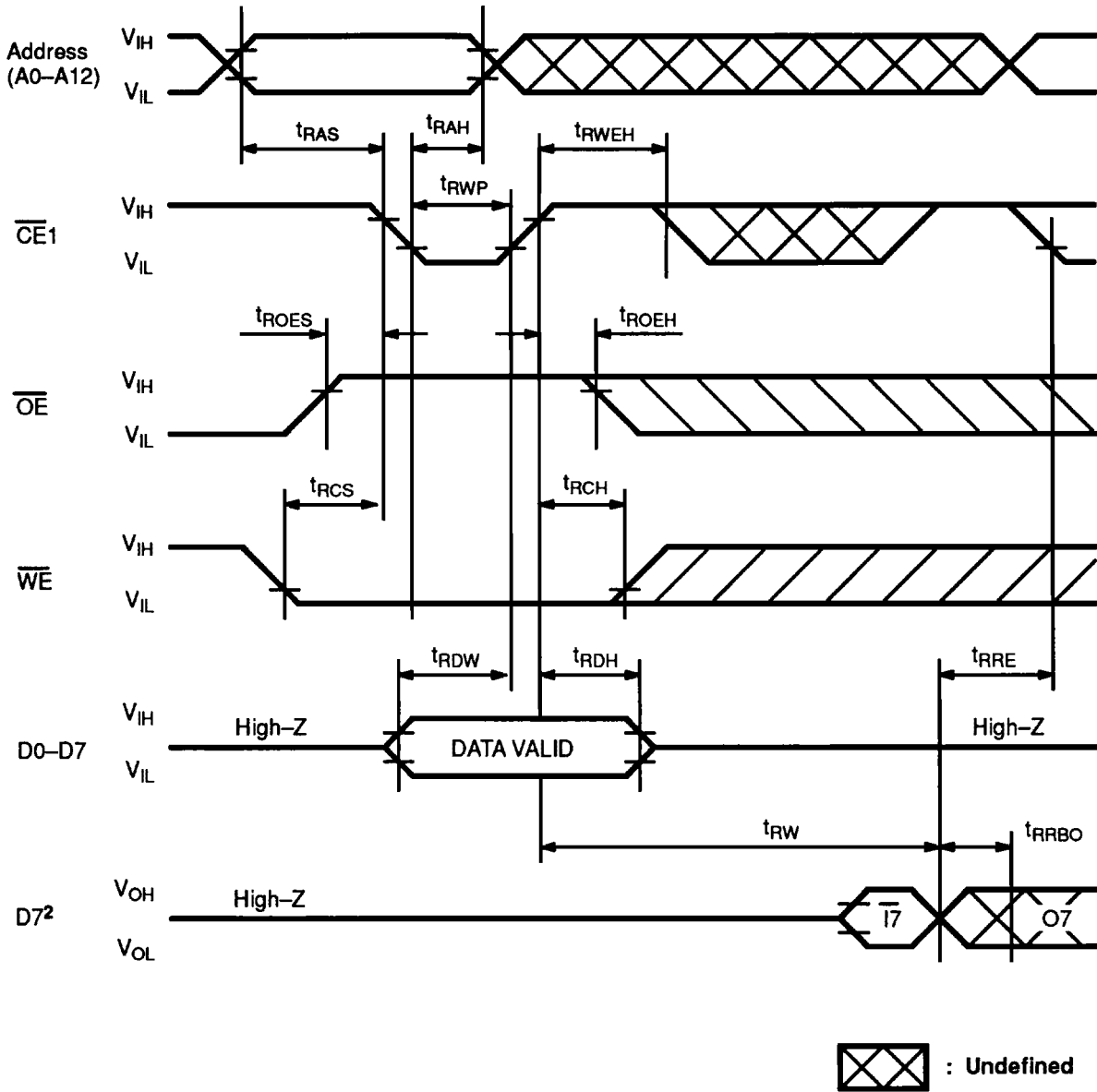
<sup>3</sup> Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ ,  $\overline{REG} = V_{IL}$ )<sup>1</sup>

WRITE CYCLE 3:  $\overline{CE}2 = V_{IH}$  : x 8-bit Bus Organization



**Notes:**<sup>1</sup> This timing diagram is for MB98A90613, MB98A90713, MB98A90813, and MB98A90913. "FF" data is available on MB98A90612, MB98A90712, MB98A90812, and MB98A90912 only.

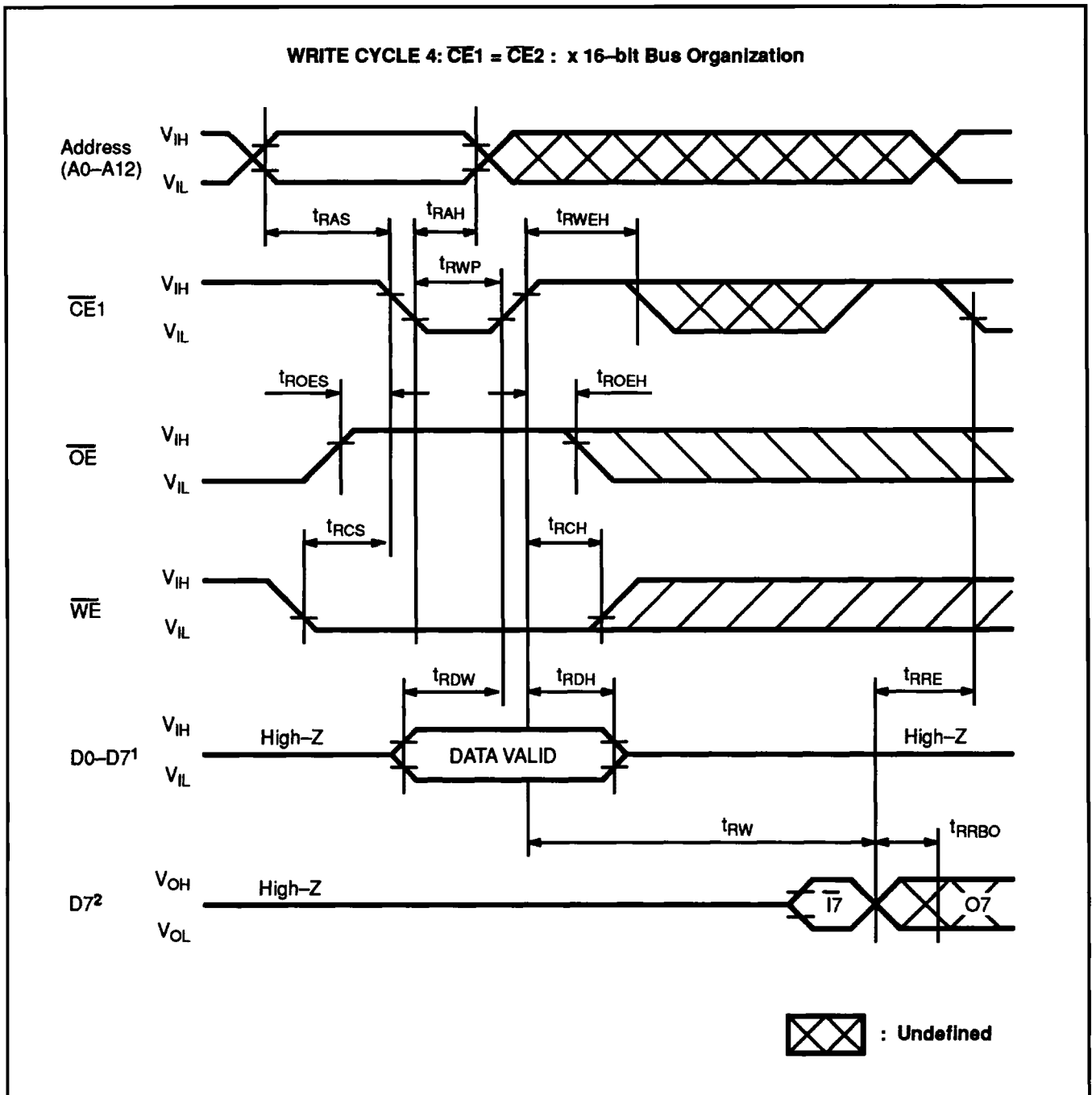
<sup>2</sup> Data polling operation.

MB98A9061x-20  
 MB98A9071x-20  
 MB98A9081x-20  
 MB98A9091x-20

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ ,  $\overline{REG} = V_{IL}$ )<sup>1</sup>



**Notes:**<sup>1</sup> This timing diagram is for MB98A90613, MB98A90713, MB98A90813, and MB98A90913. "FF" data is available on MB98A90612, MB98A90712, MB98A90812, and MB98A90912 only.

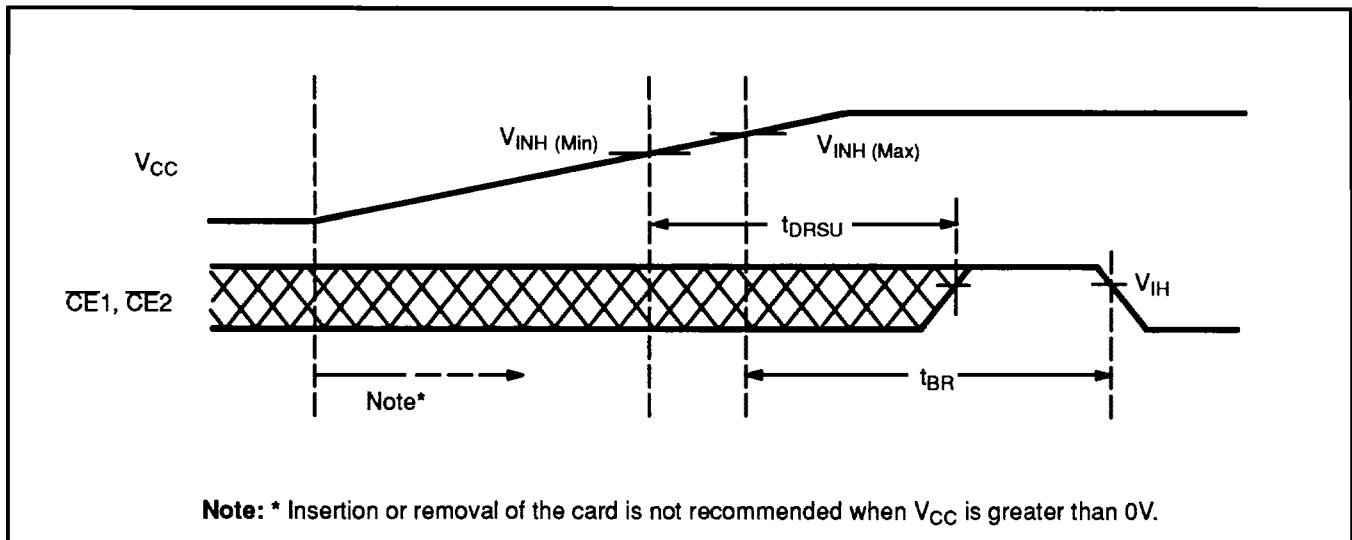
<sup>2</sup> H-level or L-level is output from D8 to D15.

<sup>3</sup> Data polling operation.

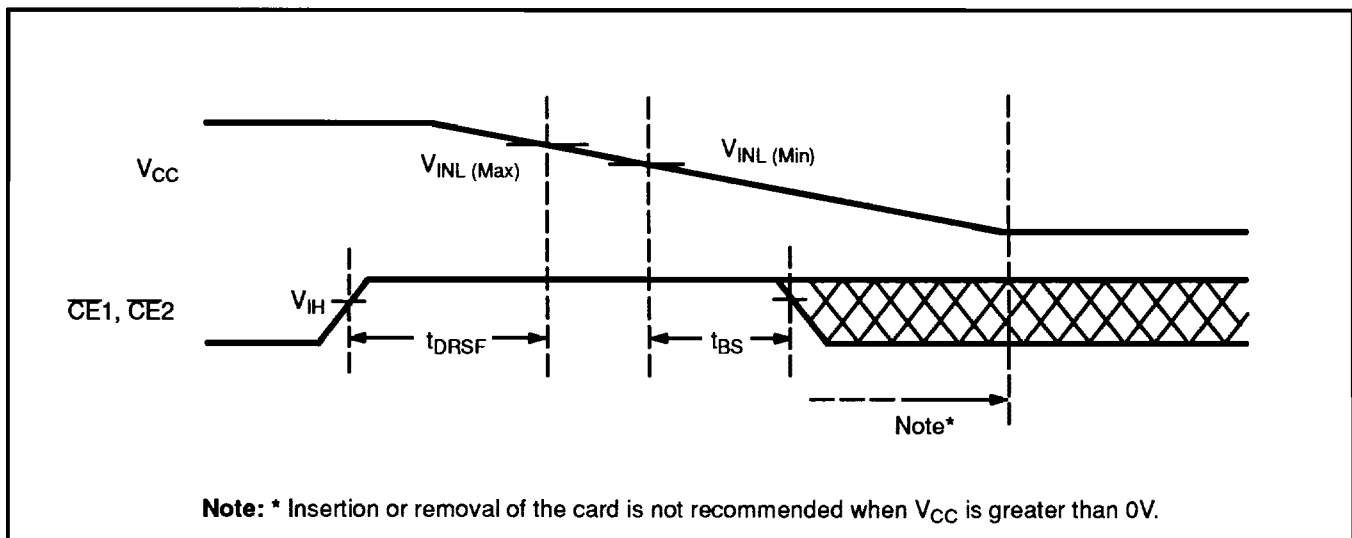
## POWER SUPPLY SEQUENCE CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Detection Rising Voltage	$V_{INH}$	4.2	4.3	4.4	V
Detection Falling Voltage	$V_{INL}$	4.1	4.2	4.3	V
Battery Backup Recovery Time	$t_{BR}$	3.0			ms
Data Retention Rising Time	$t_{DRSU}$			0.5	ms
Battery Backup Setup Time	$t_{BS}$	10			$\mu$ s
Data Retention Falling Time	$t_{DRSF}$	0			ns

### POWER-ON TIMING DIAGRAM



### POWER-OFF TIMING DIAGRAM



## UNIQUE FEATURES FOR SRAM CARD

### 1. REPLACEABLE BATTERIES FOR THE SRAM MEMORY CARD

The battery used in the SRAM Memory Card is a 3V Lithium battery (coin type) with the following specifications:

Diameter	: 23.0 (mm)
Thickness	: 2.5 (mm)
Weight	: 3.2 (g) Approx.
Type	: CR2325, or equivalent

### 2. APPROXIMATE DATA RETENTION TIME WITH BATTERY SUPPORT ONLY

Part Number	Approx. Data Retention Time * (TA=20°C)
MB98A9061x	48 months min.
MB98A9071x	24 months min.
MB98A9081x	12 months min.
MB98A9091x	6 months min.

\* Determined by the memory density of the card;  
i.e., greater card density means less battery time.

### 3. REPLACING THE BATTERY IN THE SRAM MEMORY CARD

- a. Insert a slender pointed object, such as the end of a paper clip, into the hole on the upper side of the card. (See Figure 4.)
- b. Release the battery holder by pressing the paper clip against the catch and pulling the battery holder straight out from the card. (The battery cavity is located at the top of the card. See Figure 5.) When the battery holder is free from the card the battery will fall out.
- c. Replace the old battery with a fresh one. Be certain to match battery polarity to the + and - shown on the holder.
- d. Place the new battery into the holder, squeeze the holder containing the new battery tightly, and reinsert it into the battery cavity.

**WARNING**  
 Battery **MUST** be replaced within 30 minutes\* or data will be lost.

**Note:** \*Providing the SRAM card had been inserted into application system more than 10 minutes.

Figure 4. SRAM CARD DRAWING (TOP VIEW)

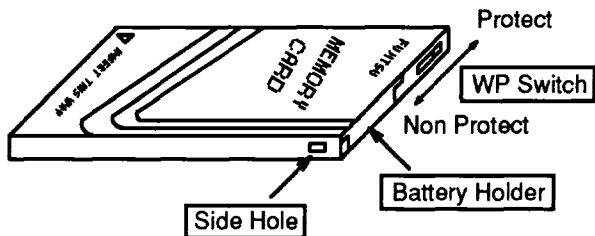
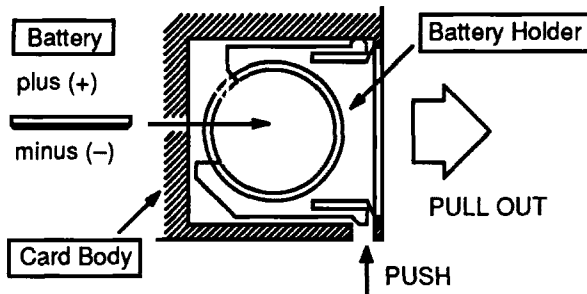


Figure 5. BATTERY CASE DRAWING (TOP VIEW)



## UNIQUE FEATURES FOR SRAM CARD (Continued)

### 4. SPECIAL MONITORING PINS

#### 4.1 BVD1, BVD2: Voltage Monitoring Pins

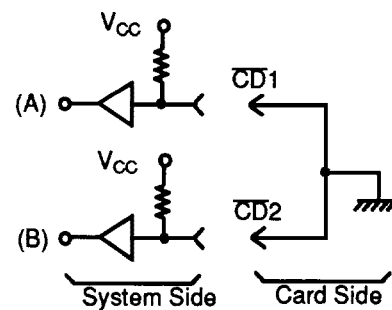
These pins monitor the voltage of the battery which must be maintained at 2.65V or greater for data retention. The condition of the battery is determined by reading the output signals on BVD1 and BVD2.

1. When  $BVD1=BVD2=V_{OH}$   
 Battery voltage is sufficient to guarantee data retention; i.e.,  $\geq 2.65V$ .
2. When  $BVD2=V_{OL}$ ,  $BVD1=V_{OH}$   
 Battery voltage is lower than 2.65V and should be replaced to safeguard data.
3. When  $BVD1=BVD2=V_{OL}$   
 Battery voltage is less than 2.37V: the level is dangerous. There is a possibility that data has not retained.

\* If the battery is removed, BVD1, BVD2 will not function.

#### 4.2 CD1, CD2: Card Detection Pins

These pins detect the insertion of the card into the system. (See Figure 6.)  
 When the memory card has been correctly inserted, CD1 and CD2 are detected by the system. CD1, CD2 are tied to ground on the card side as shown in Figure 6.



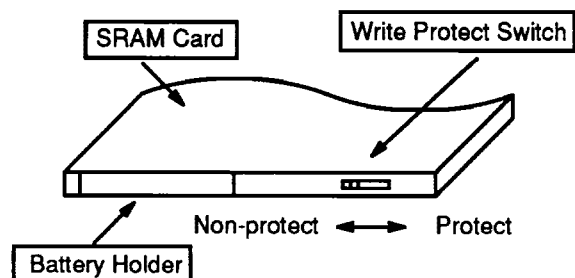
- Figure 6 -

#### 4.3 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Figure 7, the SRAM card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non-protect" position and the WE pin low. L-level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the "Protect" position. H-level is output on the WP pin.

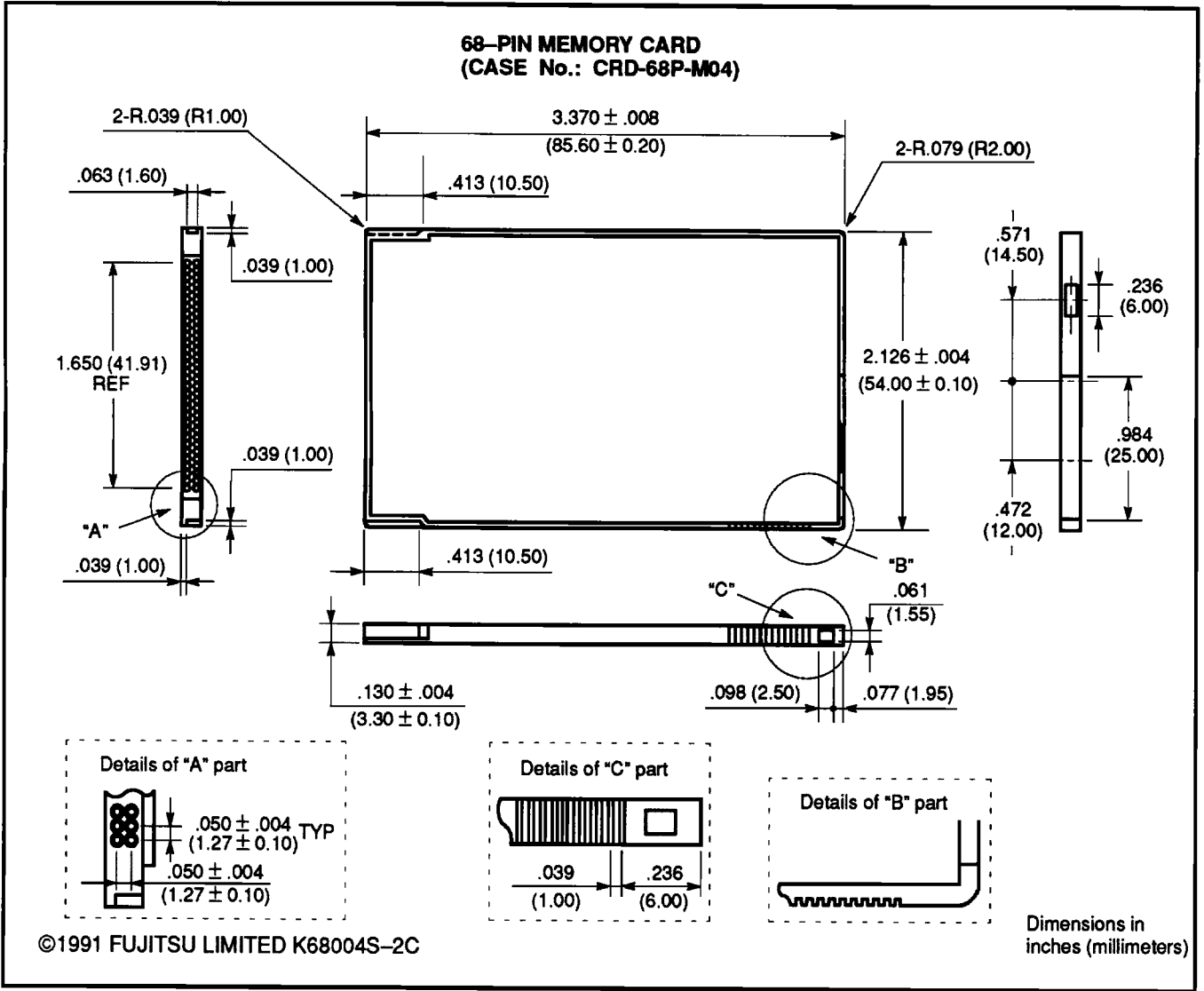


- Figure 7 -

WP Switch	WP
Protect	H
Non-protect	L

**MB98A9061x-20**  
**MB98A9071x-20**  
**MB98A9081x-20**  
**MB98A9091x-20**

**PACKAGE DIMENSIONS**



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**MB98A9061x-20**  
**MB98A9071x-20**  
**MB98A9081x-20**  
**MB98A9091x-20**

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