SPEED/PACKAGE AVAILABILITY

8241, 42—A, F, W
82S41, S42—A, F

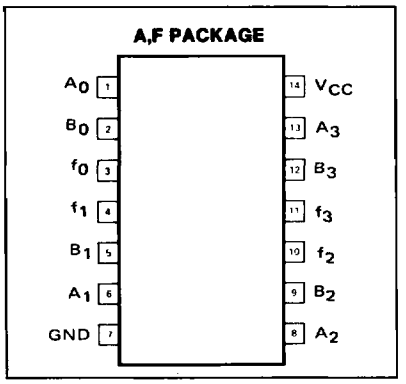
DESCRIPTION

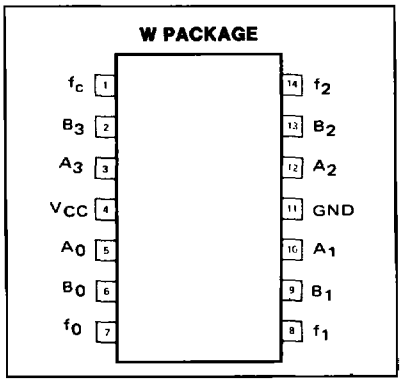
The 8241 contains four independent gating structures to perform the Exclusive-OR function on two input variables.

The output of the 8241 employs the totem-pole structure characteristic of TTL devices.

The 8242 contains four independent Exclusive-NOR gates which may be used to implement digital comparison functions. The 8242 outputs are bare collector to facilitate implementation of multiple-bit comparisons; a 4-bit comparison is made by connecting the outputs of the four independent gates together.

PIN CONFIGURATION





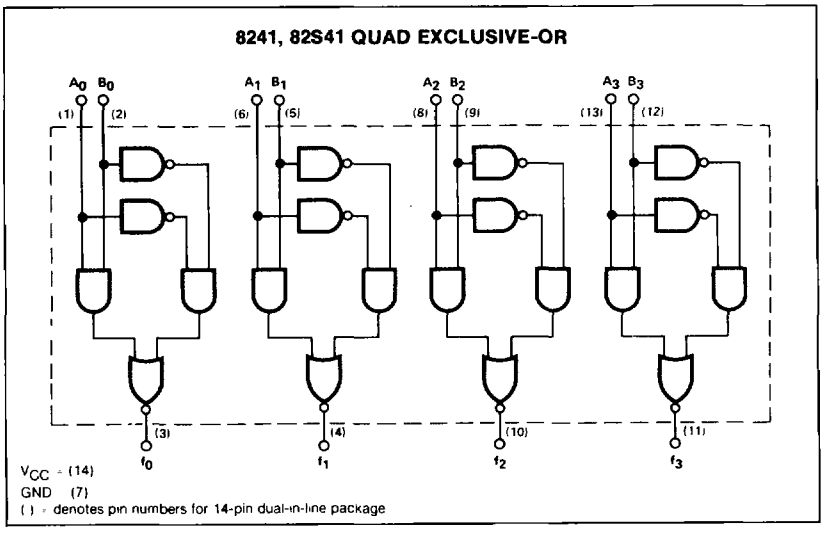
TRUTH TABLE

	A	B	f
8241/82S41	0	0	0
	1	0	1
	0	1	1
	1	1	0
8242/82S42	0	0	1
	1	0	0
	0	1	0
	1	1	1

SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

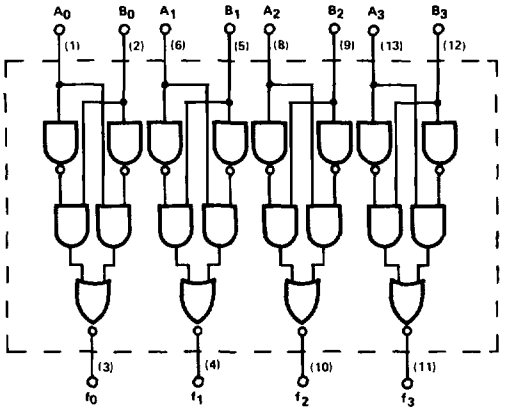
	LIMITS								
	8241		8242		82S41		82S42		
PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNIT
Propagation Delay									
t_{on} Turn-on time	17	23			7	10	9	14	ns
t_{off} Turn-off time	11	17			7	10	9	14	
Inverting path									
t_{on} Turn-on time			12	20					
t_{off} Turn-off time			14	23					
Non-inverting path									
T_{on} Turn-on time			14	2					
t_{off} Turn-off time			20	28					

LOGIC DIAGRAM



LOGIC DIAGRAM

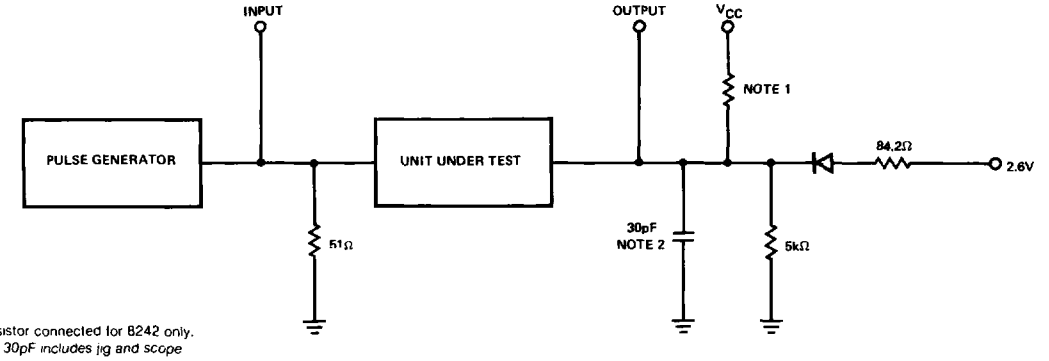
8242 4-BIT DIGITAL COMPARATOR (OPEN COLLECTOR)



V_{CC} (14)
GND (7)
( ) : denotes pin numbers for 14 pin dual-in-line package

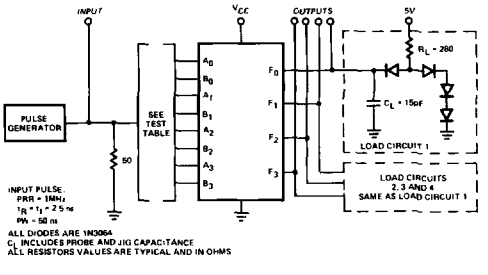
AC TEST FIGURE

8241, 8242



NOTE:
1. 530Ω resistor connected for 8242 only.
2. 5kΩ and 30pF includes jig and scope

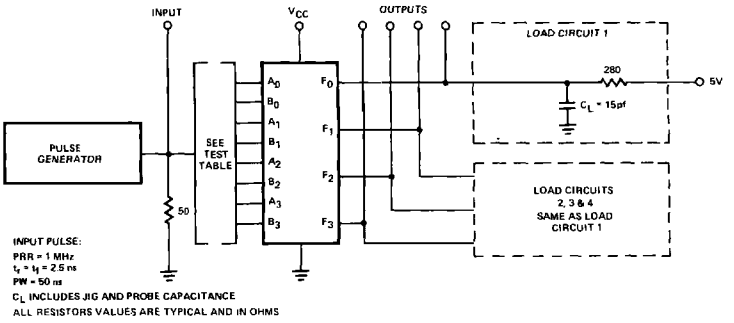
82S41



LOGIC

AC TEST FIGURE

82S42



TEST TABLE—82S41

	INPUTS								OUTPUTS			
	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3
	0	0	PG	1	0	0	0	0		T		
	0	0	1	PG	0	0	0	0		T		
3	PG	1	0	0	0	0	0	0	T			
	1	PG	0	0	0	0	0	0	T			
5	0	0	0	0	1	PG	0	0		T		
6	0	0	0	0	PG	1	0	0			T	
7	0	0	0	0	0	0	1	PG				T
8	0	0	0	0	0	0	0	PG	1			T

"1"=2.7V, "0"=GROUND

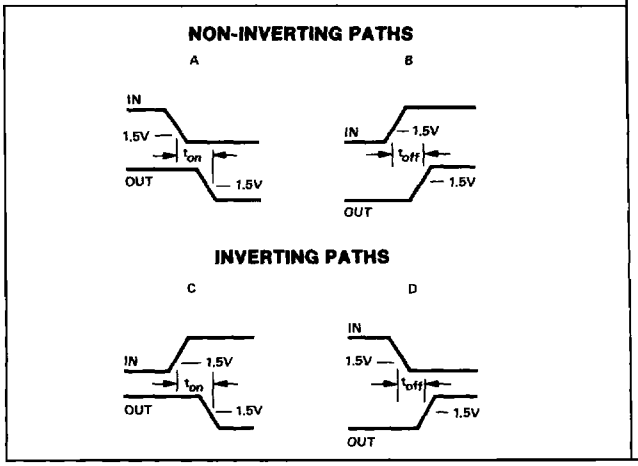
TEST TABLE—82S42

TEST	INPUTS								OUTPUTS			
#	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3
1	0	0	PG	1	0	0	0	0		T		
2	0	0	1	PG	0	0	0	0		T		
3	PG	1	0	0	0	0	0	0	T			
4	1	PG	0	0	0	0	0	0	T			
5	0	0	0	0	1	PG	0	0			T	
6	0	0	0	0	PG	1	0	0			T	
7	0	0	0	0	0	0	1	PG				T
8	0	0	0	0	0	0	PG	1				T

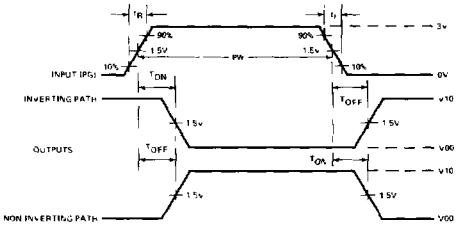
"1" = 2.7V, "0" = GROUND

NOTE
1. AC test jigs must not have any switches.
2. AC test jigs must have less than ⅛ inch lead length from package pins.

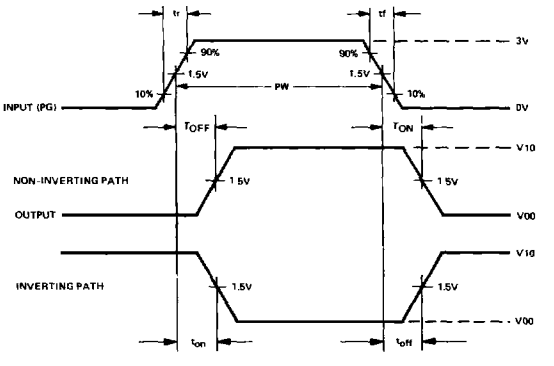
PROPAGATION DELAY WAVEFORMS



82S41

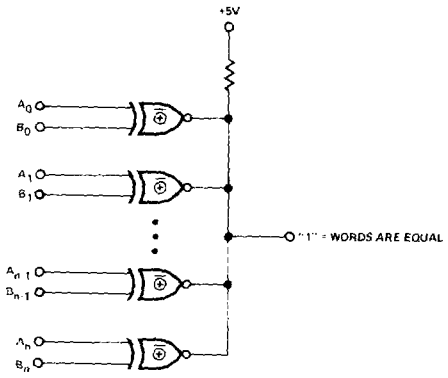


82S42

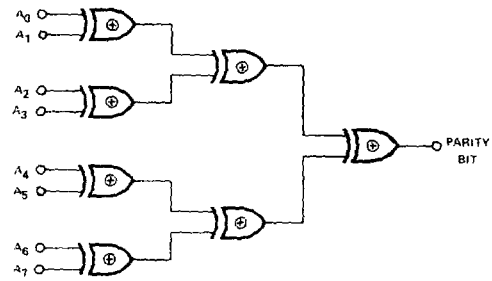


TYPICAL APPLICATIONS

EQUALITY GATE USED FOR COMPARISON



PARITY GENERATOR/TESTER



8-BIT POSITION SCALER 8243

8243-N,F,Q

LOGIC

DESCRIPTION

The 8243 8-Bit Position Scaler is an MSI array of approximately 70 gate complexity. The primary function of the 8243 is to scale (or shift) data bit positions by a selection of a 3-bit binary selector code.

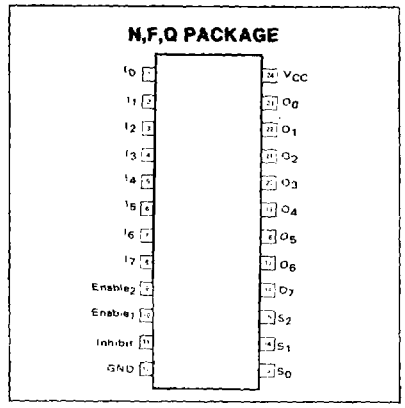
The most significant bit input (I_7) may be shifted 8 positions to the least significant bit output (O_0). At zero shift, or scale select, all eight input data bits are transferred and inverted to their respective outputs, (I_0 to O_0, I_1 to O_1, I_2 to O_2, etc.) At a shift, or scale select, of one, each input bit (I_n) will shift to the next lower output bit (O_n-1). See truth table for other shift codes.

The 8243's advantages over shift registers are the speed of operation and lower complexity of external logic required to effect a scale function. The speed of the 8243 Scaler is a function of gate propagation delays—the speed of equivalent shift registers is the time for clock periods plus the propagation delay to effect a scale function.

The 8243 is provided with open collector outputs to provide expansion to larger scaling functions. Data input logic zero loading is reduced to less than —100μA when the unit is disabled.

PIN CONFIGURATION

N,F,Q PACKAGE



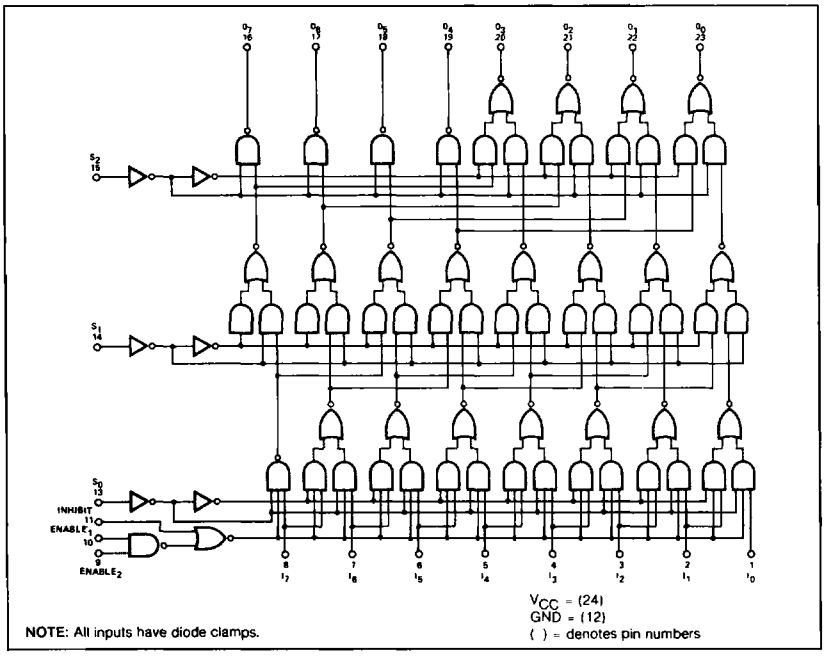
TRUTH TABLE

INHIBIT	ENABLE 1 & 2	S_0	S_1	S_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	1	0	0	0	$\bar{I}_0$	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$
0	1	1	0	0	$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1
0	1	0	1	0	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1
0	1	1	1	0	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1
0	1	0	0	1	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1
0	1	1	0	1	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1	1
0	1	0	1	1	$\bar{I}_6$	$\bar{I}_7$	1	1	1	1	1	1
0	1	1	1	1	$\bar{I}_7$	1	1	1	1	1	1	1
1	X	X	X	X	1	1	1	1	1	1	1	1
X	0	X	X	X	1	1	1	1	1	1	1	1

X indicates either logic "1" or logic "0" may be present.

8243-N,F,Q

LOGIC DIAGRAM



NOTE: All inputs have diode clamps.

SWITCHING CHARACTERISTICS T_A = 25°C and V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	LIMITS TYP	LIMITS MAX	UNIT
Propagation delay				
Data in	I_n,S_0,S_1,S_2,	20	32	ns
Select S_n	Enable 1 & 2	30	40	
Inhibit	Inhibit = 10mA	25	35	
Enable 1 & 2		30	45	

NOTES
I_n "0" threshold 0.7 volts for S8243.

AC TEST TABLES

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	1	A	B	C	D	E	F	RIGHT
2	1	1	A	B	C	D	E	
3	1	1	1	A	B	C	D	
4	1	1	1	1	A	B	C	
5	1	1	1	1	1	A	B	SCALE = 0
6	1	1	1	1	1	1	A	AROUND = 0
7	1	1	1	1	1	1	1	

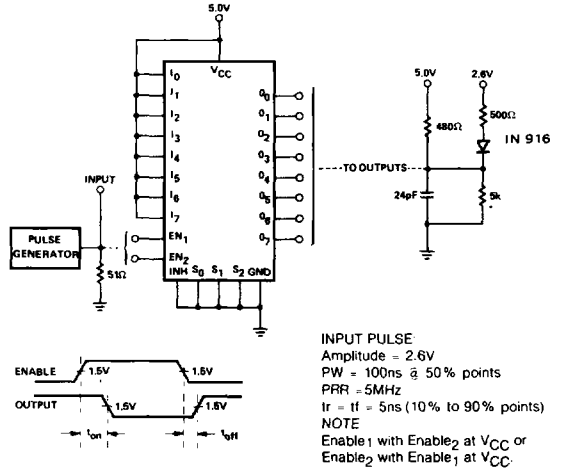
SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	B	C	D	E	F	G	1	LEFT
2	C	D	E	F	G	1	1	
3	D	E	F	G	1	1	1	
4	E	F	G	1	1	1	1	
5	F	G	1	1	1	1	1	SCALE = 1
6	G	1	1	1	1	1	1	AROUND = 0
7	1	1	1	1	1	1	1	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	G	A	B	C	D	E	F	RIGHT
2	F	G	A	B	C	D	E	& AROUND
3	E	F	G	A	B	C	D	
4	D	E	F	G	A	B	C	
5	C	D	E	F	G	A	B	SCALE = 0
6	B	C	D	E	F	G	A	AROUND = 1
7	A	B	C	D	E	F	G	

SCALE FACTOR	OUTPUTS 1	2	3	4	5	6	7	
0	A	B	C	D	E	F	G	SCALE
1	B	C	D	E	F	G	A	LEFT
2	C	D	E	F	G	A	B	& AROUND
3	D	E	F	G	A	B	C	
4	E	F	G	A	B	C	D	
5	F	G	A	B	C	D	E	SCALE = 1
6	G	A	B	C	D	E	F	AROUND = 1
7	A	B	C	D	E	F	G	

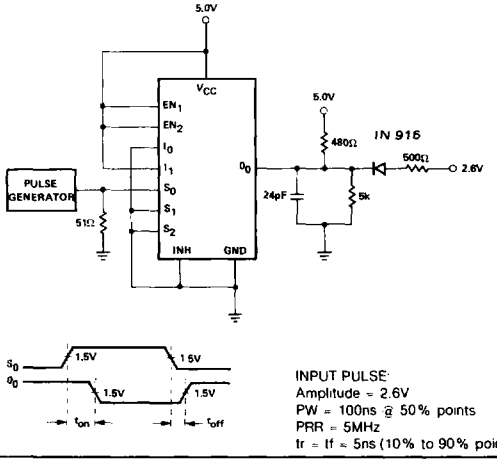
AC TEST FIGURE AND WAVEFORMS

PROPAGATION DELAY, ENABLE TO OUTPUT



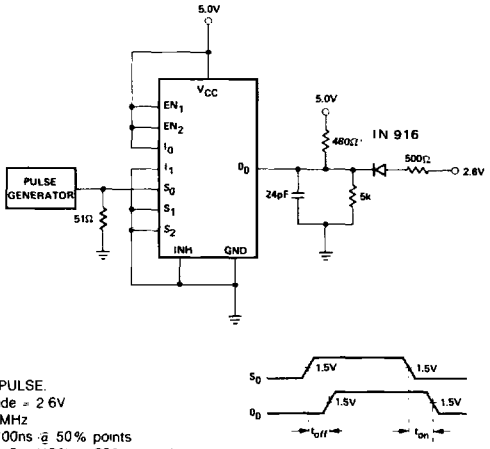
INPUT PULSE:
Amplitude = 2.6V
PW = 100ns @ 50% points
PRR = 5MHz
tr = tf = 5ns (10% to 90% points)
NOTE
$Enable_1$ with $Enable_2$ at V_{CC} or
$Enable_2$ with $Enable_1$ at V_{CC}

PROPAGATION DELAY, DATA INPUT TO DATA OUTPUT



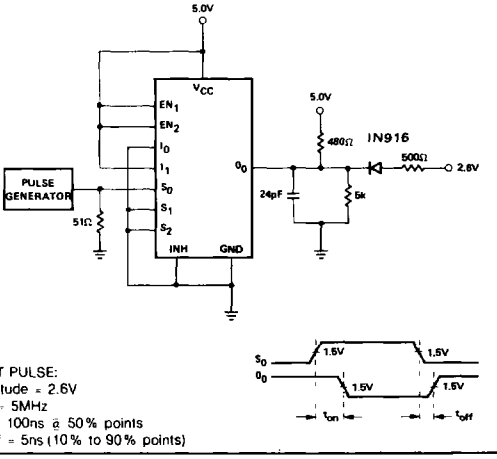
INPUT PULSE:
Amplitude = 2.6V
PW = 100ns @ 50% points
PRR = 5MHz
tr = tf = 5ns (10% to 90% points)

PROPAGATION DELAY, DATA SELECT TO OUTPUT



INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz
PW = 100ns @ 50% points
tr = tf = 5ns (10% to 90% points)

PROPAGATION DELAY, DATA SELECT TO OUTPUT



INPUT PULSE:
Amplitude = 2.6V
PRR = 5MHz
PW = 100ns @ 50% points
tr = tf = 5ns (10% to 90% points)

LOGIC

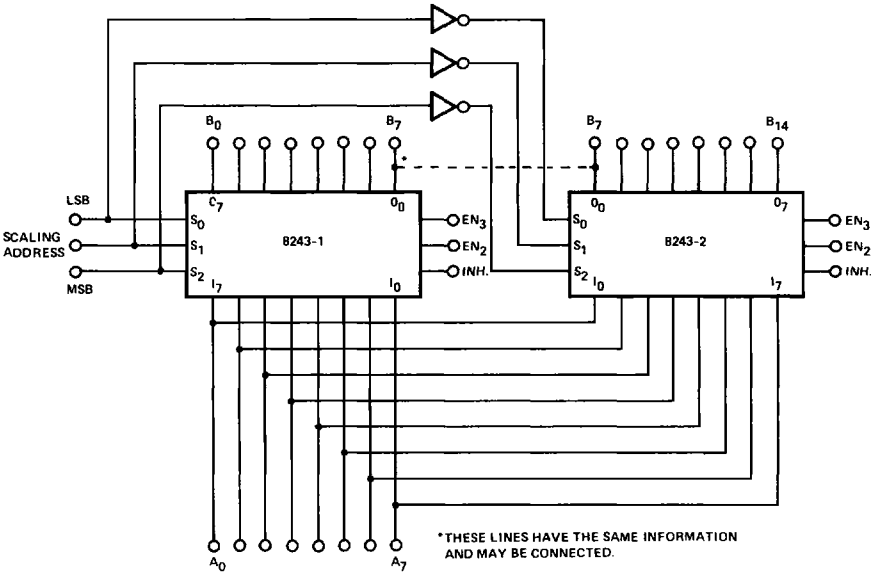
TRUTH TABLE FOR ARRAY EXPANSION

SCALE ADDRESS			8243-1								8243-2							
MSB		LSB	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}
0	0	0	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	$\overline{A}_7$	1	1	1	1	1	1	1
0	0	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_6$	$\overline{A}_7$	1	1	1	1	1	1
0	1	0	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1	1	1	1
0	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1	1	1
1	0	0	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1	1
1	0	1	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1	1
1	1	0	1	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	1
1	1	1	1	1	1	1	1	1	1	$\overline{A}_0$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$

8243-N,F,Q

TYPICAL APPLICATIONS

ARRAY EXPANSION



BI-DIRECTIONAL 8-POSITION SHIFTER