

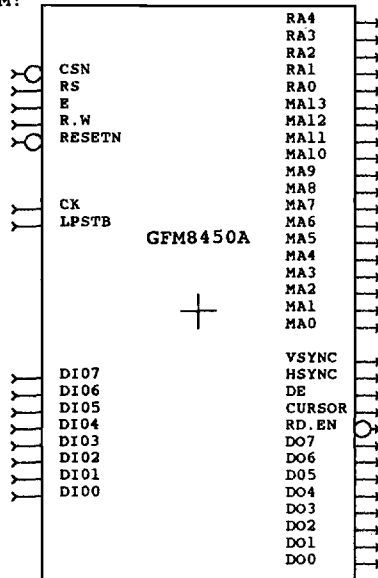
GFM8450A

CRT CONTROLLER

GENERAL DESCRIPTION:

THE GFM8450A MEGAFUNCTION IS DESIGNED TO BE FUNCTIONALLY COMPATIBLE WITH THE HITACHI HD6845 "S" VERSION, ALTHOUGH THE I/O'S ARE DIFFERENT (SEE PAGE 3 OF 3 FOR A DESCRIPTION OF THE ENHANCEMENTS TO THE HD6845 "S" VERSION). THE PERFORMANCE OF THE GFM8450A IS MUCH IMPROVED. FOR A DETAILED FUNCTIONAL DESCRIPTION, SEE THE HITACHI DATA BOOK.

PIN DIAGRAM:



- GATES USED - 2792
- AREA USED - 3000 GATE LOCATIONS
- LL7000 SERIES COMPATIBLE
- LSA2000 SERIES COMPATIBLE

INPUT LOADING: (LOADING IN TRANSISTOR PAIRS)

CSN - 1.5 E - 4 RESETN - 2 LPSTB - 5.4 DI07:0 - 3.4
RS - 3 R.W - 2 CK - 10

OUTPUT DRIVE: (DRIVE IN (#P, #N))

RA4:1 - (1,1) VSYNC - (1,0.33) CURSOR - (1,0.5)
RA0 - (2,1) HSYNC - (2,1) RD.EN - (4,4)
MA13:0 - (1,1) DE - (1,0.33) DO7:0 - (1,0.5)

NDL SYNTAX:

Z(RA4, RA3, RA2, RA1, RA0, MA13, MA12, MA11, MA10, MA9, MA8, MA7, MA6, MA5, MA4, MA3, MA2, MA1, MA0, VSYNC, HSYNC, DE, CURSOR, RD.EN, DO7, DO6, DO5, DO4, DO3, DO2, DO1, DO0)

-GFM8450A (CSN, RS, E, R.W, RESETN, CK, LPSTB, DI07, DI06, DI05, DI04, DI03, DI02, DI01, DI00)\$

AC CHARACTERISTICS*:

ITEM	MIN.	MAX.
T(CYC)C	100	
PW(CH)	50	
PW(CL)	50	
T(MAD)		50
T(RAD)		50
T(DTD)		50
T(CDD)		50
T(HSD)		50
T(VSD)		50
PW(LPH)	50	
T(LPD1)		20
T(CYC)E	100	
PW(EH)	50	
PW(EL)	50	
T(AS)	20	
T(DDR) RD		20
T(H)	10	
T(AH)	10	
T(ACC) RD		40
T(DSW) WR	10	

*ALL UNITS ARE IN NS AND ARE TYPICAL (7K TECHNOLOGY)

APPLICATION NOTE:

This megafunction can be used to duplicate the function of the Hitachi HD6845 S version by using the circuit diagram shown below.

HD6845 S VERSION ENHANCEMENTS:

Although the GFM8450A is designed to be functionally identical to the HD6845 S version, its I/O's are not exactly the same. Each of the bidirectional pins of the HD6845 become three pins in the GFM8450A. One pin is for the input, and the second and third pins are for the output and output enable. The I/O's of the GFM8450A can be made compatible with the standard part as shown in the diagram below. Note that the RD.EN output is used to gate the output of the data lines. All of the other signals are compatible with the standard part.

