Am9512

Arithmetic Processor

DISTINCTIVE CHARACTERISTICS

- Single (32-bit) and double (64-bit) precision capability
- Add, subtract, multiply and divide functions
- Compatible with proposed IEEE format
- Easy interfacing to microprocessors
- 8-bit data bus
- Standard 24-pin package
- 12V and 5V power supplies
- Stack oriented operand storage
- Direct memory access or programmed I/O Data Transfers
- End of execution signal
- Error interrupt
- All inputs and outputs TTL level compatible
- Advanced N-channel silicon gate MOS technology

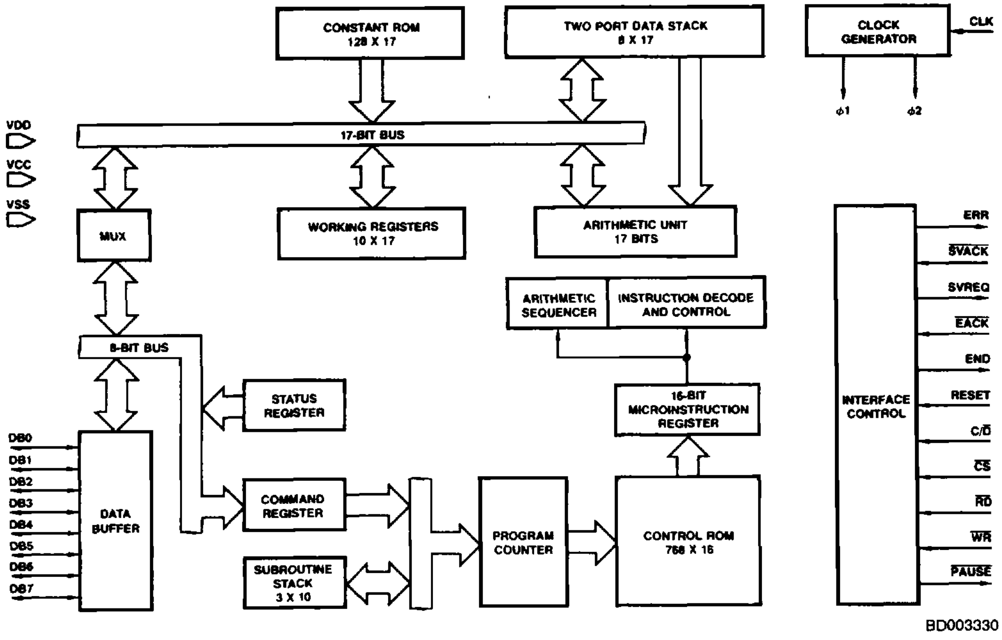
GENERAL DESCRIPTION

The Am9512 is a high performance floating-point processor unit (FPU). It provides single precision (32-bit) and double precision (64-bit) add, subtract, multiply and divide opertions. It can be easily interfaced to enhance the computational capabilities of the host microprocessor.

The operand, result, status and command information transfers take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack by the host processor, and a command is issued to perform an operation on the data stack. The results of this operation are available to the host processor by popping the stack.

Information transfers between the Am9512 and the host processor can be handled by using programmed I/O or direct memory access techniques. After completing an operation, the Am9512 activates an "end of execution" signal that can be used to interrupt the host processor.

BLOCK DIAGRAM



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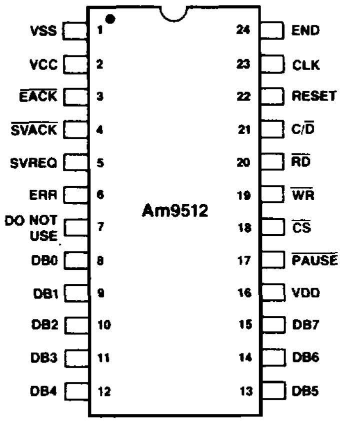
CONNECTION DIAGRAM
Top View

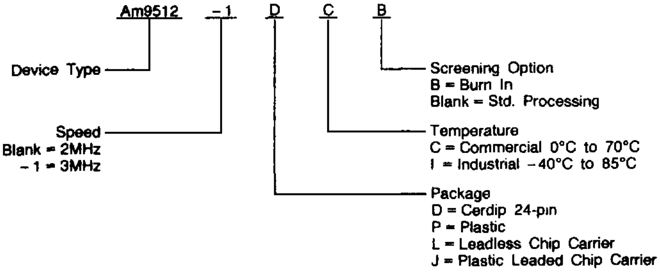


CD005160

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Am9512 -1 D C B

Device Type

Speed
Blank = 2MHz
-1 = 3MHz

Screening Option
B = Burn In
Blank = Std. Processing

Temperature
C = Commercial 0°C to 70°C
I = Industrial -40°C to 85°C

Package
D = Cerdip 24-pin
P = Plastic
L = Leadless Chip Carrier
J = Plastic Leaded Chip Carrier

Valid Combinations	
Am9512	DC, DCB, DI, DIB,
Am9512-1	LC, LCB, LI, LIB

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>23</td><td>CLK</td><td>I</td><td>(Clock). An external timing source connected to the CLK input provides the necessary clocking.</td></tr>
<tr><td>22</td><td>RESET</td><td>I</td><td>(Reset). A HIGH on this input causes initialization. Reset terminates any operation in progress, and clears the status register to zero. The internal stack pointer is initialized, and the contents of the stack may be affected. After a reset, the END output, the ERR output and the SVREQ output will be LOW. For proper initialization, RESET must be HIGH for at least five CLK periods following stable power supply voltages and stable clock.</td></tr>
<tr><td>21</td><td>C/$\overline{\text{D}}$</td><td>I</td><td>(Command/Data Select). The C/$\overline{\text{D}}$ input together with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs determines the type of transfer to be performed on the data bus as follows:
<table>
<tr><th>C/$\overline{\text{D}}$</th><th>$\overline{\text{RD}}$</th><th>$\overline{\text{WR}}$</th><th>Function</th></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Push data byte onto the stack</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Pop data byte from the stack</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>Enter command</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Read Status</td></tr>
<tr><td>X</td><td>L</td><td>L</td><td>Undefined</td></tr>
</table>
L = LOW
H = HIGH
X = DON'T CARE</td></tr>
<tr><td>24</td><td>END</td><td>O</td><td>(End of Execution). A HIGH on this output indicates that execution of the current command is complete. This output will be cleared LOW by activating the $\overline{\text{EACK}}$ input LOW or performing any read or write operation or device initialization using the RESET. If $\overline{\text{EACK}}$ is tied LOW, the END output will be a pulse (see $\overline{\text{EACK}}$ description).

Reading the status register while a command execution is in progress is allowed. However, any read or write operation clears the flip-flop that generates the END output. Thus, such continuous reading could conflict with internal logic setting of the END flip-flop at the end of command execution.</td></tr>
<tr><td>3</td><td>$\overline{\text{EACK}}$</td><td>I</td><td>(End Acknowledge). This input when LOW makes the END output go LOW. As mentioned earlier, HIGH on the END output signals completion of a command execution. The END signal is derived from an internal flip-flop which is clocked at the completion of a command. This flip-flop is clocked to the reset state when $\overline{\text{EACK}}$ is LOW. Consequently, if $\overline{\text{EACK}}$ is tied LOW, the END output will be a pulse that is approximately one CLK period wide.</td></tr>
<tr><td>5</td><td>SVREQ</td><td>O</td><td>(Service Request). A HIGH on this output indicates completion of a command. In this sense, this output is the same as the END output. However, the Service Bit in the Command Register determines whether the SVREQ output will go HIGH at the completion of a command. This bit must be 1 for SVREQ to go HIGH. The SVREQ can be cleared (i.e., go LOW) by activating the $\overline{\text{SVACK}}$ input LOW or initializing the device using the RESET. Also, the SVREQ will be automatically cleared after completion of any command that has the service request bit as 0.</td></tr>
<tr><td>4</td><td>$\overline{\text{SVACK}}$</td><td>I</td><td>(Service Acknowledge). A LOW on this input clears SVREQ. If the $\overline{\text{SVACK}}$ input is permanently tied LOW, it will conflict with the internal setting of the SVREQ output. Thus, the SVREQ indication cannot be relied upon if the $\overline{\text{SVACK}}$ is tied LOW.</td></tr>
<tr><td>8-15</td><td>DB0–DB7</td><td>I/O</td><td>(Data Bus). These eight bidirectional lines are used to transfer command, status and operand information between the device and the host processor. DB0 is the least significant and DB7 is the most significant bit position. HIGH on a data bus line corresponds to 1 and LOW corresponds to 0.

When pushing operands onto the stack using the data bus, the least significant byte must be pushed first and the most significant byte last. When popping the stack to read the result of an operation, the most significant byte will be available on the data bus first and the least significant byte will be the last. Moreover, for pushing operands and popping results, the number of transactions must be equal to the proper number of bytes appropriate for the chosen format. Otherwise, the internal byte pointer will not be aligned properly. The Am9512 single precision format requires 4 bytes, and double precision format requires 8 bytes.</td></tr>
<tr><td>6</td><td>ERR</td><td>O</td><td>(Error). This output goes HIGH to indicate that the current command execution resulted in an error condition. The error conditions are: attempt to divide by zero, exponent overflow and exponent underflow. The ERR output is cleared LOW on read status register operation or upon RESET.

The ERR output is derived from the error bits in the status register. These error bits will be updated internally at an appropriate time during a command execution. Thus, ERR output going HIGH may not correspond with the completion of a command. Reading of the status register can be performed while a command execution is in progress. However, it should be noted that reading the status register clears the ERR output. Thus, reading the status register while a command execution is in progress may result in an internal conflict with the ERR output.</td></tr>
<tr><td>18</td><td>$\overline{\text{CS}}$</td><td>I</td><td>(Chip Select). This input must be LOW to accomplish any read or write operation to the Am9512.

To perform a write operation, appropriate data is presented on DB0 through DB7 lines, appropriate logic level on the C/$\overline{\text{D}}$ input, and the $\overline{\text{CS}}$ input is made LOW. Whenever $\overline{\text{WR}}$ and $\overline{\text{RD}}$ inputs are both HIGH and $\overline{\text{CS}}$ is LOW, $\overline{\text{PAUSE}}$ goes LOW. However, actual writing into the Am9512 cannot start until $\overline{\text{WR}}$ is made LOW. After initiating the write operation by the HIGH-to-LOW transition on the $\overline{\text{WR}}$ input, the $\overline{\text{PAUSE}}$ output will go HIGH, indicating the write operation has been acknowledged. The $\overline{\text{WR}}$ input can go HIGH after $\overline{\text{PAUSE}}$ goes HIGH. The data lines, C/$\overline{\text{D}}$ input and the $\overline{\text{CS}}$ input can change when appropriate hold time requirements are satisfied. See Write Timing diagram for details.

To perform a read operation, an appropriate logic level is established on the C/$\overline{\text{D}}$ input and $\overline{\text{CS}}$ is made LOW. The $\overline{\text{PAUSE}}$ output goes LOW because $\overline{\text{WR}}$ and $\overline{\text{RD}}$ inputs are HIGH. The read operation does not start until the $\overline{\text{RD}}$ input goes LOW. $\overline{\text{PAUSE}}$ will go HIGH, indicating that the read operation is complete and the required information is available on the DB0 through DB7 lines. This information will remain on the data lines as long as $\overline{\text{RD}}$ is LOW. The $\overline{\text{RD}}$ input can return HIGH anytime after $\overline{\text{PAUSE}}$ goes HIGH. The $\overline{\text{CS}}$ input and C/$\overline{\text{D}}$ input can change anytime after $\overline{\text{RD}}$ returns HIGH. See Read Timing diagram for details. If the $\overline{\text{CS}}$ is tied LOW permanently, $\overline{\text{PAUSE}}$ will remain LOW until the next Am9512 read or write access.</td></tr>
</table>

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PIN DESCRIPTION (Cont.)

Pin No.	Name	I/O	Description
20	$\overline{RD}$	I	(Read). A LOW on this input is used to read information from an internal location and gate that information onto the data bus. The $\overline{CS}$ input must be LOW to accomplish the read operation. The C/$\overline{D}$ input determines what internal location is of interest. See C/$\overline{D}$, $\overline{CS}$ input descriptions and Read Timing diagram for details. If the END output was HIGH, performing any read operation will make the END output go LOW after the HIGH-to-LOW transition of the $\overline{RD}$ input (assuming $\overline{CS}$ is LOW). If the ERR output was HIGH, performing a status register read operation will make the ERR output LOW. This will happen after the HIGH-to-LOW transition of the RD input (assuming $\overline{CS}$ is LOW).
19	$\overline{WR}$	I	(Write). A LOW on this input is used to transfer information from the data bus into an internal location. The $\overline{CS}$ must be LOW to accomplish the write operation. The C/$\overline{D}$ determines which internal location is to be written. See C/$\overline{D}$, $\overline{CS}$ input descriptions and Write Timing diagram for details. If the END output was HIGH, performing any write operation will make the END output go LOW after the LOW-to-HIGH transition of the $\overline{WR}$ input (assuming $\overline{CS}$ is LOW).
17	$\overline{PAUSE}$	O	(Pause). This output is a handshake signal used while performing read or write transactions with the Am9512. If the $\overline{WR}$ and $\overline{RD}$ inputs are both HIGH, the $\overline{PAUSE}$ output goes LOW with the $\overline{CS}$ input in anticipation of a transaction. If $\overline{WR}$ goes LOW to initiate a write transaction with proper signals established on the DB0 - DB7, C/$\overline{D}$ inputs, the $\overline{PAUSE}$ will return HIGH, indicating that the write operation has been accomplished. The $\overline{WR}$ can be made HIGH after this event. On the other hand, if a read operation is desired, the $\overline{RD}$ input is made LOW after activating $\overline{CS}$ LOW and establishing proper C/$\overline{D}$ input. (The $\overline{PAUSE}$ will go LOW in response to $\overline{CS}$ going LOW.) The $\overline{PAUSE}$ will return HIGH indicating completion of read. The $\overline{RD}$ can return HIGH after this event. It should be noted that a read or write operation can be initiated without any regard to whether a command execution is in progress or not. Proper device operation is assured by obeying the $\overline{PAUSE}$ output indication as described.
2	V_{CC}		+5V Power Supply.
16	V_{DD}		+12V Power Supply.
1	V_{SS}		Ground.

DETAILED DESCRIPTION

Major functional units of the Am9512 are shown in the block diagram. The Am9512 employs a microprogram controlled stack oriented architecture with 17-bit wide data paths.

The Arithmetic Unit receives one of its operands from the Operand Stack. This stack is an eight word by 17-bit two port memory with last in - first out (LIFO) attributes. The second operand to the Arithmetic Unit is supplied by the internal 17-bit bus. In addition to supplying the second operand, this bidirectional bus also carries the results from the output of the Arithmetic Unit when required. Writing into the Operand Stack takes place from this internal 17-bit bus when required. Also, connected to this bus are the Constant ROM and Working Registers. The ROM provides the required constants to perform the mathematical operations while the Working Registers provide storage for the intermediate values during command execution.

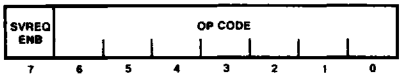
Communication between the external world and the Am9512 takes place on eight bidirectional input/output lines, DB0 through DB7 (Data Bus). These signals are gated to the internal 8-bit bus through appropriate interface and buffer circuitry. Multiplexing facilities exist for bidirectional communication between the internal eight and 17-bit buses. The Status Register and Command Register are also located on the 8-bit bus.

The Am9512 operations are controlled by the microprogram contained in the Control ROM. The Program Counter supplies the microprogram addresses and can be partially loaded from the Command Register. Associated with the Program Counter is the Subroutine Stack where return addresses are held during subroutine calls in the microprogram. The Microinstruction Register holds the current microinstruction being executed. The register facilitates pipelined microprogram execution. The Instruction Decode logic generates various internal control signals needed for the Am9512 operation.

The Interface Control logic receives several external inputs and provides handshake related outputs to facilitate interfacing the Am9512 to microprocessors.

Command Format

The Operation of the Am9512 is controlled from the host processor by issuing instructions called commands. The command format is shown below:



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The command consists of 8 bits; the least significant 7 bits specify the operation to be performed as detailed in the accompanying table. The most significant bit is the Service Request Enable bit. This bit must be a 1 if SVREQ is to go high at end of executing a command.

The Am9512 commands fall into three categories: single precision arithmetic, double precision arithmetic and data manipulation. There are four arithmetic operations that can be performed with single precision (32-bit) or double precision (64-bit) floating-point numbers: add, subtract, multiply and divide. These operations require two operands. The Am9512 assumes that these operands are located in the internal stack as Top of Stack (TOS) and Next on Stack (NOS). The result will always be returned to the previous NOS which becomes the new TOS. Results from an operation are of the same precision and format as the operands. The results will be rounded to preserve the accuracy. The actual data formats and rounding procedures are described in a later section. In addition to the arithmetic operations, the Am9512 implements eight data manipulating operations. These include changing the sign of a double or single precision operand located in TOS, exchanging single precision operands located at TOS and NOS, as well as copying and popping single or double precision operands. See also the sections on status register and operand formats.

The Execution times of the Am9512 commands are all data dependent. Table 2 shows one example of each command execution time.

Table 1. Command Decoding Table.

Command Bits									
7	6	5	4	3	2	1	0	Mnemonic	Description
X	0	0	0	0	0	0	1	SADD	Add TOS to NOS Single Precision and result to NOS. Pop stack.
X	0	0	0	0	0	1	0	SSUB	Subtract TOS from NOS Single Precision and result to NOS. Pop stack.
X	0	0	0	0	0	1	1	SMUL	Multiply NOS by TOS Single Precision and result to NOS. Pop stack.
X	0	0	0	0	1	0	0	SDIV	Divide NOS by TOS Single Precision and result to NOS. Pop stack.
X	0	0	0	0	1	0	1	CHSS	Change sign of TOS Single Precision operand.
X	0	0	0	0	1	1	0	PTOS	Push Single Precision operand on TOS to NOS.
X	0	0	0	0	1	1	1	POPS	Pop Single Precision operand from TOS. NOS becomes TOS.
X	0	0	0	1	0	0	0	XCHS	Exchange TOS with NOS Single Precision.
X	0	1	0	1	1	0	1	CHSD	Change sign of TOS Double Precision operand.
X	0	1	0	1	1	1	0	PTOD	Push Double Precision operand on TOS to NOS.
X	0	1	0	1	1	1	1	POPD	Pop Double Precision operand from TOS. NOS becomes TOS.
X	0	0	0	0	0	0	0	CLR	CLR status.
X	0	1	0	1	0	0	1	DADD	Add TOS to NOS Double Precision and result to NOS. Pop stack.
X	0	1	0	1	0	1	0	DSUB	Subtract TOS from NOS Double Precision and result to NOS. Pop Stack.
X	0	1	0	1	0	1	1	DMUL	Multiply NOS by TOS Double Precision and result to NOS. Pop Stack.
X	0	1	0	1	1	0	0	DDIV	Divide NOS by TOS Double Precision and result to NOS. Pop Stack.

Note: X = Don't Care Operation for bit combinations not listed above is undefined.

Table 2. Am9512 Execution Time in Cycles.

Single Precision			
	Min	Typ	Max
Add	58	220	512
Subtract	56	220	512
Multiply	192	220	254
Divide	228	240	264

Double Precision			
	Min	Typ	Max
Add	578	1200	3100
Subtract	578	1200	3100
Multiply	1720	1770	1860
Divide	4560	4920	5120

Note: Typical for add and subtract, assumes the operands are within six decimal orders of magnitude. Max is derived from the maximun execution time of 1000 executions with random 32-bit or 64-bit patterns.

Table 3. Some Execution Examples.

Command	TOS	NOS	Result	Clock periods
SADD	3F800000	3F800000	40000000	58
SSUB	3F800000	3F800000	00000000	56
SMUL	40400000	3FC00000	40900000	198
SDIV	40000000	3F800000	3F000000	228
CHSS	3F800000	–	BF800000	10
PTOS	3F800000	–	–	16
POPS	3F800000	–	–	14
XCHS	3F800000	4000000	–	26
CHSD	3FF0000000000000	–	BFF0000000000000	24
PTOD	3FF0000000000000	–	–	40
POPD	3FF0000000000000	–	–	26
CLR	3FF0000000000000	–	–	4
DADD	3FF00000A0000000	8000000000000000	3FF00000A0000000	578
DSUB	3FF00000A0000000	8000000000000000	3FF00000A0000000	578
DMUL	BFF0000000000000	3FF8000000000000	C002000000000000	1748
DDIV	BFF8000000000000	3FF8000000000000	BFF0000000000000	4560

Note: TOS, NOS and Result are in hexadecimal; Clock period is in decimal.

Command Initiation

After properly positioning the required operands in the stack, a command may be issued. The procedure for initiating a command execution is as follows:

1. Establish appropriate command on the DB0-DB7 lines.
2. Establish HIGH on the $C/\overline{D}$ input.
3. Establish LOW on the $\overline{CS}$ input. Whenever $\overline{WR}$ and $\overline{RD}$ inputs are HIGH, the PAUSE output follows the $\overline{CS}$ input. Hence, $\overline{PAUSE}$ will become LOW.
4. Establish LOW on the $\overline{WR}$ input after an appropriate set-up time (see Timing diagrams).
5. Sometime after the HIGH-to-LOW level transition of $\overline{WR}$ input, the $\overline{PAUSE}$ output will become HIGH to acknowledge the write operation. The $\overline{WR}$ input can return to HIGH anytime after $\overline{PAUSE}$ goes HIGH. The DB0-DB7, $C/\overline{D}$ and $\overline{CS}$ inputs are allowed to change after the hold time requirements are satisfied (see Timing diagram).

An attempt to issue a new command while the current command execution is in progress is allowed. Under these circumstances, the $\overline{PAUSE}$ output will not go HIGH until the current command execution is completed.

Operand Entry

The Am9512 commands operate on the operands located at the TOS and NOS, and results are returned to the stack at NOS and then popped to TOS. The operands required for the Am9512 are one of two formats – single precision floating-point (4 bytes) or double precision floating-point (8 bytes). The result of an operation has the same format as the operands. In other words, operations using single precision quantities always result in a single precision result, while operations involving double precision quantities will result in double precision result.

Operands are always entered into the stack least significant byte first and most significant byte last. The following procedure must be followed to enter operands into the stack:

1. The lower significant operand byte is established on the DB0-DB7 lines.
2. A LOW is established on the $C/\overline{D}$ input to specify that data is to be entered into the stack.
3. The $\overline{CS}$ input is made LOW. Whenever the $\overline{WR}$ and $\overline{RD}$ inputs are HIGH, the $\overline{PAUSE}$ output will follow the $\overline{CS}$ input. Thus $\overline{PAUSE}$ output will become LOW.
4. After appropriate set-up time (see Timing diagrams), the $\overline{WR}$ input is made LOW.
5. After this event, $\overline{PAUSE}$ will return HIGH to indicate that the write operation has been acknowledged.
6. Anytime after the $\overline{PAUSE}$ output goes HIGH, the $\overline{WR}$ input can be made HIGH. The DB0-DB7, $C/\overline{D}$ and $\overline{CS}$ inputs can change after appropriate hold time requirements are satisfied (see Timing diagrams).

The above procedure must be repeated until all bytes of the operand are pushed onto the stack. It should be noted that for single precision operands 4 bytes should be pushed and 8 bytes must be pushed for double precision. Not pushing all the bytes of a quantity will result in byte pointer misalignment.

The Am9512 stack can accomodate 4 single precision quantities or 2 double precision quantities. Pushing more quantities than the capacity of the stack will result in loss of data, which is usual with any LIFO stack.

Removing the Results

Result from an operation will be available at the TOS. Results can be transferred from the stack to the data bus by reading the stack. When the stack is popped for results, the most significant byte is available first and the least significant byte last. A result is always of the same precision as the operands that produced it. Thus, when the result is taken from the stack, the total number of bytes popped out should be appropriate with the precision – single precision results are 4 bytes and double precision results are 8 bytes. The following procedure must be used for reading the result from the stack:

1. A LOW is established on the $C/\overline{D}$ input.
2. The $\overline{CS}$ input is made LOW. When $\overline{WR}$ and $\overline{RD}$ inputs are both HIGH, the $\overline{PAUSE}$ output follows the $\overline{CS}$ input, thus $\overline{PAUSE}$ will be LOW.
3. After appropriate set-up time (see Timing diagrams), the $\overline{RD}$ input is made LOW.
4. Sometime after this, $\overline{PAUSE}$ will return HIGH, indicating that the data is available on the DB0-DB7 lines. This data will remain on the DB0-DB7 lines. This data will remain on the DB0-DB7 lines as long as the $\overline{RD}$ input remains LOW.
5. Anytime after $\overline{PAUSE}$ goes HIGH, the $\overline{RD}$ input can return HIGH to complete transaction.
6. The $\overline{CS}$ and $C/\overline{D}$ inputs can change after appropriate hold time requirements are satisfied (see Timing diagram).
7. Repeat this procedure until all bytes appropriate for the precision of the result are popped out.

Reading of the stack does not alter its data; it only adjusts the byte pointer. If more data is popped than the capacity of the stack, the internal byte pointer will wrap around and older data will be read again, consistent with the LIFO stack.

Reading Status Register

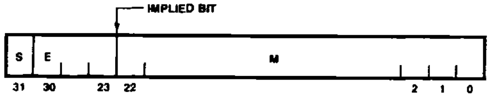
The Am9512 status register can be read without any regard to whether a command is in progress or not. The only implication that has to be considered is the effect this might have on the END and ERR outputs discussed in the signal descriptions.

The following procedure must be followed to accomplish status register reading:

1. Establish HIGH on the $C/\overline{D}$ input.
2. Establish LOW on the $\overline{CS}$ input. Whenever $\overline{WR}$ and $\overline{RD}$ inputs are HIGH, $\overline{PAUSE}$ will follow the $\overline{CS}$ input. Thus, $\overline{PAUSE}$ will go LOW.
3. After appropriate set-up time (see Timing diagram) $\overline{RD}$ is made LOW.
4. Sometime after the HIGH-to-LOW transition of $\overline{RD}$, $\overline{PAUSE}$ will become HIGH, indicating that status register contents are available on the DB0-DB7 lines. These lines will contain this information as long as $\overline{RD}$ is LOW.
5. The $\overline{RD}$ input can be returned HIGH anytime after $\overline{PAUSE}$ goes HIGH.
6. The $C/\overline{D}$ input and $\overline{CS}$ input can change after satisfying approprite hold time requirements (see Timing diagram).

Data Formats

The Am9512 handles floating-point quantities in two different formats – single precision and double precision. The single precision quantities are 32-bits long as shown below.



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Bit 31:
S = Sign of the mantissa. 1 represents negative and 0 represents positive.

Bits 23-30
E = These 8-bits represent a biased exponent. The bias is $2^7 - 1 = 127$.

Bits 0-22
M = 23-bit mantissa. Together with the sign bit, the mantissa represents a signed fraction in sign-magitude notation. There is an implied 1 beyond the most significant bit (bit 22) of the mantissa. In other words, the mantissa is assumed to be a 24-bit normalized quantity, and the most significant bit, which will always be 1 due to normalization, is implied. The Am9512 restores this implied bit internally before performing arithmetic, normalizes the result, and strips the implied bit before returning the results to the external data bus. The binary point is between the implied bit and bit 22 of the mantissa.

The quantity N represented by the above notation is:

$$N = (-1)^S\ \overset{\text{Bias}}{2^{E-(2^7-1)}}\ \overset{\text{Binary Point}}{(1.M)}$$

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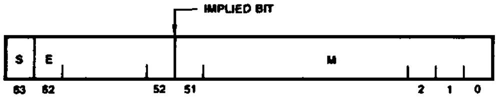
Provided E ≠ 0 or all 1's.

A double precision quantity consists of the mantissa sign bit(s), an 11-bit biased exponent (E), and a 52-bit mantissa (M). The bias for double precision quantities is $2^{10} - 1$. The double precision format is illustrated below.



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Bit 63:
S = Sign of the mantissa. 1 represents negative and 0 represents positive.

Bits 52-62
E = These 11 bits represent a biased exponent. The bias is $2^{10} - 1 = 1023$.

Bit 0-51
M = 52-bit mantissa. Together with the sign bit, the mantissa represents a signed fraction in sign-magnitude notation. There is an implied 1 beyond the most significant bit (bit 51) of the mantissa. In other words, the mantissa is assumed to be a 53-bit normalized quantity, and the most significant bit, which will always be a 1 due to normalization, is implied. The Am9512 restores this implied bit internally before performing arithmetic, normalizes the result, and strips the implied bit before returning the result to the external data bus. The binary point is between the implied bit and bit 51 of the mantissa.

The quantity N represented by the above notation is:

$$N = (-1)^S\ \overset{\text{Bias}}{2^{E-(2^{10}-1)}}\ \overset{\text{Binary point}}{(1.M)}$$

TB000009

Provided E ≠ 0 or all 1's.

Status Register

The Am9512 contains an 8-bit status register with the following format.

BUSY	SIGN S	ZERO Z	RESERVED	DIVIDE EXCEPTION D	EXPONENT UNDERFLOW U	EXPONENT OVERFLOW V	RESERVED
7	6	5	4	3	2	1	0

DF001350

Bit 0 and bit 4 are reserved. Occurrence of exponent overflow (V), exponent underflow (U) and divide exception (D) are indicated by bits 1, 2 and 3 respectively. An attempt to divide by zero is the only divide exception. Bits 5 and 6 represent a zero result and the sign of a result respectively. Bit 7 (Busy) of the status register indicates if the Am9512 is currently busy executing a command. All the bits are initialized to zero upon reset. Also, executing a CLR (Clear Satus) command will result in all zero status register bits. A zero in Bit 7 indicates that the Am9512 is not busy and a new command may be initiated. As soon as a new command is issued, Bit 7 becomes 1 to indicate the device is busy and remains 1 until the command execution is complete – at which time it will become 0. As soon as a new command is issued, status register bits 0, 1, 2, 3, 4, 5 and 6 are cleared to zero. The status bits will be set as required during the command execution. Hence, as long as bit 7 is 1, the remainder of the status register bit indications should not be relied upon unless the ERR occurs. The following is a detailed bit description.

Bit 0 Reserved

Bit 1 Exponent Overflow (V): When 1, this bit indicates that exponent overflow has occurred. Cleared to zero otherwise.

Bit 2 Exponent Underflow (U): When 1, this bit indicates that exponent underflow has occurred. Cleared to zero otherwise.

Bit 3 Divide Exception (D): When 1, this bit indicates that an attempt to divide by zero is made. Cleared to zero otherwise.

Bit 4 Reserved

Bit 5 Zero (Z): When 1, this bit indicates that the result returned to TOS after a command is all zeros. Cleared to zero otherwise.

Bit 6 Sign (S): When 1, this bit indicates that the result returned to TOS is negative. Cleared to zero otherwise.

Bit 7 Busy: When 1, this bit indicates the Am9512 is in the process of executing a command. It will become zero after the command execution is complete.

All other status register bits are valid when the Busy bit is zero.

Algorithms of Floating-Point Arithmetic

1. Floating-Point to Decimal Conversion

As an introduction to floating-point arithmetic, a brief description of the Decimal equivalent of the Am9512 floating-point format should help the reader to understand and verify the validity of the arithmetic operations. The Am9512 single precision format is used for the following discussions. With a minor modification of the field lengths, the discussion would also apply to the double precision format.

There are three parts in a floating-point number:

a. The sign – the sign applies to the sign of the number. Zero means the number is positive or zero. One means the number is negative.

b. The exponent – the exponent represents the magnitude of the number. The Am9512 single precision format has an excess 127_{10} notation, which means the code representation is 127_{10} higher than the actual value. The following are a few examples of actual versus coded exponent.

Actual	Coded
$+127_{10}$	$+254_{10}$
0	127_{10}
-126_{10}	$+1_{10}$

c. The mantissa – the mantissa is a 23-bit value with the binary point to the left of the most significant bit. There is a hidden 1 to the left of the binary point so the mantissa is always less than 2 and greater than or equal to 1.
To find the Decimal equivalent of the floating-point number, the mantissa is multiplied by 2 to the power of the actual exponent. The number is negated if the sign bit = 1. The following are two examples of conversion:

Example 1

Floating Point No. = 0 1 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 B

Sign   Exponent   Mantissa

TB000010

Coded Exponent = 1 0 0 0 0 0 1 1 B
Actual Exponent = 1 0 0 0 0 0 1 1 B – 0 1 1 1 1 1 1 1 B = 0 0 0 0 0 1 0 0 B = 4_{10}
Mantissa = 1.1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 B
= 1 + ½ + ¼ = 1.75_{10}
Decimal No. = 2^4 x 1.75 = 16 x 1.75 = 28_{10}

Example 2

Floating Point No. = 1 0 1 1 1 1 0 1 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 B

Sign   Exponent   Mantissa

TB000011

Coded Exponent = 0 1 1 1 1 0 1 0 B
Actual Exponent = 0 1 1 1 1 0 1 0 B – 0 1 1 1 1 1 1 1 B = 1 1 1 1 1 0 1 1 B = -5_{10}
Mantissa = 1.0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 B
= 1 + ¼ + ⅛ = 1.375_{10}
Decimal No. = -2^{-5} x 1.375 = $-.04296875_{10}$

2. Unpacking of the Floating-Point Numbers
The Am9512 unpacks the floating-point number into three parts before any of the arithmetic operation. The number is divided into three parts as described in Section 1. The sign and expondent are copied from the original number as 1-bit and 8-bit numbers, respectively. The mantissa is stored as a 24-bit number. The least significant 23 bits are copied from the original number and the MSB is set to 1. The binary point is asumed to the right of the MSB.

The abbreviations listed below are used in the following sections of algorithm description:

SIGN – Sign of Result
EXP – Exponent of Result
MAN – Mantissa of Result
SIGN (TOS) – Sign of Top of Stack
EXP (TOS) – Exponent of Top of Stack
MAN (TOS) – Mantissa of Top of Stack
SIGN (NOS) – Sign of Next on Stack
EXP (NOS) – Exponent of Next on Stack
MAN (NOS) – Mantissa of Next on Stack

3. Floating-Point Add/Subtract
The floating-point add and subtract essentially use the same algorithm. The only difference is that floating-point subtract changes the sign of the floating-point number at top of stack and then performs the floating-point add.

The following is a step-by-step description of a floating-point add algorithm (Figure 1):

a. Unpack TOS and NOS.

b. The exponent of TOS is compared to the exponent of NOS.

c. If the exponents are equal, go to step f.

d. Right shift the mantissa of the number with the smaller exponent.

e. Increment the smaller exponent and go to step b.

f. Set sign of result to sign of larger number.

g. Set exponent of result to exponent of larger number.

h. If sign of the two numbers are not equal, go to m.

i. Add Mantissas.

j. Right shift resultant mantissa by 1 and increment exponent of result by 1.

k. If MSB of exponent changes from 1 to 0 as a result of the increment, set overflow status.

l. Round if necessary and exit.

m. Subtract smaller mantissa from larger mantissa.

n. Left shift mantissa and decrement exponent of result.

o. If MSB of exponent changes from 0 to 1 as a result of the decrement, set underflow status and exit.

p. If the MSB of the resultant mantissa = 0, go to n.

q. Round if necessary and exit.

4. Floating-Point Multiply
Floating-point multiply basically involves the addition of the exponents and multiplication of the mantissas. The following is a step-by-step description of a floating multiplication algorithm (Figure 2):

a. Check if TOS or NOS = 0.

b. If either TOS or NOS = 0, set result to 0 and exit.

c. Unpack TOS and NOS.

d. Convert EXP (TOS) and EXP (NOS) to unbiased form.
EXP (TOS) = EXP (TOS) – 127_{10}
EXP (NOS) = EXP (NOS) – 127_{10}

e. Add exponents.
EXP = EXP (TOS) + EXP (NOS)

f. If MSB of EXP (TOS) = MSB of EXP (NOS) = 0 and MSB of EXP = 1, then set overflow status and exit.

g. If MSB of EXP (TOS) = MSB of EXP (NOS) = 1 and MSB of EXP = 0, then set underflow status and exit.

h. Convert Exponent back to biased form.
EXP = EXP + 127_{10}

i. If sign of TOS = sign of NOS, set sign of result to 0, else set sign of result to 1.

j. Multiply mantissa.

k. If MSB of resultant = 1, right shift mantissa by 1 and increment exponent of resultant.

l. If MSB of exponent changes from 1 to 0 as a result of the increment, set overflow status.

m. Round if necessary and exit.

5. Floating-Point Divide
The floating-point divide basically involves the subtraction of exponents and the division of mantissas. The following is a step-by-step description of a division algorithm (Figure 3).

a. If TOS = 0, set divide exception error and exit.

b. If NOS = 0, set result to 0 and exit.

c. Unpack TOS and NOS.

d. Convert EXP (TOS) and EXP (NOS) to unbiased form.
EXP (TOS) = EXP(TOS) - 127_{10}
EXP (NOS) = EXP (NOS) - 127_{10}

e. Subtract exponent of TOS from exponent of NOS.
EXP = EXP (NOS) - EXP (TOS)

f. If MSB of EXP (NOS) = 0, MSB of EXP (TOS) = 1 and MSB of EXP = 1, then set overflow status and exit.

g. If MSB of EXP (NOS) = 1, MSB of EXP (TOS) = 0, and MSB of EXP = 0, then set underflow status and exit.

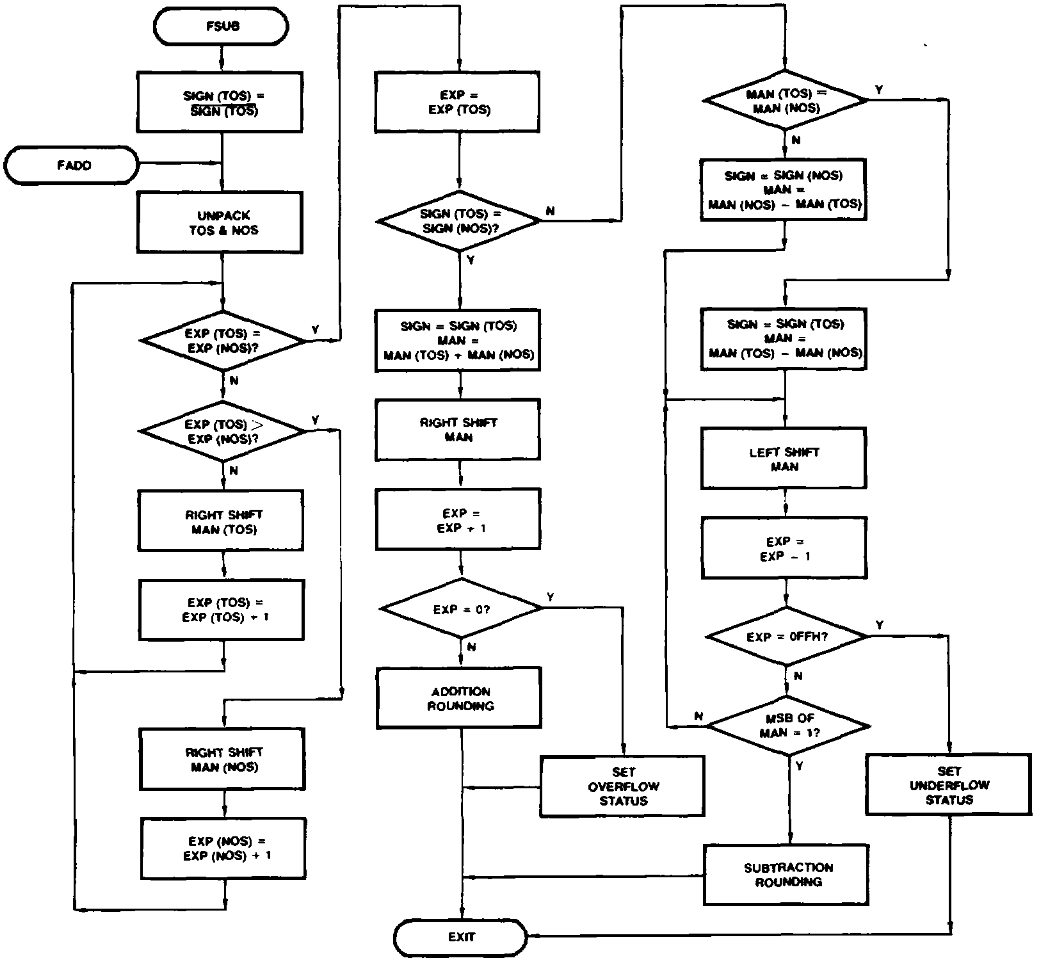


Figure 1. Conceptual Floating-Point Addition/Subtraction

h. Add bias to exponent of result.
EXP = EXP + 127_{10}

i. If sign of TOS = sign of NOS, set sign of result to 0, else set sign of result to 1.

j. Divide mantissa of NOS by mantissa of TOS.

k. If MSB = 0, left shift mantissa and decrement exponent of resultant, else go to n.

l. If MSB of exponent changes from 0 to 1 as a result of the decrement, set underflow status.

m. Go to k.

n. Round if necessary and exit.

The algorithms described above provide the user a means of verifying the validity of the result. They do not necessarily reflect the exact internal sequence of the Am9512.

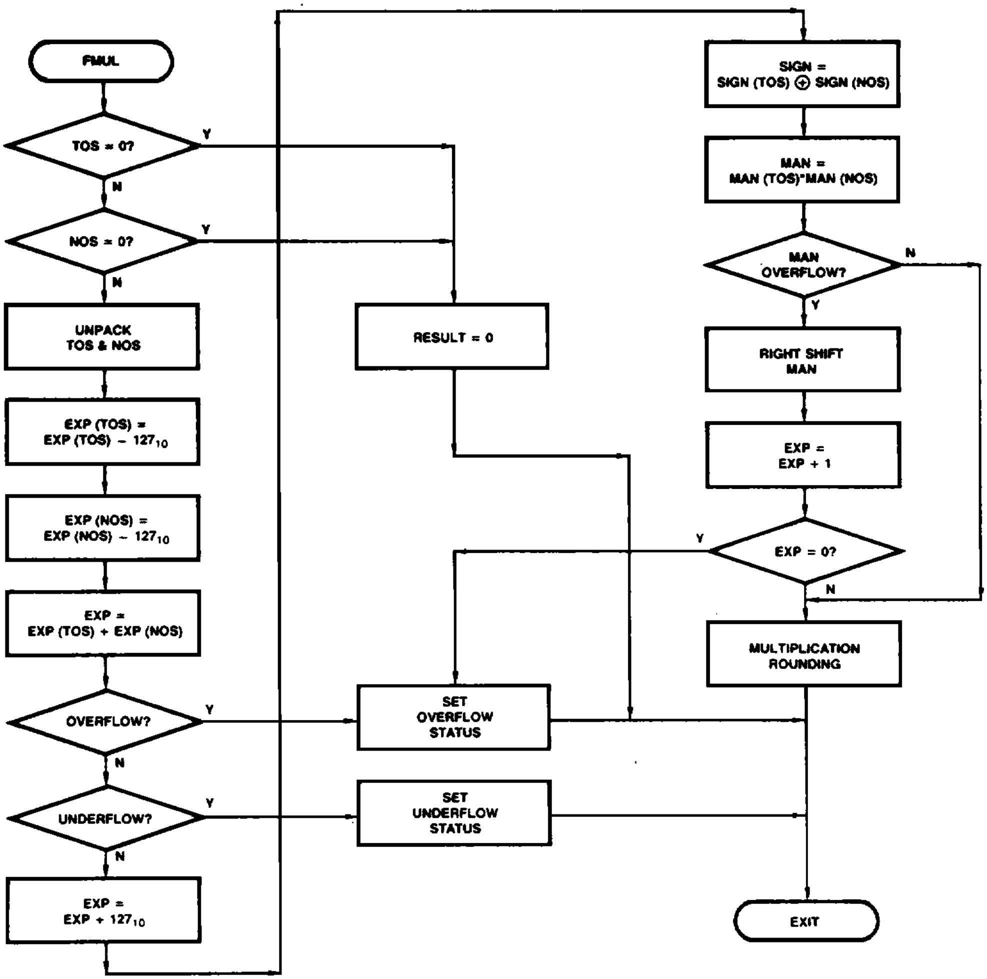
6. Rounding
   The Am9512 adopts a rounding algorithm that is consistent with the Intel® standard for floating-point arithmetic. The following description is an excerpt from the paper published in the proceedings of Compsac 77, November 1977, pp. 107-112 by Dr. John F. Palmer of Intel Corporation.

The method used for doing the rounding during floating-point arithmetic is known as "Round to Even"; i.e., if the resultant number is exactly halfway between two floating-point numbers, the number is rounded to the nearest floating-point number whose LSB of the mantissa is 0. To simplify the explanation, the algorithms will be illustrated with 4-bit arithmetic. The existence of an accumulator will be assumed as shown:

OF	B1	B2	B3	B4	G	R	ST

The bit labels denote:

OF – The overflow bit
B1-B4 – The 4 mantissa bits
G – The Guard bit
R – The Rounding bit
ST – The "Sticky" bit



PF001210

Figure 2. Conceptual Floating-Point Multiplication

The Sticky bit is set to one if any ones are shifted right of the rounding bit in the process of denormalization. If the Sticky bit becomes set, it remains set throughtout the operation. All shifting in the Accumulator involves the OF, G, R and ST bits. The ST bit is not affected by left shifts, but zeros are introduced into OF by right shifts.

Rounding during addition of magnitudes – add 1 to the G position, then if G = R = ST = 0, set B4 to 0 ("Rounding to Even").

Rounding during subtraction of magnitudes – if more than one left shift was performed, no rounding is needed; otherwise, round the same way as addition of magnitudes.

Rounding during multiplication – let the normalized double length product be:

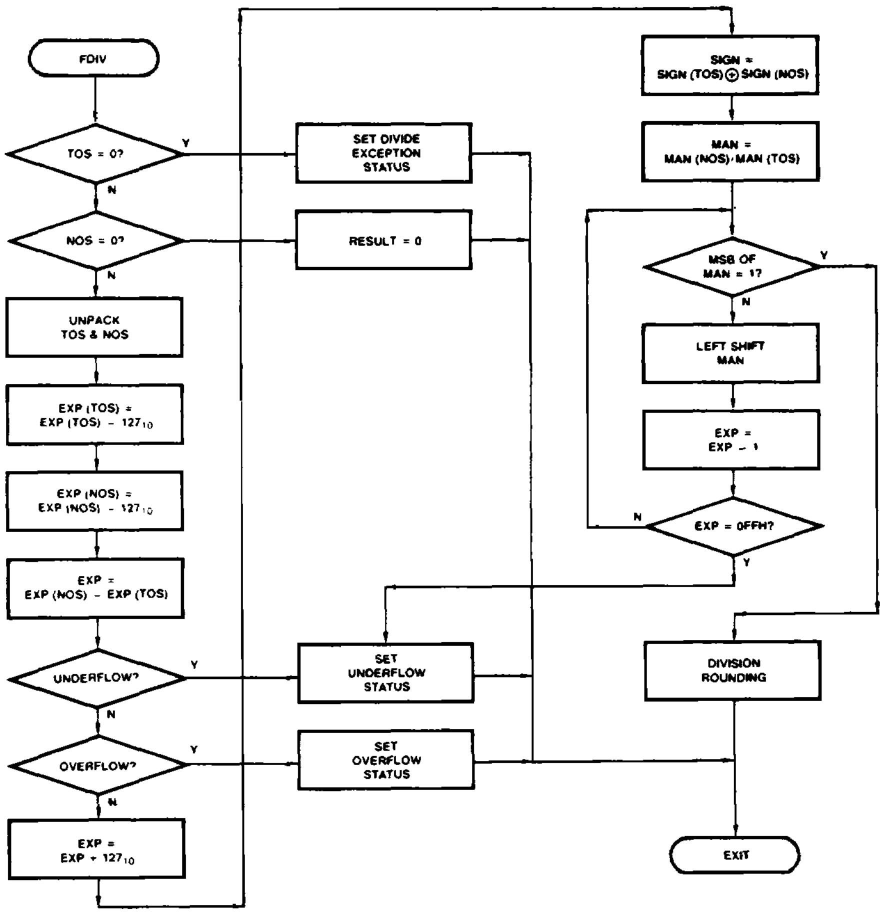
B1	B2	B3	B4	B5	B6	B7	B8

Then G = B5, R = B6, ST = B7 V B8. The rounding is then performed as in addition of magnitudes.

Rounding during division – let the first six bits of the normalized quotient be:

B1	B2	B3	B4	B5	B6

Then G = B5, R = B6, ST = 0 if and only if remainder = 0. The rounding is then performed as in addition of magnitudes.



PF001220

Figure 3. Conceptual Floating-Point Division

CHSD

CHANGE SIGN DOUBLE PRECISION

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	1	0	1	1	0	1

Hex Coding: AD IF SRE = 1
2D IF SRE = 0

Execution Time: See Table 2

Description:
The sign of the double precision TOS operand A is complemented. The double precision result R is returned to TOS. If the double precision operand A is zero, then the sign is not affected. The status bits S and Z indicate the sign of the result and if the result is zero. The status bits U, V and D are always cleared to zero.

Status Affected: S, Z. (U, V, D always zero.)

STACK CONTENTS

BEFORE		AFTER
A	TOS	R
B	NOS	B

TB000067

CHSS

CHANGE SIGN SINGLE PRECISION

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	0	1	0	1

Hex Coding: 85 IF SRE = 1
05 IF SRE = 0

Execution Time: See Table 2

Description:
The sign of the single precision operand A at TOS is complemented. The single precision result R is returned to TOS. If the exponent field of A is zero, all bits of R will be zeros. The status bits S and Z indicate the sign of the result and if the result is zero. The status bits U, V and D are cleared to zero.

Status Affected: S, Z. (U, V, D always zero.)

STACK CONTENTS

BEFORE		AFTER
A	← TOS →	R
B	← NOS →	B
C		C
D		D

TB000068

CLR

CLEAR STATUS

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	0	0	0	0

Hex Coding: 80 IF SRE = 1
00 IF SRE = 0

Execution Time: 4 clock cycles

Description:
The status bits S, Z, D, U, V are cleared to zero. The stack is not affected. This essentially is a no operation command as far as operands are concerned.

Status Affected: S, Z, D, U, V always zero.

DADD

DOUBLE PRECISION FLOATING-POINT ADD

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	1	0	1	0	0	1

Hex Coding: A9 IF SRE = 1
29 IF SRE = 0

Execution Time: See Table 2

Description:
The double precision operand A from TOS is added to the double precision operand B from NOS. The result is rounded to obtain the final double precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow, and exponent overflow, respectively. The status bit D will be cleared to zero.

Status Affected: S, Z, U, V. (D always zero.)

STACK CONTENTS

BEFORE		AFTER
A	← TOS →	R
B	← NOS →	Undefined

TB000069

DSUB

DOUBLE PRECISION FLOATING-POINT SUBTRACT

Binary Coding:

7	6	5	4	3	2	1	0
SRE	0	1	0	1	0	1	0

Hex Coding: AA IF SRE = 1
2A IF SRE = 0

Execution Time: See Table 2

Description:
The double precision operand A at TOS is subtracted from the double precision operand B at NOS. The result is rounded to obtain the final double precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow, respectively. The status bit D will be cleared to zero.

Status Affected: S, Z, U, V. (D always zero.)

STACK CONTENTS

BEFORE		AFTER
A	← TOS →	R
B	← NOS →	Undefined

TB000069

DDIV

DOUBLE PRECISION FLOATING-POINT DIVIDE

Binary Coding:

7	6	5	4	3	2	1	0
SRE	0	1	0	1	1	0	0

Hex Coding: AC IF SRE = 1
2C IF SRE = 0

Execution Time: See Table 2

Description:
The double precision operand B from NOS is divided by the double precision operand A from TOS. The result (quotient) is rounded to obtain the final double precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, attempt to divide by zero, exponent underflow and exponent overflow, respectively.

Status Affected: S, Z, D, U, V.

STACK CONTENT

BEFORE		AFTER
A	← TOS →	R (see note)
B	← NOS →	Undefined

TB000072

Note: If A is zero, the R = B (Divide exception).

DMUL

DOUBLE PRECISION FLOATING-POINT MULTIPLY

Binary Coding:

7	6	5	4	3	2	1	0
SRE	0	1	0	1	0	1	1

Hex Coding: AB IF SRE = 1
2B IF SRE = 0

Execution Time: See Table 2

Description:
The double precision operand A from TOS is multiplied by the double precision operand B from NOS. The result is rounded to obtain the final double precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow, respectively. The status bit D will be cleared to zero.

Status Affected: S, Z, U, V. (D always zero.)

STACK CONTENTS

BEFORE		AFTER
A	← TOS →	R
B	← NOS →	Undefined

TB000069

SADD

SINGLE PRECISION FLOATING-POINT ADD

Binary Coding:

7	6	5	4	3	2	1	0
SRE	0	0	0	0	0	0	1

Hex Coding: 81 IF SRE = 1
01 IF SRE = 0

Execution Time: See Table 2

Description:
The single precision operand A from TOS is added to the single precision operand B from NOS. The result is rounded to obtain the final single precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow, respectively. The status bit D will be cleared to zero.

Status Affected: S, Z, U, V. (D always zero.)

STACK CONTENT

BEFORE		AFTER
A	← TOS →	R
B	← NOS →	C
C		D
D		Undefined

TB000074

SSUB

SINGLE PRECISION FLOATING-POINT SUBTRACT

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	0	0	1	0

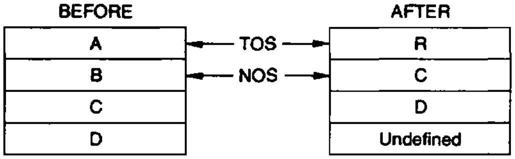
Hex Coding: 82 IF SRE = 1
02 IF SRE = 0

Execution Time: See Table 2

Description:
The single precision operand A at TOS is subtracted from the single precision operand B at NOS. The result is rounded to obtain the final single precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow, respectively. The status bit D will be cleared to zero.

Status Affected: S, Z, U, V. (D always zero.)

STACK CONTENTS



TB000073

SMUL

SINGLE PRECISION FLOATING-POINT MULTIPLY

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	0	0	1	1

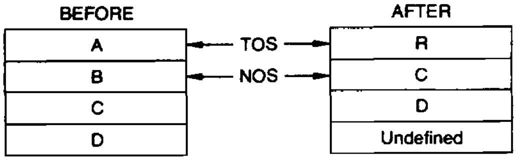
Hex Coding: 83 IF SRE = 1
03 IF SRE = 0

Execution Time: See Table 2

Description:
The single precision operand A from TOS is multiplied by the single precision operand B from NOS. The result is rounded to obtain the final single precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow, respectively. The status bit D will be cleared to zero.

Status Affected: S, Z, U, V. (D always zero.)

STACK CONTENTS



TB000075

SDIV

SINGLE PRECISION FLOATING-POINT DIVIDE

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	0	1	0	0

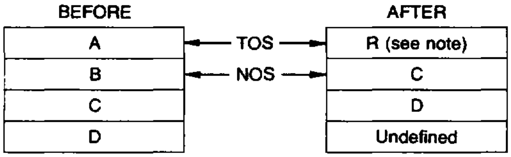
Hex Coding: 84 IF SRE = 1
04 IF SRE = 0

Execution Time: See Table 2

Description:
The single precision operand B from NOS is divided by the single precision operand A from TOS. The result (quotient) is rounded to obtain the final result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, attempt to divide by zero, exponent underflow and exponent overflow, respectively.

Status Affected: S, Z, D, U, V

STACK CONTENTS



TB000076

Note: If exponent field of A is zero, then R = B (Divide exception).

POPS

POP STACK SINGLE PRECISION

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	0	1	1	1

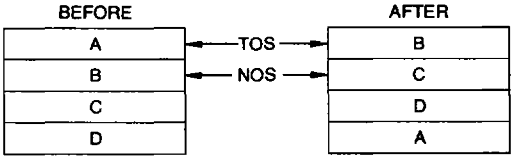
Hex Coding: 87 IF SRE = 1
07 IF SRE = 0

Execution Time: See Table 2

Description:
The single precision operand A is popped from the stack. The internal stack control mechanism is such that A will be written at the bottom of the stack. The status bits S and Z are affected to report the sign of the new operand at TOS and if it is zero, respectively. The status bits U, V and D will be cleared to zero. Note that only the exponent field of the new TOS is checked for zero; if it is zero, status bit Z will set to 1.

Status Affected: S, Z. (U, V, D always zero.)

STACK CONTENTS



TB000078

PTOD

PUSH STACK DOUBLE PRECISION

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	1	0	1	1	1	0

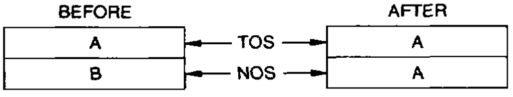
Hex Coding: AE IF SRE = 1
2E IF SRE = 0

Execution Time: See Table 2

Description:
The double precision operand A from the TOS is pushed back onto the stack. This is effectively a duplication of A into two consecutive stack locations. The status bits S and Z are affected to report the sign of the new TOS and if the new TOS is zero, respectively. The status bits U, V and D will be cleared to zero.

Status Affected: S, Z. (U, V, D always zero.)

STACK CONTENTS



TB000077

PTOS

PUSH STACK SINGLE PRECISION

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	0	1	1	0

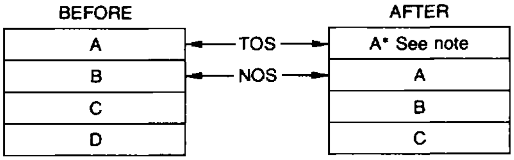
Hex Coding: 86 IF SRE = 1
06 IF SRE = 0

Execution Time: See Table 2

Description:
This instruction effectively pushes the single precision operand from TOS onto the stack. This amounts to duplicating the operand at two locations in the stack. However, if the operand at TOS prior to the PTOS command has only its exponent field as zero, the new content of the TOS will all be zeroes. The contents of NOS will be an exact copy of the old TOS. The status bits S and Z are affected to report the sign of the new TOS and if the content of TOS is zero, respectively. The status bits U, V and D will be cleared to zero.

Status Affected: S, Z. (U, V, D always zero.)

STACK CONTENTS



TB000079

Note: A* = A if Exponent field of A is not zero.
A* = 0 if Exponent field of A is zero.

POPD

POP STACK DOUBLE PRECISION

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	1	0	1	1	1	1

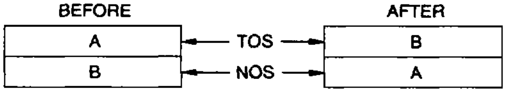
Hex Coding: AF IF SRE = 1
2F IF SRE = 0

Execution Time: See Table 2

Description:
The double precision operand A is popped from the stack. The internal stack control mechanism is such that A will be written at the bottom of the stack. This operation has the same effect as exchanging TOS and NOS. The status bits S and Z are affected to report the sign of the new operand at TOS and if it is zero, respectively. The status bits U, V and D will be cleared to zero.

Status Affected: S, Z. (U, V and D always zero.)

STACK CONTENTS



TB000080

XCHS

EXCHANGE TOS AND NOS SINGLE-PRECISION

	7	6	5	4	3	2	1	0
Binary Coding:	SRE	0	0	0	1	0	0	0

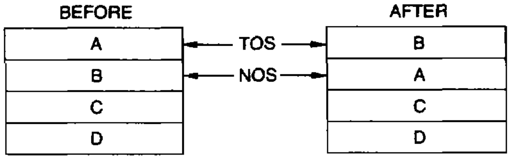
Hex Coding: 88 IF SRE = 1
08 IF SRE = 0

Execution Time: See Table 2

Description:
The single precision operand A from TOS and the single precision operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All other operands are unchanged.

Status Affected: S, Z. (U, V, and D always zero.)

STACK CONTENTS



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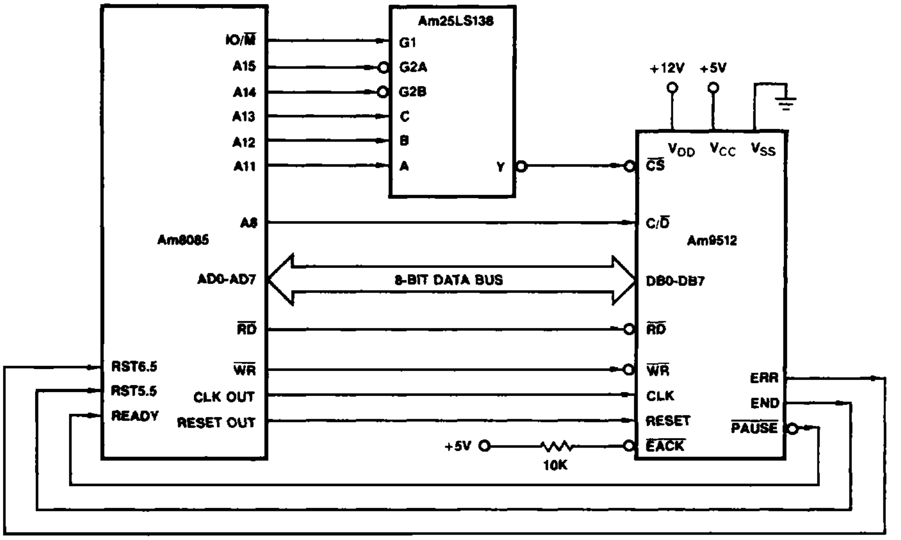

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Figure 4. Am9512 to Am8085 Interface

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
VDD with Respect to VSS .... −0.5 to +15.0V
VCC with Respect to VSS .... −0.5 to +7.0V
All Signal Voltages
with Respect to VSS .... −0.5 to +7.0V
Power Dissipitation (Package Limitation) 2.0W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

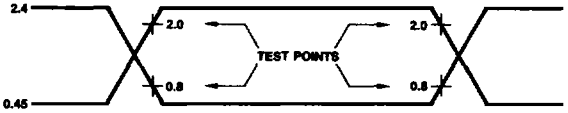
Grade	T_A	V_{CC}	V_{SS}
Commercial	0°C to 70°C	5.0V ±5%	0V
Industrial	−40°C to 85°C	5.0V ±10%	0V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions	Min	Typ	Max	Units
VOH	Output HIGH Voltage	IOH = −200μA	3.7			Volts
VOL	Output LOW Voltage	IOL = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage		2.0		VCC	Volts
VIL	Input LOW Voltage		−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC			±10	μA
IOZ	Data Bus Leakage	VO = 0.4V			10	μA
		VO = VCC			10	
ICC	VCC Supply Current	T_A = +25°C		50	90	mA
		T_A = 0°C			95	
IDD	VDD Supply Current	T_A = +25°C		50	90	mA
		T_A = 0°C			95	
CO	Output Capacitance	f_C = 1.0MHz, Inputs = 0V		8	10	pF
CI	Input Capacitance			5	8	pF
CIO	I/O Capacitance			10	12	pF

SWITCHING TEST INPUT/OUTPUT WAVEFORM



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Refer to page 7-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameters	Description		Am9512		Am9512-1		Units
			Min	Max	Min	Max	
TAPW	$\overline{\text{EACK}}$ LOW Pulse Width		100		75		ns
TCDR	C/$\overline{\text{D}}$ to $\overline{\text{RD}}$ LOW Set-up Time		0		0		ns
TCDW	C/$\overline{\text{D}}$ to $\overline{\text{WR}}$ LOW Set-up Time		0		0		ns
TCPH	Clock Pulse HIGH Width		200	500	140	500	ns
TCPL	Clock Pulse LOW Width		240		160		ns
TCSP	$\overline{\text{CS}}$ LOW to $\overline{\text{PAUSE}}$ LOW Delay (Note 5)		150		100		ns
TCSR	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ LOW Set-up Time		0		0		ns
TCSW	$\overline{\text{CS}}$ LOW to $\overline{\text{WR}}$ LOW Set-up Time		0		0		ns
TCY	Clock Period		480	5000	320	2000	ns
TDW	Data Valid to $\overline{\text{WR}}$ HIGH Delay		150		100		ns
TEAE	$\overline{\text{EACK}}$ LOW to END LOW Delay			200		175	ns
TEHPHR	END HIGH to $\overline{\text{PAUSE}}$ HIGH Data Read when Busy			5.5TCY+300		5.5TCY+200	ns
TEHPHW	END HIGH to $\overline{\text{PAUSE}}$ HIGH Write when Busy			200		175	ns
TEPW	END HIGH Pulse Width		400		300		ns
TEX	Execution Time		See Table 2				ns
TOP	Data Bus Output Valid to $\overline{\text{PAUSE}}$ HIGH Delay		0		0		ns
TPPWR	$\overline{\text{PAUSE}}$ LOW Pulse Width Read	Data	3.5TCY+50	5.5TCY+300	3.5TCY+50	5.5TCY+200	ns
		Status	1.5TCY+50	3.5TCY+300	1.5TCY+50	3.5TCY+200	
TPPWRB	END HIGH to $\overline{\text{PAUSE}}$ HIGH Read when Busy	Data	See Table 2				ns
		Status	1.5TCY+50	3.5TCY+300	1.5TCY+50	3.5TCY+200	
TPPWW	$\overline{\text{PAUSE}}$ LOW Pulse Width Write when Not Busy			TCSW+50		TCSW+50	ns
TPPWWB	$\overline{\text{PAUSE}}$ LOW Pulse Width Write when Busy		See Table 2				ns
TPR	$\overline{\text{PAUSE}}$ HIGH to Read HIGH Hold Time		0		0		ns
TPW	$\overline{\text{PAUSE}}$ HIGH to Write HIGH Hold Time		0		0		ns
TRCD	$\overline{\text{RD}}$ HIGH to C/$\overline{\text{D}}$ Hold Time		0		0		ns
TRCS	$\overline{\text{RD}}$ HIGH to $\overline{\text{CS}}$ HIGH Hold Time		0		0		ns
TRO	$\overline{\text{RD}}$ LOW to Data Bus On Delay		50		50		ns
TRZ	$\overline{\text{RD}}$ HIGH to Data Bus Off Delay		50	200	50	150	ns
TSAPW	SVACK LOW Pulse Width		100		75		ns
TSAR	SVACK LOW to SVREQ LOW Delay			300		200	ns
TWCD	$\overline{\text{WR}}$ HIGH to C/D Hold Time		60		30		ns
TWCS	$\overline{\text{WR}}$ HIGH to CS HIGH Hold Time		60		30		ns
TWD	$\overline{\text{WR}}$ HIGH to Data Bus Hold Time		20		20		ns

Notes: 1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Switching parameters are listed in alphabetical order.
3. Test conditions assume transition times of 20ns or less, output loading of one TTL gate plus 100pF and timing reference levels of 0.8V and 2.0V.
4. END HIGH pulse width is specified for $\overline{\text{EACK}}$ tied to VSS. Otherwise TEAE applies.
5. $\overline{\text{PAUSE}}$ is pulled LOW for both command and data operations.
6. TEX is the execution time of the current command (see the Command Execution Times table).
7. $\overline{\text{PAUSE}}$ will go LOW at this point if $\overline{\text{CS}}$ is LOW and $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are HIGH.

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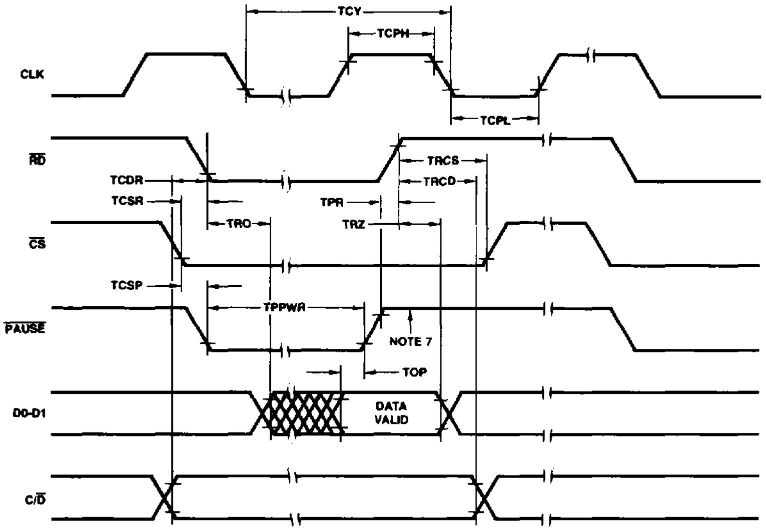
TIMING DIAGRAMS

READ OPERATION



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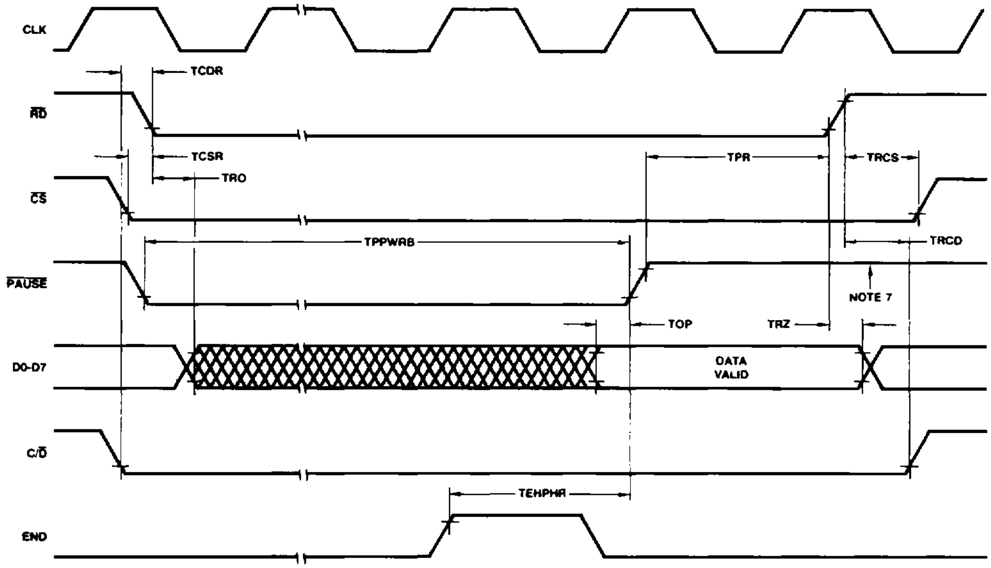
OPERAND READ WHEN Am9512 IS BUSY



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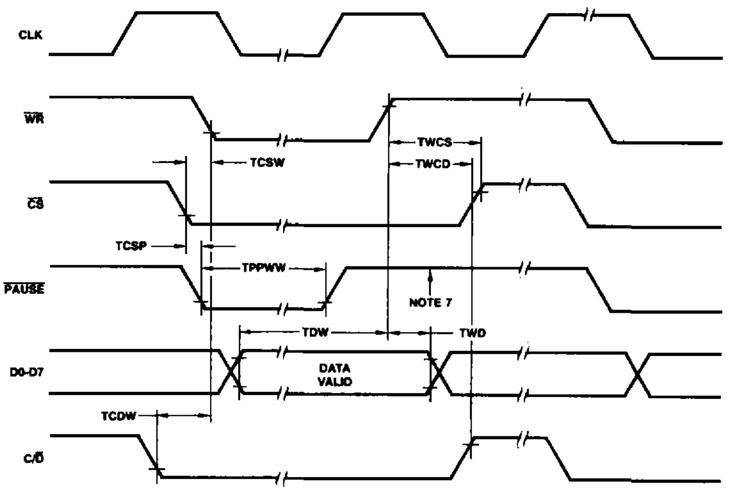
TIMING DIAGRAMS (Cont.)

OPERAND ENTRY



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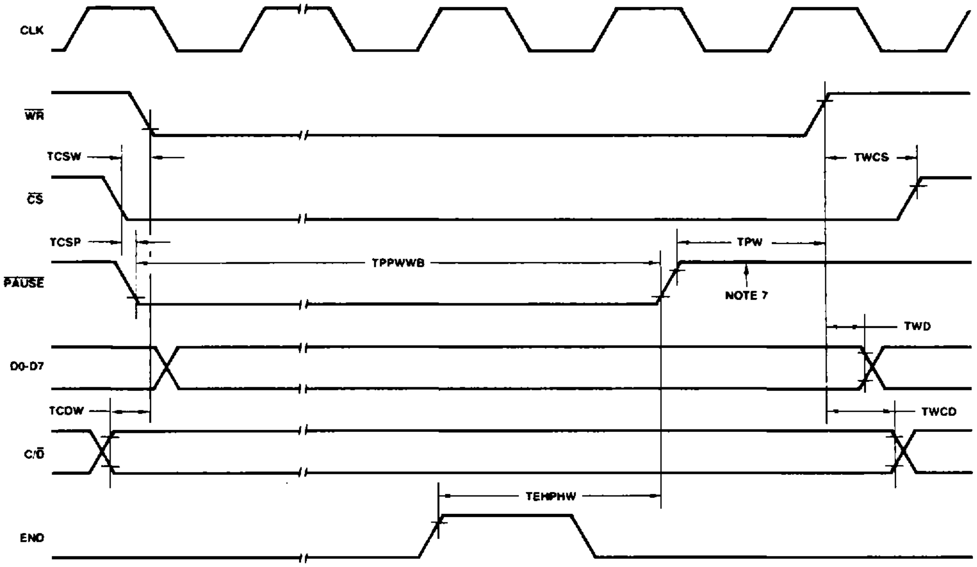
COMMAND OR DATA WRITE WHEN Am9512 IS BUSY



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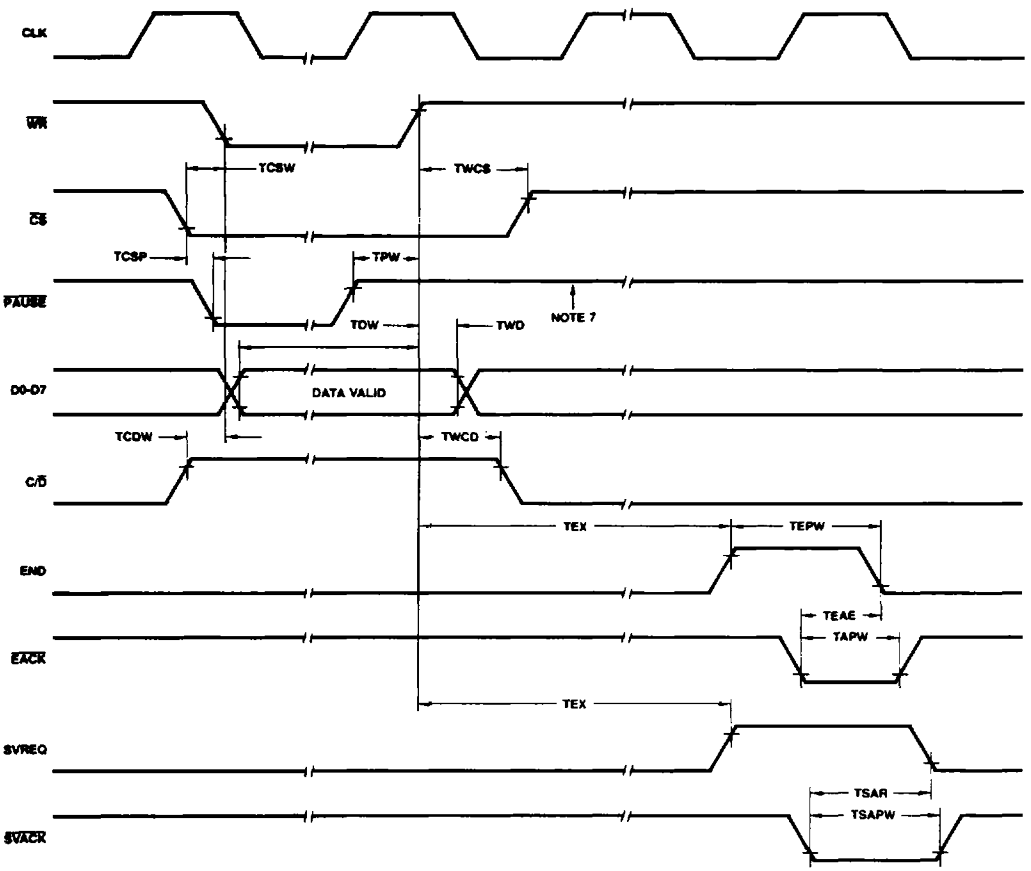
TIMING DIAGRAMS (Cont.)

COMMAND INITIATION



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