High Speed Analog N-Channel Enhancement-Mode DMOS Power FETs

calogic CORPORATION

SD220 / SD221

T-35-25

FEATURES

- Fast Switching ..... <1.0ns (typ)
- low capacitance
  - Ciss ..... 12 pF (typ)
  - Crss ..... .0.6 pF (typ)
- Low Threshold ..... <2.3V, TTL compatible

APPLICATIONS

- Broadband RF Power Amplifiers
- High Speed Switch Drivers
- High Speed Display Drivers
- CMOS and TTL to High Current Interfaces

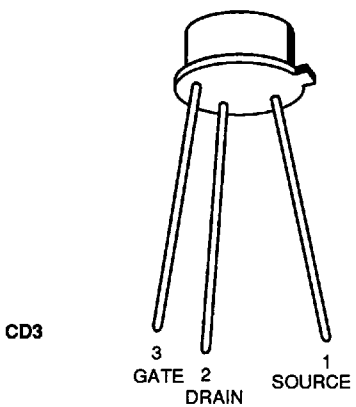
DESCRIPTION:

The SD220 and SD221 are high speed N-Channel enhancement mode medium power DMOS FETS. Designed for CMOS and TTL compatibility low voltage input, high speed and low capacitance. Each device is an excellent switch driver or analog switch.

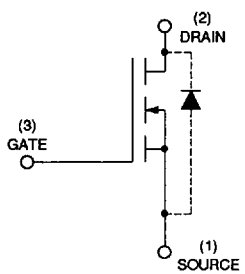
ORDERING INFORMATION

Part	Package	TemperatureRange
SD220HD	Hermetic TO-39 Package	-55°C to +150°C
SD221HD	Hermetic TO-39 Package	-55°C to +150°C
XSD220	Sorted Chips in Carriers	-55°C to +150°C
XSD221	Sorted Chips in Carriers	-55°C to +150°C

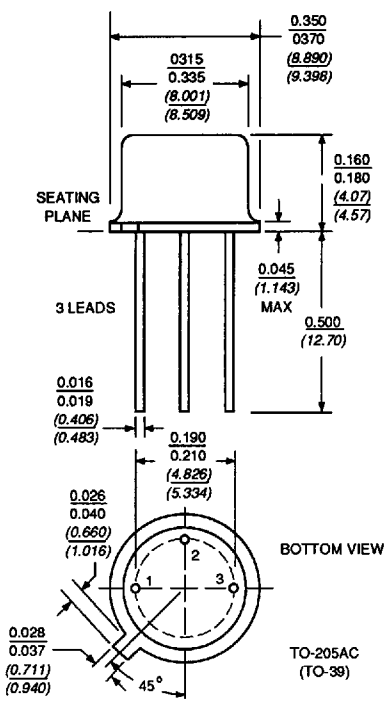
PIN CONFIGURATION



SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS



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ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage
- SD220 ..... +60 V
- SD221 ..... +100 V

V_{DG} Drain-Gate Voltage (RGS = 1 MΩ)
- SD220 ..... +60 V
- SD221 ..... +100 V

$V_{GS(F)}$ Gate-Source (Forward) Voltage ..... +30 V

$V_{GS(R)}$ Gate-Source (Reverse) Voltage ..... -30 V

I_D Continuous Drain Current

	T_C = +100°C	T_C = +25°C
SD220HD	.32A	.51A
SD221HD	.30A	.47A

I_{DM} Peak Pulsed DrainCurrent
- SD220 ..... 0.8A
- SD221 ..... 0.6A

P_D Maximum Power Dissipation

	T_C = +100°C	T_C = +25°C
HD, TO-39 Package	2.5W	6.25W

Linear Derating Factor

	Junction to Ambient (mW/ °C)	Junction to Case (mW/ °C)
HD, TO-39 Package	8.0	50

Operating Junction and Storage Temperature Range ..... -55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

SYMBOL	CHARACTERISTICS	SD220			SD221			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
STATIC										
BV_{DSS}	Drain Source Breakdown Voltage	60	80		100	115		V	I_D = 10μA, V_{GS} = 0	
$V_{GS(th)}$	Gate-Source Threshold Volage	0.1	0.8	2.3	0.1		2.3	V	I_D = 10μA, V_{DS} = V_{GS}	
		0.5	1.5	3.0	0 5		3.0		I_D = 1 mA, V_{DS} = V_{GS}	
I_{GSS}	Gate Leakage Current			±10			±10	nA	V_{GS} = 20, V_{DS} = 0	
I_{DSS}	Drain-Source OFF Leakage Current		0.1	10				μA	V_{DS} = 60 V	V_{GS} = 0
						0.1	10		V_{DS} = 100 V	
				1.0				mA	V_{DS} = 48 V	V_{GS} = 0, T_A = +125°C
							1.0		V_{DS} = 80 V	
$I_{D(ON)}$	ON (Note 1) Drain Current	500			300				V_{DS} = 6 V	V_{GS} = 10V
		600	700		400				V_{DS} = 10 V	
$r_{DS(ON)}$	Drain-Source ON Resistance (Note 1)		7.5	10			12	ohms	V_{GS} = 5V, I_D = 50 mA	
				16			19.2			T_A = +125°C
			6.5	9.0			10		V_{GS} = 10 V, I_D = 50 mA	
				15			16			T_A = +125°C
							14		V_{GS} = 10 V, I_D = 250 mA	
							21			T_A = +125°C
			9.0	12					V_{GS} = 10 V, I_D = 500 mA	
				18						T_A = +125°C
DYNAMIC										
g_{fs}	Common-Source Forward Transconductance (Note 1)	150	190		100			mS	V_{DS} = 30 V, I_D = 300 mA f = 1 KHz (Note 1)	
C_{iss}	Common-Source Input Capacitance		12	15		11	15	pF	V_{DS} = 30V, V_{GS} = 0 f = 1 MHz	
C_{oss}	Common-Source Output Capacitance		2.8	3.5		2.6	15			
C_{rss}	Common-Source Reverse Transfer Capacitance		0.6	1 0		0 6	1.0			
$t_{d(ON)}$	Turn-On Delay Time		1 0	2 0		1.0	2 0	nS	V_{DD} = 30 V, $V_{G(ON)}$ = 5.0 V, R_L = 90 ohms, R_G = 51 ohms	
t_r	Rise Time		1.0	3.0		1.0	3.0			
t_f	Fall Time		3.0	5 0		3.0	5 0			

NOTE 1: Pulse Test 80 μSec, 1% Duty Cycle