SONY

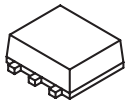
CXA3691EN

High-speed Buffer Amplifier for CCD Imager

Description

The CXA3691EN is a high-speed buffer amplifier IC.

6 pin WSON (Plastic)



Features

- Power consumption: 24mW (typ.)
  (External resistance R_{IDRV} = 220kΩ, during no signal)
- Push-pull output
- High-speed response: 500V/µs
  (R_{IDRV} = 220kΩ, C_L = 20pF)
- Internal sink current mode for CCD with open source output
  (Settable by external resistance R_{ISF})
- Enables to set the responsibility by changing the drive current by an external resistor

Structure

Bipolar silicon monolithic IC

Applications

- CCD image sensor output buffers
- Digital still cameras
- Camcorders
- Other general buffers

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	16	V
• Input voltage	IN	GND – 0.3 to V_{CC} + 0.3	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	0.28	W

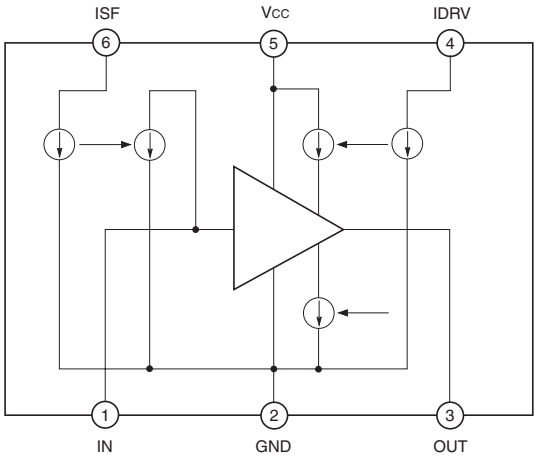
(when mounted on a two-layer board; 50mm × 50mm, t = 1.6mm)

Recommended Operating Conditions

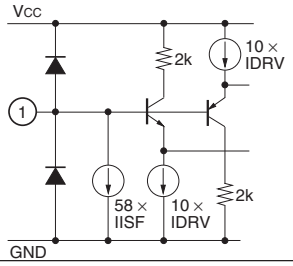
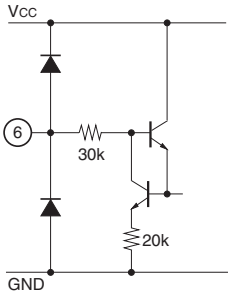
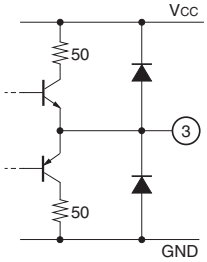
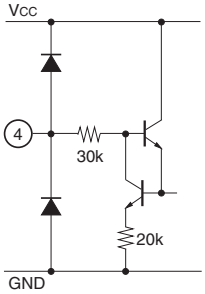
• Supply voltage	V_{CC}	11.0 to 15.5 (typ. 15)	V
• Operating temperature	Ta	–20 to +75	°C

E04658C78

Block Diagram and Pin Configuration (Top View)



Pin Description and I/O Pin Equivalent Circuit

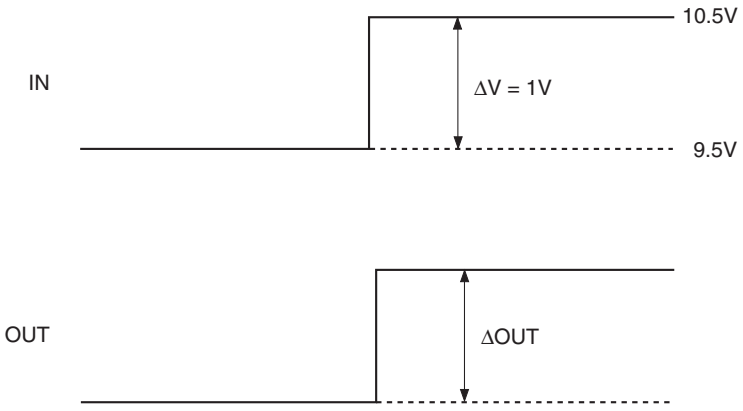
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
2	GND	—	0V	—	GND.
5	Vcc	—	15V	—	Supply voltage input.
1	IN	I	CCD output voltage		Input.
6	ISF	I	—		External resistor connection for setting the sink current for CCD with open source output. Connect an external resistor between this pin and Vcc (Pin 5). Connect this pin to GND (Pin 2) when not using this function. * The minimum value of the external resistance should be 100kΩ (when Vcc = 15V).
3	OUT	O	≈ IN		Output.
4	IDRV	I	—		External resistor connection for setting the drive current. Connect an external resistor between this pin and Vcc (Pin5). * The minimum value of the external resistance should be 100kΩ (when Vcc = 15V).

Electrical Characteristics (Ta = 25°C, V_{CC} = 15V, R_{IDRV} = 220kΩ, ISF pin: connected to GND)

DC Characteristics

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	IN = 10V, R_{IDRV} = 220kΩ	1.4	1.6	1.8	mA
Voltage gain	V_{GAIN}	*1 IN: 10Vdc ΔV = 1V GAIN = ΔOUT/ΔV	—	0.999	—	V/V
I/O offset voltage	V_{OFFSET}	IN = 10V V_{OFFSET} = OUT-IN	–100	—	100	mV
I/O voltage range	V_{RANGE}	R_{IDRV} = 100kΩ R_{IDRV} = 150kΩ R_{IDRV} = 220kΩ R_{IDRV} = 330kΩ	3.3 2.9 2.5 2.1	— — — —	V_{CC} – 2.4 V_{CC} – 2.2 V_{CC} – 2.0 V_{CC} – 1.8	V
Input bias current	I_{BIAS}	IN = 10V, I_{SF} = 0V	–15	–5	6	µA
Sync current	I_{SINK}	IN = 10V, R_{ISF} = 220kΩ	2.6	2.9	3.2	mA

*1 Voltage gain

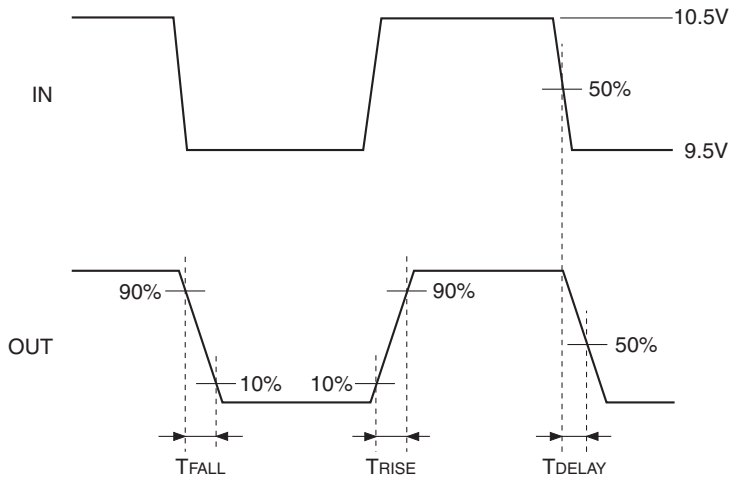


AC Characteristics

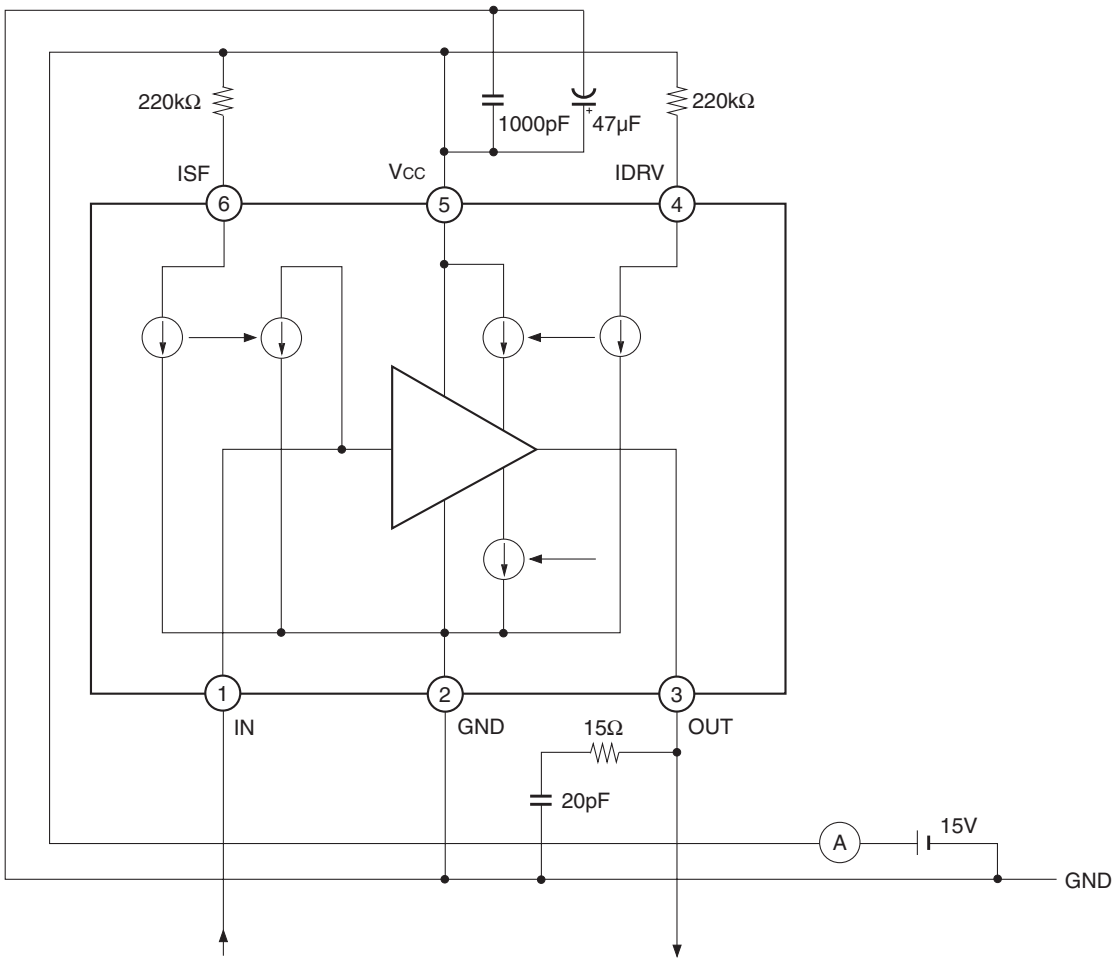
(Ta = 25°C, V_{CC} = 15V, R_{IDRV} = 220kΩ, ISF pin: connected to GND, R_L = 15Ω, C_L = 20pF)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bandwidth	GBW	IN = 50mVp-p	—	220	—	MHz
Rise time	T_{RISE}	*2 IN = 9.5 to 10.5V 10 to 90%	—	2.5	3.5	ns
Fall time	T_{FALL}	*2 IN = 10.5 to 9.5V 10 to 90%	—	3.0	4.0	ns
I/O delay time	T_{DELAY}	*2 IN = 9.5 to 10.5V @50%	0.9	1.0	2.0	ns

*2 Rise time, fall time and I/O delay time



Evaluation Circuit



Description of Operation

Current Settings

1. Output Drive Current

The small signal output impedance of the OUT pin (Pin 3) can be set by connecting the IDRV pin (Pin 4) to V_{CC} through a resistor. The inflow current to the IDRV pin is multiplied by 10 times inside the IC, and flows as the output stage idling current.
The IDRV pin has an internal 50kΩ resistor, so the inflow current to the IDRV pin can be calculated as follows.

$$I_{IDRV} = (V_{CC} - V_{BE} \times 2)/(R_{IDRV} + 50k\Omega)$$
$$= (15 - 1.46)/270k\Omega$$
$$= 50.1\mu A$$

Here, V_{CC} = 15V, V_{BE} = 0.73V (typ.), and R_{IDRV} = 220kΩ.
The small signal output impedance at this time can be calculated as follows.

$$R_{OUT} = (26mV/(10 \times I_{IDRV}))/2$$
$$= (26mV/501\mu A)/2$$
$$= 26\Omega$$

2. Sink Current for CCD with open source output

The sink current of the IN pin (Pin 6) can be set by connecting the ISF pin (Pin 1) to V_{CC} through a resistor. This sink current can be used as the CCD output stage source follower drive current. The inflow current to the ISF pin is multiplied by 58 times inside the IC, and flows as the sink current.
The ISF pin has an internal 50kΩ resistor, so the inflow current to the ISF pin can be calculated as follows.

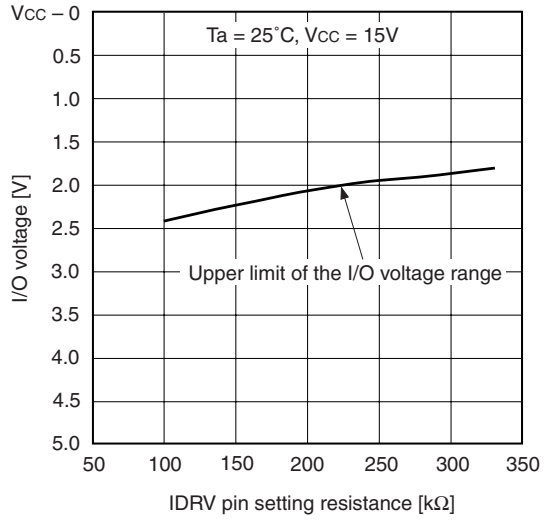
$$I_{ISF} = (V_{CC} - V_{BE} \times 2)/(R_{ISF} + 50k\Omega)$$
$$= (15 - 1.46)/270k\Omega$$
$$= 50.1\mu A$$

Here, V_{CC} = 15V, V_{BE} = 0.73V (typ.), and R_{ISF} = 220kΩ.
The sink current at this time can be calculated as follows.

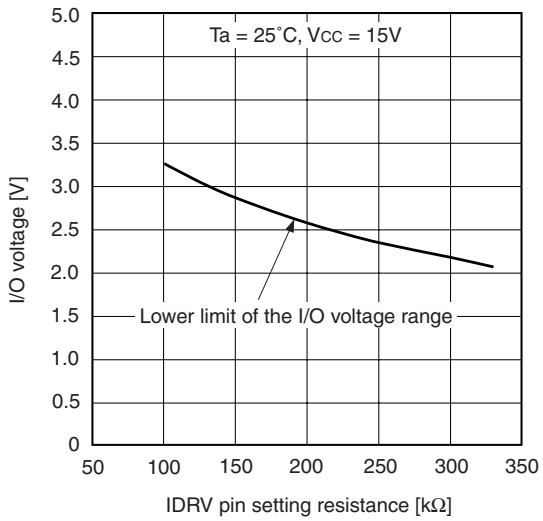
$$Isink = 58 \times I_{ISF}$$
$$= 2.9mA$$

Characteristics Graphs

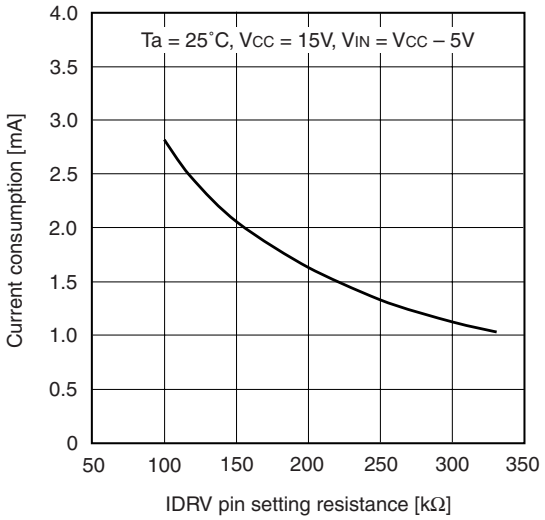
(Upper side) I/O voltage range vs. IDRV pin setting resistance



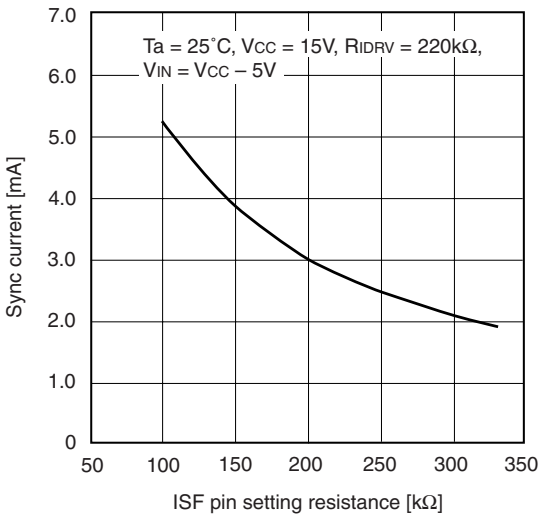
(Lower side) I/O voltage range vs. IDRV pin setting resistance



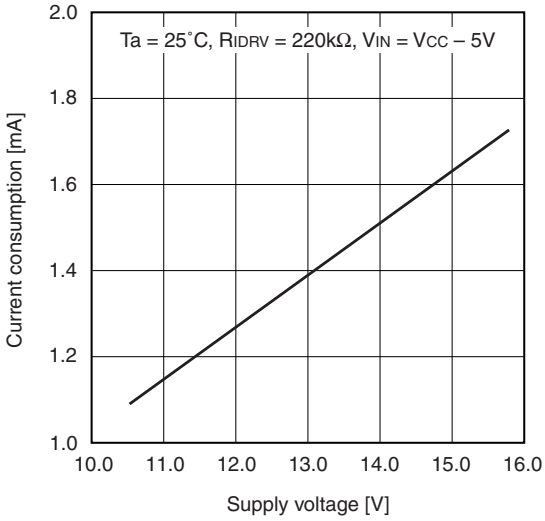
Current consumption vs. IDRV pin setting resistance



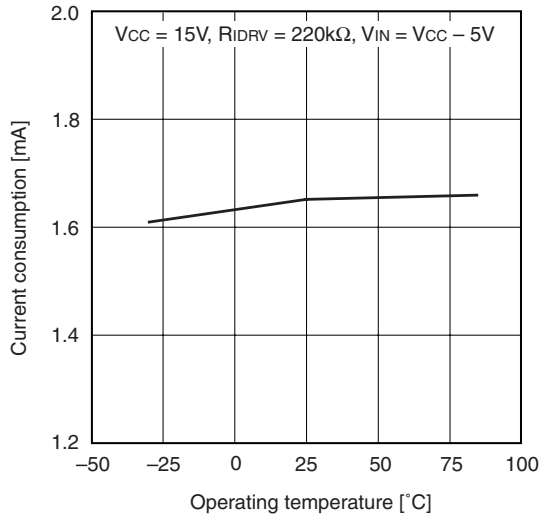
Sink current vs. ISF pin setting resistance



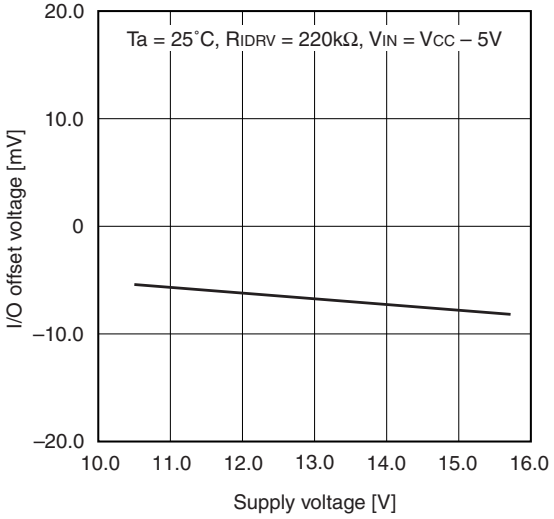
Current consumption vs. Supply voltage



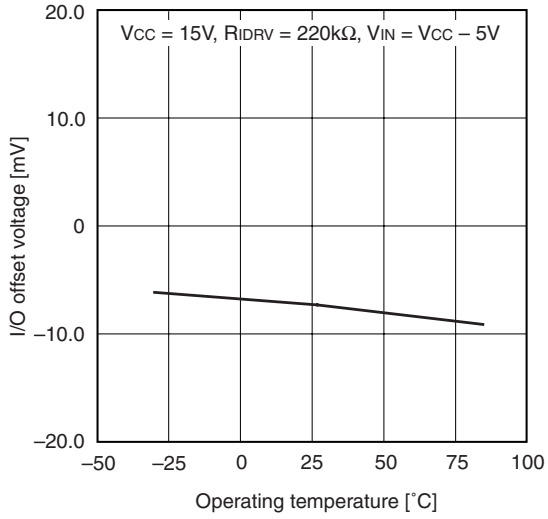
Current consumption vs. Operating temperature



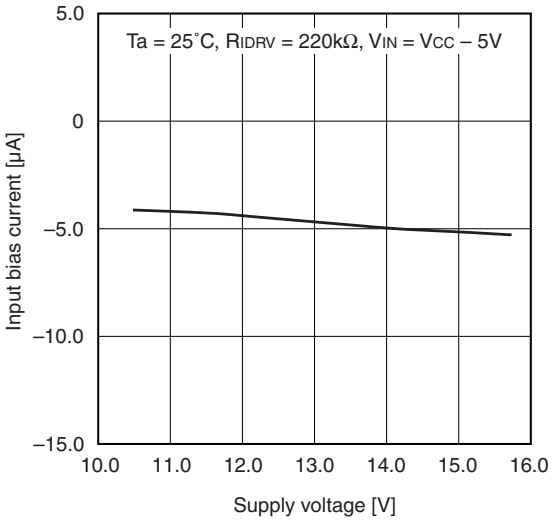
I/O offset voltage vs. Supply voltage



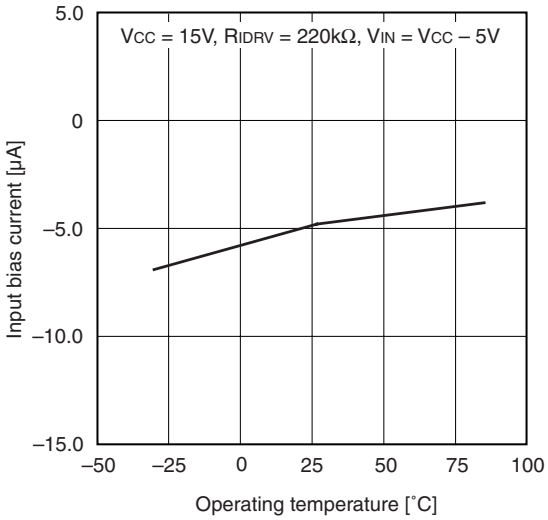
I/O offset voltage vs. Operating temperature



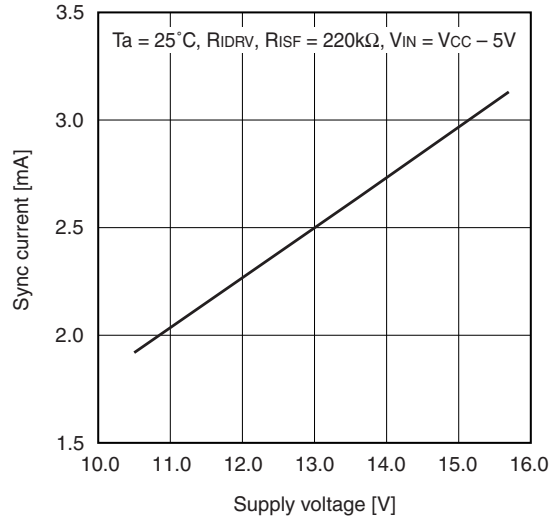
Input bias current vs. Supply voltage



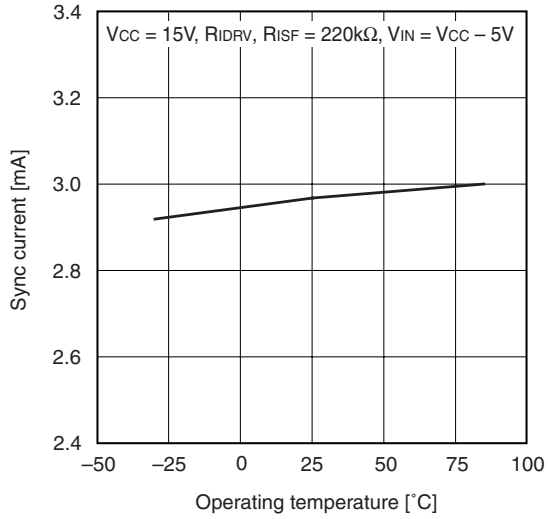
Input bias current vs. Operating temperature



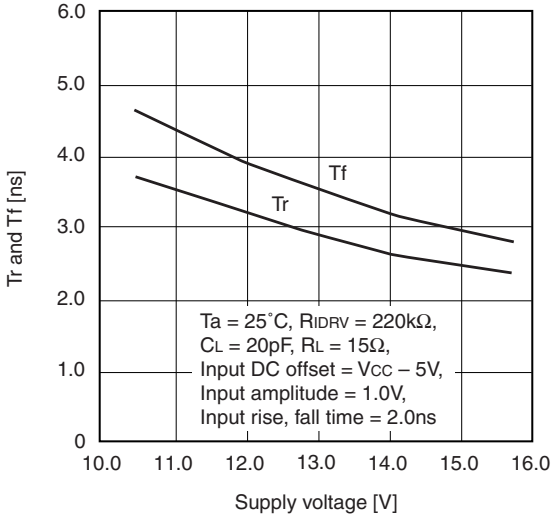
Sink current vs. Supply voltage



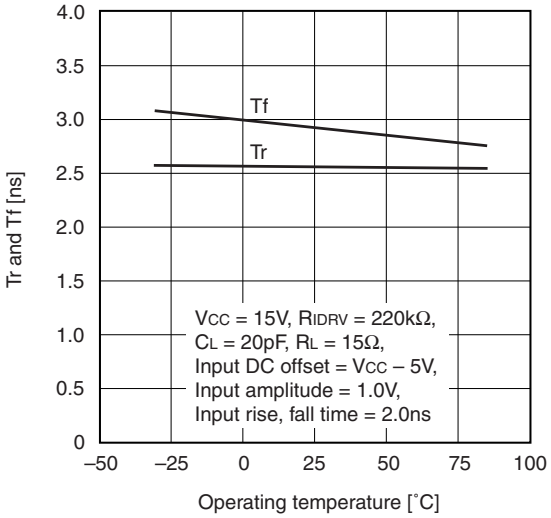
Sink current vs. Operating temperature



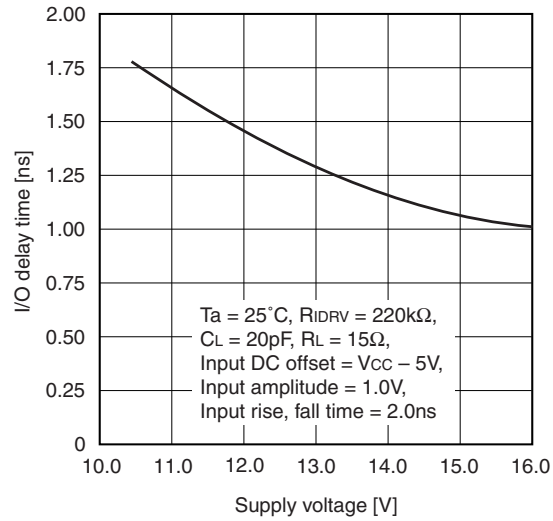
Tr and Tf vs. Supply voltage



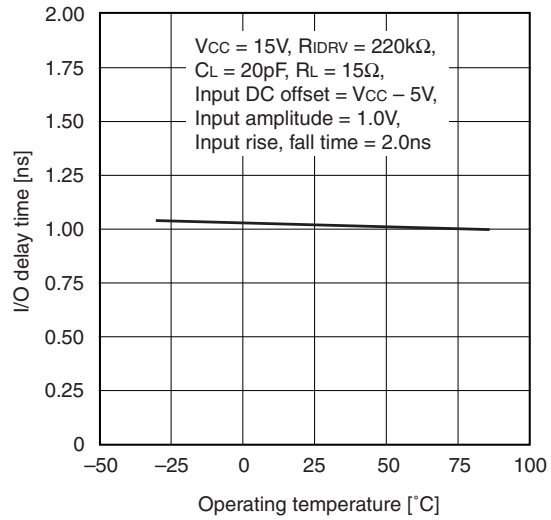
Tr and Tf vs. Operating temperature



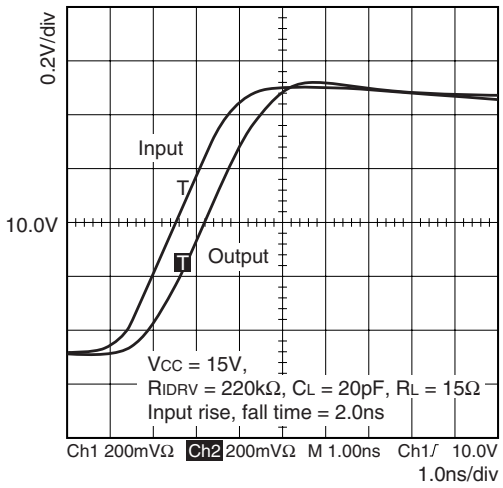
I/O delay time vs. Supply voltage



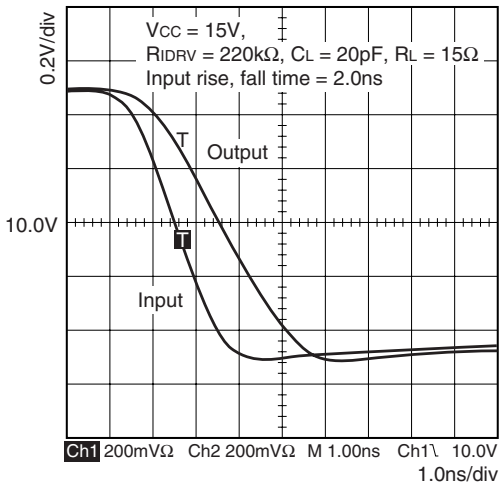
I/O delay time vs. Operating temperature



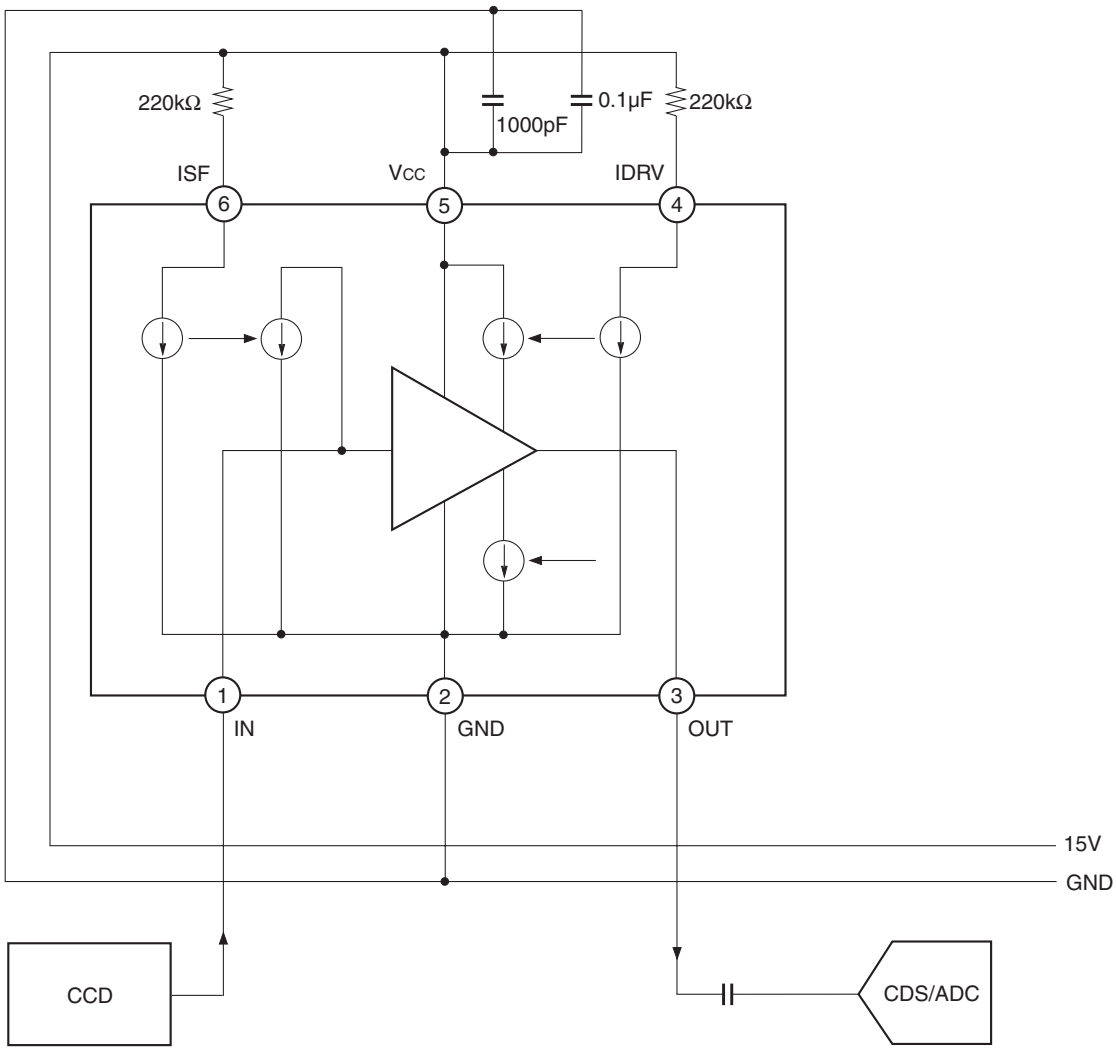
Positive pulse response



Negative pulse response

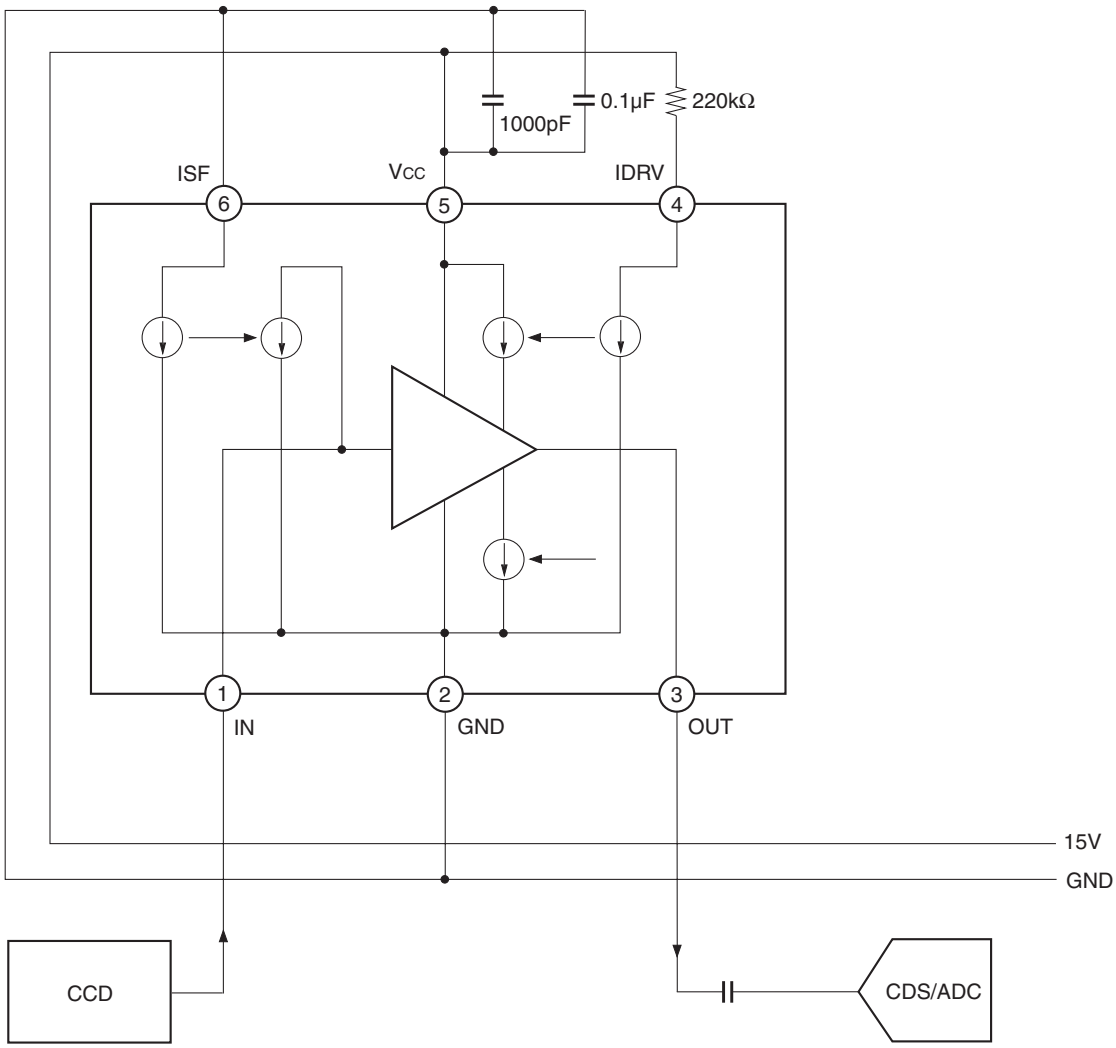


Application Circuit 1 (when using CCD with open source output)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 (when using CCD with internal current source)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

- Provide the widest GND pattern possible on the board.

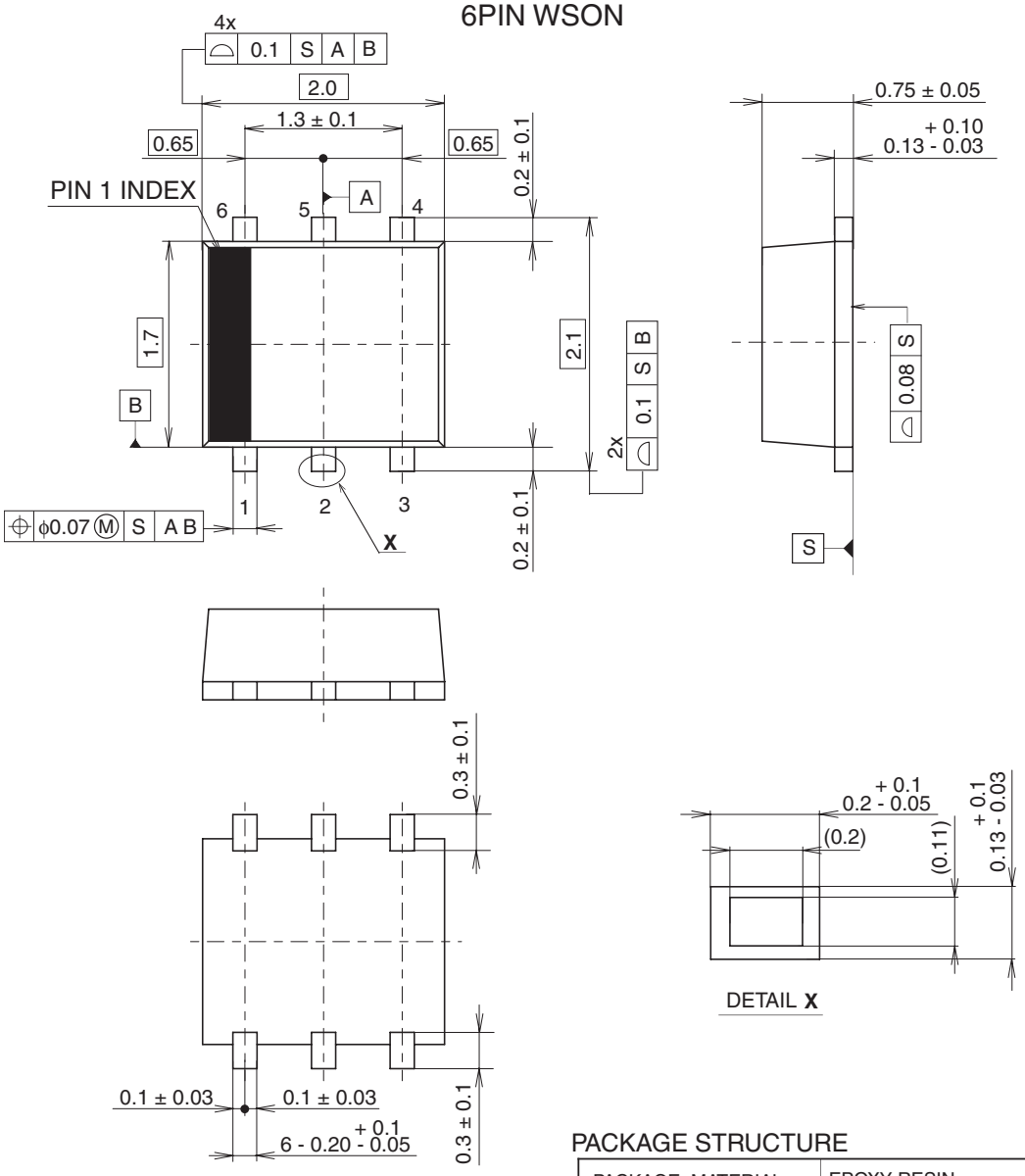
- Use a 1000pF (recommended) and a 0.1µF (recommended) ceramic capacitors in parallel for the bypass capacitor connected between the power supply and GND, and connect them as close to the IC pins as possible.

- Load capacitance causes the input/output wiring response to worsen and results in noise. Use the shortest wiring layout possible, and shield it with GND.

- When the output pin (Pin 3) is shorted to either the power supply or GND, an overcurrent may flow to the output stage elements and damage them.
  When the input pin (Pin 1) is shorted to GND, an overcurrent may flow to the internal parasitic elements and damage them.

Package Outline Unit: mm

6PIN WSON



SONY CODE	WSON-6P-051
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	Sn-Bi
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.008g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

Sony Corporation