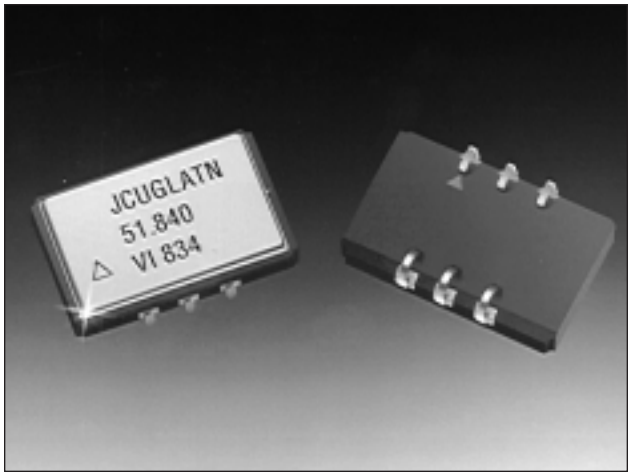
J-Type CMOS Output Option



Description:

The J-Type CMOS output option is a high reliability CMOS VCXO, ASIC based and available in a 6 or 4 pin J-Lead ceramic package.

Features:

- **Output Frequencies from 1.024 MHz to 77.76 MHz**
- **3.3 or 5.0 volt options**
- **Small 14mm x 9mm J-Lead Package**
- **Low phase noise and custom options**
- **0/70°C or –40/85°C operating temperature**
- **Tri-state output (CMOS)**

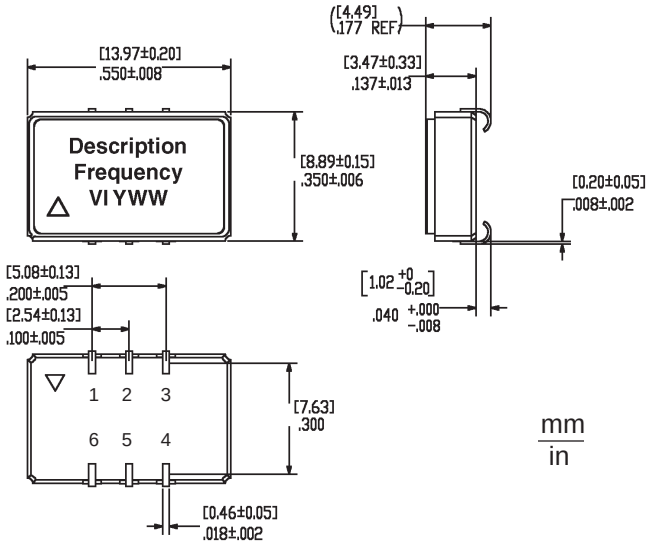
Performance Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Center Frequency, *see ordering information*	f_0	1.024		77.760	MHz
Supply Voltage[1], +5.0 volt option +3.3 volt option		4.5 3.0	5.0 3.3	5.5 3.6	Vdc Vdc
Maximum Supply Voltage				7	V
Supply Current (frequency dependent)		10 mA +0.25 mA per MHz, typical			
Output Level High	V_{OH}	0.8*Vcc	-		V
Output Level Low	V_{OL}		-	0.1*Vcc	V
Output Rise and Fall Time	t_R/t_F			5	ns
Symmetry (Duty Cycle[2])	SYM	45/55 or 40/60			%
Operating Temperature, see ordering info	T_{OP}	0/70, -40/85			°C
RMS Jitter, Output = 12.0-77.760 MHz			*3*		ps
RMS Jitter, Output = 12.0 -77.760 MHz, Band = 12.0 kHz to 20 MHz			<0.5		ps
Absolute Pull Range over the operating temperature range, aging and power supply. Vc= 0.5 to 4.5 supply or 0.3 to 3.0V at 3.3V supply. *See ordering information for options*	APR	±50, ±100			ppm
Control Range		0		V_{DD}	
Gain Transfer: (Frequency vs. Control Voltage)	K_V	Positive			
Control Input Leakage	I_L			1	uA
Control Voltage Modulation Bandwidth	BW		10		kHz
Storage Temperature	T_S	-55	-	125	°C
Soldering Temp./Time	T_{LS}	-	-	220/10	°C/s
Package Size	14 x 9 x 4.5 mm				

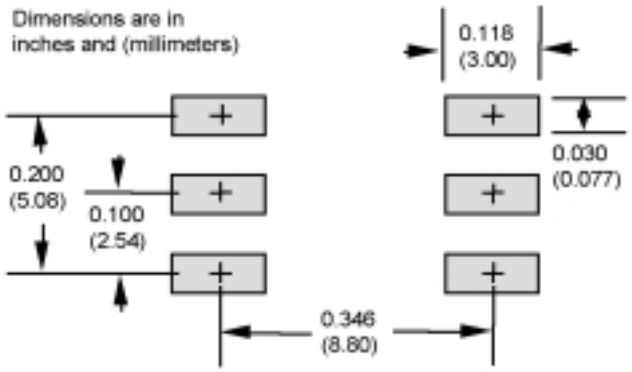
1. Power supply bypass is required and a 0.1uF in parallel with a 0.01uF high frequency capacitor is recommended.
2. Duty cycle is defined as on-time versus period at 1.4V for TTL and 2.5V for CMOS (5 volt supply) and at 1.65 V for CMOS (3.3 volt operation)

CMOS Output Option

Outline Drawing



Pad Layout



Pin Out Information

Pin	Symbol	Function
1	Vc	VCXO Control Voltage.
2	Tri-state	TTL logic low disables output TTL logic high, or no connect, enables output
3	GND	Case and electrical ground.
4	Output	VCXO Output
5	CMOS/TTL select	TTL logic low optimizes symmetry for CMOS TTL logic high, or NC, optimizes symmetry for TTL.
6	V_{CC}	Power Supply Voltage (5.0 V or 3.3V ±10%)

Standard Frequencies (MHz)

1.024	1.544	2.000	2.048	3.088	3.580
3.686	4.000	4.032	4.096	4.434	5.000
6.144	6.176	6.312	6.400	8.000	8.192
8.448	10.000	12.000	12.288	12.352	13.000
14.318	15.360	15.440	16.000	16.384	18.432
19.44	20.000	20.480	24.000	24.576	24.704
27.000	30.000	32.000	32.768	34.368	35.328
38.880	40.000	40.960	44.736	50.000	51.840
52.000	65.536	77.760			

Ordering Information

J D U G C J T N – 44.736 MHz

Package:
6-Pin Ceramic SOJ

Supply Voltage
D = 3.3 Vdc ±10%
C = 5.0 Vdc ±10%

Output
U = VCXO
L = ±10% Linear VCXO

APR
G = ±50 ppm
N = ±80 ppm
H = ±100 ppm

Temperature Range
C = 0 to 70°C
L = -40 to 85°C

Duty Cycle
A = TTL/CMOS 45/55%
J = CMOS 45/55%
K = CMOS 40/60%

Tri-state
T = Pin 2

Specials
N = Standard

Frequency
1.024 - 77.760 MHz