

Advance Information

16M CMOS Dynamic RAM Family

Extended Data Out, x4, 2K and 4K Refresh

The family of 16M dynamic RAMs is fabricated using 0.4μ CMOS high-speed silicon-gate process technology. It includes devices organized as 4,194,304 four-bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The x4 devices with 2048 cycle refresh (MCM317405C) require only 11 address lines.

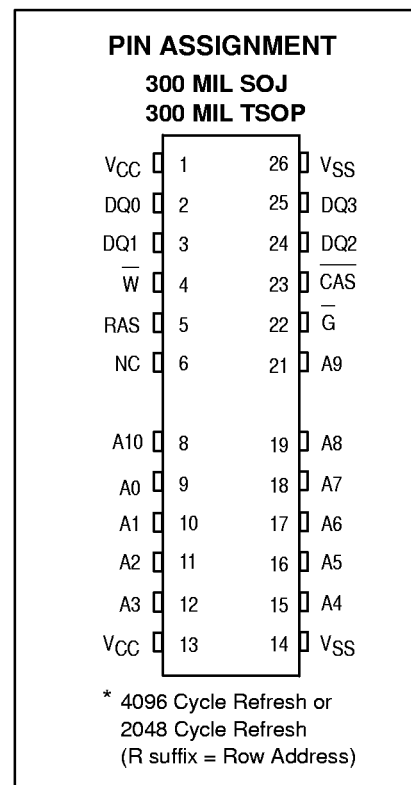
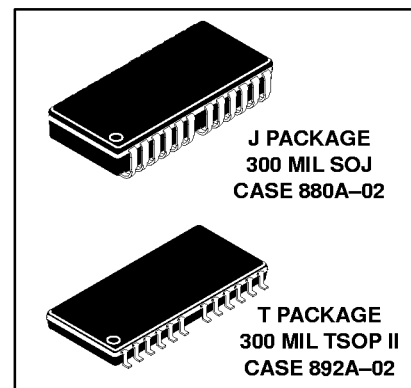
These devices are packaged in a standard 300 mil J-lead small outline package (SOJ) and a 300 mil thin-small-outline package (TSOP).

- Three-State Data Output
- Extended Data Out
- TTL-Compatible Inputs and Outputs
- RAS-Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM317405C = 32 ms
- Fast Access Time (t_{RAC}):
 - MCM317405C-50 = 50 ns (Max)
 - MCM317405C-60 = 60 ns (Max)
 - MCM317405C-70 = 70 ns (Max)
- Low Active Power Dissipation:
 - MCM317405C-50 = 800 mW (Max)
 - MCM317405C-60 = 660 mW (Max)
 - MCM317405C-70 = 580 mW (Max)
- Low Standby Power Dissipation:
 - All Devices = 11 mW (Max, TTL Levels)
 - All Devices = 5.5 mW (Max, CMOS Levels)

4M x 4

MCM317405C

Extended Data Out
2048 Cycle Refresh

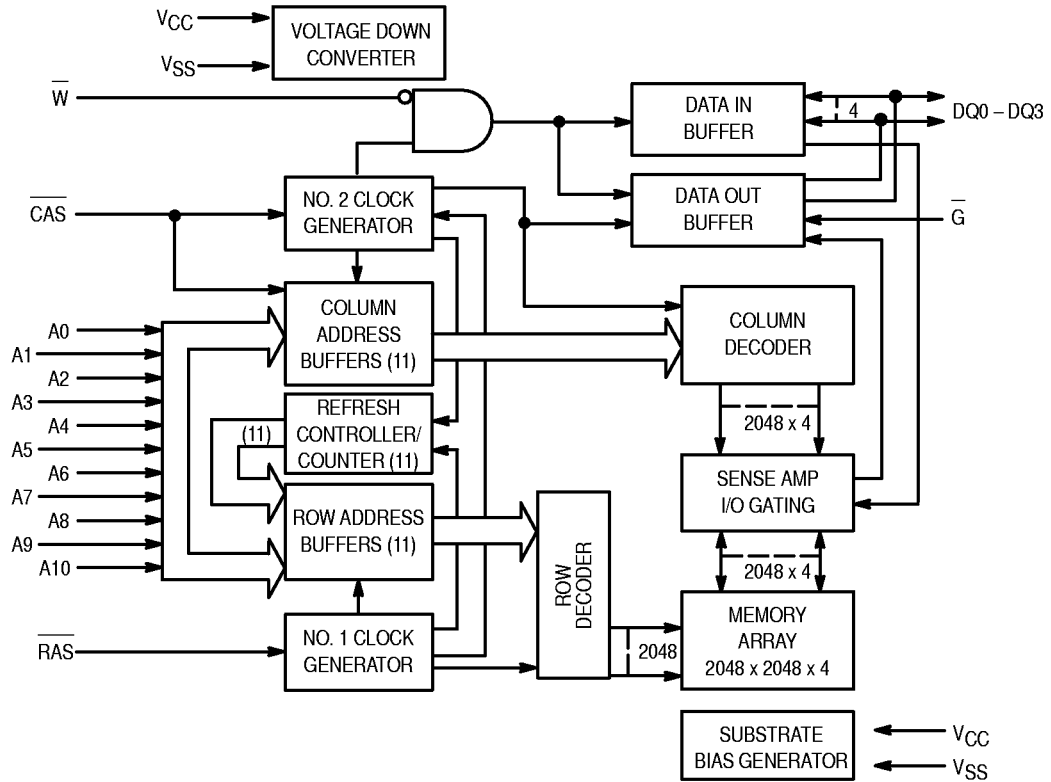


PIN NAMES	
A0 – A11 Address Input	CAS Column Address Strobe
<u>DQ0</u> – <u>DQ3</u> Data Input/Output	VCC Power Supply (+ 5 V)
<u>G</u> Output Enable	VSS Ground
<u>W</u> Read/Write Enable	NC No Connection
RAS Row Address Strobe	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM

2048 CYCLE REFRESH BLOCK DIAGRAM MCM317405C



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	- 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	- 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	1000	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	- 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 10\%$, $T_A = 0\text{ to }70^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All Voltages Referenced To V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	5.5	V
Logic Low Voltage, All Inputs	V_{IL}	- 1.0*	—	0.8	V

* -2.0 V at pulse width $\leq 25\text{ ns}$.

DC CHARACTERISTICS AND SUPPLY CURRENTS (See Note 1)

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current (Operating) MCM317405C-50, $t_{RC} = 90$ ns MCM317405C-60, $t_{RC} = 110$ ns MCM317405C-70, $t_{RC} = 130$ ns	I_{CC1}	—	145 120 105	mA	2, 3, 4
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{IH}) Output Open	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During RAS-Only Refresh Cycles (CAS = V_{IH}) Output Open MCM317405C-50, $t_{RC} = 90$ ns MCM317405C-60, $t_{RC} = 110$ ns MCM317405C-70, $t_{RC} = 130$ ns	I_{CC3}	—	145 120 105	mA	2, 4
V_{CC} Power Supply Current During Extended Data Out Cycle (RAS = V_{IL}), (CAS cycling) Output Open MCM317405C-50, $t_{PC} = 20$ ns MCM317405C-60, $t_{PC} = 25$ ns MCM317405C-70, $t_{PC} = 30$ ns	I_{CC4}	—	140 115 90	mA	2, 3, 4
V_{CC} Power Supply Current (Standby) (RAS = CAS $\geq V_{CC} - 0.2$ V)	I_{CC5}	—	0.5	mA	
V_{CC} Power Supply Current During CAS or Before RAS Refresh Cycle, Output Open MCM317405C-50, $t_{RC} = 90$ ns MCM317405C-60, $t_{RC} = 110$ ns MCM317405C-70, $t_{RC} = 130$ ns	I_{CC6}	—	145 120 105	mA	2, 4
Input Leakage Current ($0 \text{ V} \leq V_{in} \leq 6.0 \text{ V}$, Other Input Pins = 0 V)	$I_{kg(I)}$	-10	10	μA	
Output Leakage Current ($0 \text{ V} \leq V_{out} \leq 5.5 \text{ V}$, Q Floating)	$I_{kg(O)}$	-10	10	μA	
Output High Voltage ($I_{OH} = -5$ mA)	V_{OH}	2.4	—	V	
Output Low Voltage ($I_{OL} = 4.2$ mA)	V_{OL}	—	0.4	V	

NOTES:

- All voltages are referenced to V_{SS} .
- I_{CC1} , I_{CC3} , I_{CC4} , and I_{CC6} depend on cycle rate.
- I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
- Address can be changed once or less while RAS = V_{IL} . In case of I_{CC4} , it can be changed once or less during an extended data out cycle (t_{PC}).

CAPACITANCE ($f = 1.0$, $T_A = 25^\circ$, $V_{CC} = 5$ V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit	
Input Capacitance	$\overline{A0 - A11, D}$ $\overline{G, RAS, CAS, W}$	C_{in}	5	pF
			7	
I/O Capacitance (CAS = V_{IH} to Disable Output)	$\overline{DQ0 - DQ3, Q}$	$C_{I/O}$	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I \Delta t / \Delta V$.

16M FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM317405C-50		MCM317405C-60		MCM317405C-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t _{RELREL}	t _{RC}	90	—	110	—	130	—	ns	
Read-Write Cycle Time	t _{RELREL}	t _{RWC}	109	—	133	—	161	—	ns	
Access Time from RAS	t _{RELQV}	t _{RAC}	—	50	—	60	—	70	ns	8, 13, 14
Access Time from CAS	t _{CELQV}	t _{CAC}	—	13	—	15	—	20	ns	8, 13
Access Time from Column Address MCM317405C	t _{AVQV}	t _{AA}	—	25	—	30	—	35	ns	8, 14
Access Time from Precharge CAS	t _{CEHQV}	t _{CPA}	—	30	—	35	—	40	ns	8
CAS to Output in Low-Z	t _{CELQX}	t _{CLZ}	5	—	5	—	5	—	ns	8
Output Buffer and Turn-Off Delay	t _{CEHQZ}	t _{OFF}	0	13	0	15	0	20	ns	9
Transition Time (Rise and Fall)	t _T	t _T	1	50	1	50	1	50	ns	7
RAS Precharge Time	t _{REHREL}	t _{RP}	30	—	40	—	50	—	ns	
RAS Pulse Width	t _{RELREH}	t _{RAS}	50	10 k	60	10 k	70	10 k	ns	
RAS Hold Time	t _{CELREH}	t _{RSH}	13	—	15	—	20	—	ns	
CAS Hold Time	t _{RELCEH}	t _{CSH}	40	—	48	—	55	—	ns	
CAS Precharge to RAS Hold Time	t _{CEHREH}	t _{RHCP}	28	—	33	—	38	—	ns	
CAS Pulse Width	t _{CELCEH}	t _{CAS}	8	10 k	10	10 k	13	10 k	ns	
RAS to CAS Delay Time	t _{RELCEL}	t _{RCD}	18	32	20	38	20	42	ns	13
RAS to Column Address Delay Time	t _{RELAV}	t _{RAD}	13	25	15	30	15	35	ns	14
CAS to RAS Precharge Time	t _{CEHREL}	t _{CRP}	5	—	5	—	5	—	ns	
CAS Precharge Time	t _{CEHCEL}	t _{CP}	8	—	10	—	13	—	ns	
Row Address Setup Time	t _{AVREL}	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RELAX}	t _{RAH}	8	—	10	—	10	—	ns	

NOTES:

- All voltages are referenced to V_{SS}.
- I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
- I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
- Address can be changed once or less while RAS = V_{IL}. In case of I_{CC4}, it can be changed once or less during an extended data out cycle (t_{PC}).
- An initial pause of 200 μs is required after power-up followed by 8 RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS before RAS refresh cycles instead of 8 RAS only refresh cycles are required.
- AC measurements t_T = 5.0 ns.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
- Measured with a load equivalent to 2 TTL loads and 100 pF.
- t_{OFF} (max) and t_{GZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in Read-Modify-Write cycles.
- t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS} (min), the cycle is an early write cycle and the DQ pins remain high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD} (min), t_{RWD} ≥ t_{RWD} (min), t_{AWD} ≥ t_{AWD} (min), and t_{CPWD} ≥ t_{CPWD} (min) (for extended data out cycle only), the cycle is a read-modify-write cycle and the DQ pins will contain the data read from the selected address. If neither of these conditions are met, delayed write or at access time and until CAS or OE goes back to V_{IH}, DQ is indeterminate.
- Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
- Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

ALL DEVICES, READ, WRITE, AND READ-WRITE CYCLES (continued)

Parameter	Symbol		MCM317405C-50		MCM317405C-60		MCM317405C-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t _{AVCEL}	t _{ASC}	0	10	0	13	0	13	ns	
Column Address Hold Time	t _{CELAX}	t _{CAH}	8	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t _{AVREH}	t _{RAL}	25	—	30	—	35	—	ns	
Read Command Setup Time	t _{WHCEL}	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t _{CEHWX}	t _{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to RAS	t _{REHWX}	t _{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time Referenced to CAS	t _{CELWH}	t _{WCH}	8	—	10	—	13	—	ns	
Write Command Pulse Width	t _{WLWH}	t _{WCP}	8	—	10	—	13	—	ns	
Write Command to RAS Lead Time	t _{WLREH}	t _{RWL}	8	—	10	—	13	—	ns	
Write Command to CAS Lead Time	t _{WLCEH}	t _{CWL}	8	—	10	—	13	—	ns	
Data In Setup Time	t _{DVCEL}	t _{DS}	0	—	0	—	0	—	ns	11
Data In Hold Time	t _{CELDX}	t _{DH}	8	—	10	—	13	—	ns	11
Write Command Setup Time	t _{WLCEL}	t _{WCS}	0	—	0	—	0	—	ns	12
CAS to Write Delay	t _{CELWL}	t _{CWD}	28	—	32	—	42	—	ns	12
RAS to Write Delay	t _{RELWL}	t _{RWD}	65	—	77	—	92	—	ns	12
Column Address to Write Delay	t _{AVWL}	t _{AWD}	40	—	47	—	57	—	ns	12
Refresh Period MCM317405C	t _{RVRV}	t _{RFSSH}	—	32	—	32	—	32	ms	
CAS Setup Time for CAS Before RAS Refresh	t _{RELCEL}	t _{CSR}	5	—	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t _{RELCEH}	t _{CHR}	10	—	10	—	15	—	ns	
RAS Precharge to CAS Active Time	t _{REHCEL}	t _{RPC}	0	—	0	—	0	—	ns	
Write Command Setup Time (Test Mode)	t _{WLREL}	t _{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t _{RELWH}	t _{WTH}	10	—	10	—	15	—	ns	
Write to RAS Precharge Time (CAS Before RAS Refresh)	t _{WHREL}	t _{WRP}	10	—	10	—	10	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t _{RELWL}	t _{WRH}	10	—	10	—	10	—	ns	

DEVICE-SPECIFIC AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = 0 \text{ to } 70^\circ\text{C}$, Unless Otherwise Noted)

4M x 4 CONFIGURATION-SPECIFIC READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM317405C-50		MCM317405C-60		MCM317405C-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
RAS Hold Time Referenced to G	t _{GLREH}	t _{ROH}	13	—	15	—	20	—	ns	
G Access Time	t _{GLQV}	t _{GA}	—	13	—	15	—	20	ns	5
G to Data Delay	t _{GLHDX}	t _{GD}	13	—	15	—	20	—	ns	6
Output Buffer Turn-Off Delay Time from G	t _{GHQZ}	t _{GZ}	0	13	0	15	0	20	ns	
G Command Hold Time	t _{WLGL}	t _{GH}	13	—	15	—	20	—	ns	
Output Disable Setup Time	t _{GHCEL}	t _{GDS}	0	—	0	—	0	—	ns	

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
2. An initial pause of 200 μs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0 \text{ ns}$.
5. Measured with a current load equivalent to 2 TTL ($-200 \mu\text{A}$, $+4 \text{ mA}$) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0 \text{ V}$ and $V_{OL} = 0.8 \text{ V}$.
6. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

EXTENDED DATA OUT MODE ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(See Notes 1 through 5)

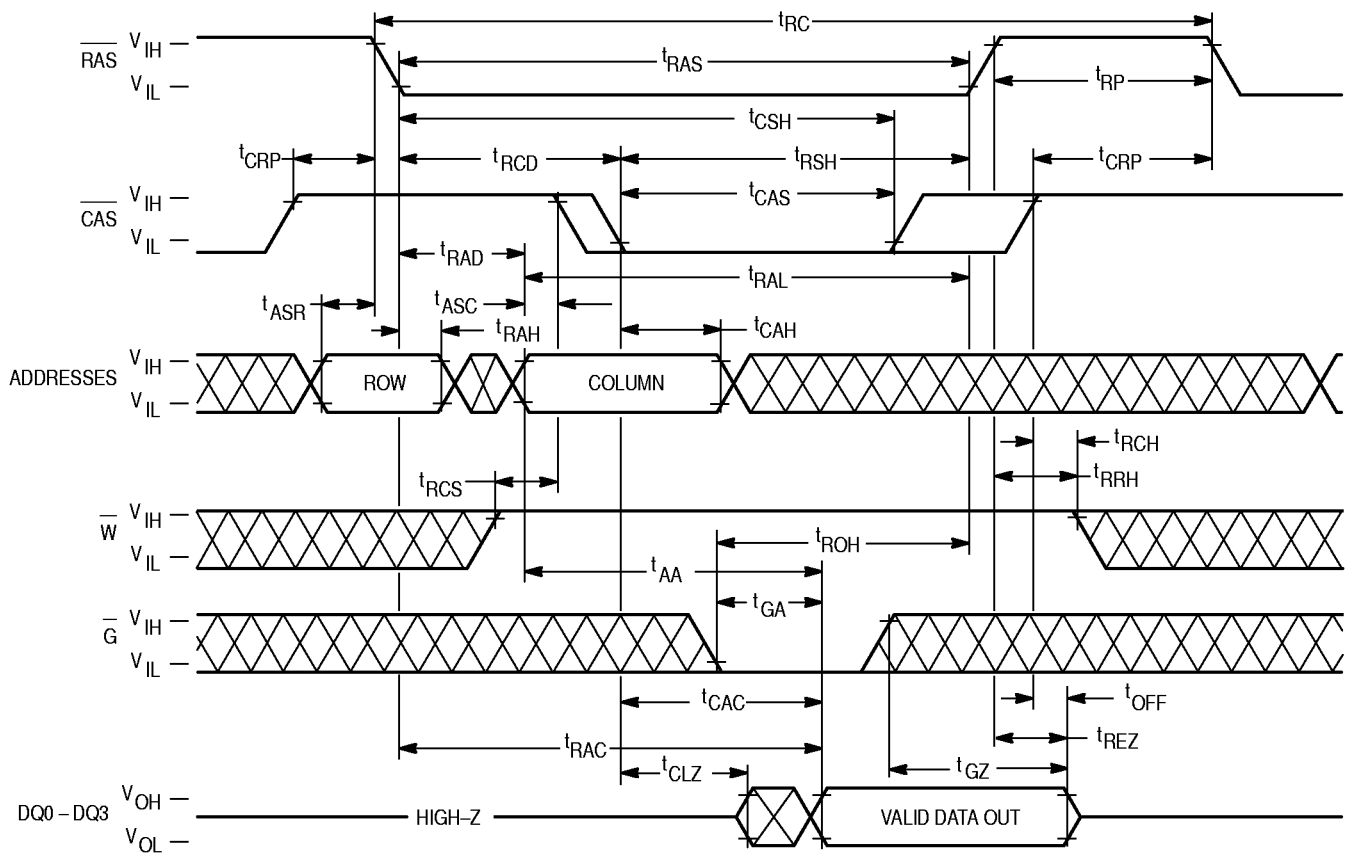
Parameter	Symbol		MCM317405C-50		MCM317405C-60		MCM317405C-70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
RAS to next CAS Delay Time (EDO mode)	t _{RELCEL}	t _{RNCD}	50	—	60	—	70	—	ns	
Extended Data Out Cycle Time	t _{EPC}	t _{EC}	20	—	25	—	30	—	ns	
Extended Data Out Read-Modify-Write Cycle Time	t _{CELCEL}	t _{ERWC}	57	—	66	—	79	—	ns	
Output Data Hold Time	t _{CELQZ}	t _{COH}	7	—	7	—	7	—	ns	
Output Buffer Turn-Off Delay from RAS	t _{REHQZ}	t _{REZ}	0	13	0	15	0	20	ns	
Output Buffer Turn-Off Delay from W	t _{WLQZ}	t _{WEZ}	0	13	0	15	0	20	ns	
G Precharge Time	t _{GHGL}	t _{GP}	7	—	7	—	7	—	ns	
CAS to G Precharge Time	t _{CEHGL}	t _{CPG}	7	—	7	—	7	—	ns	

NOTES:

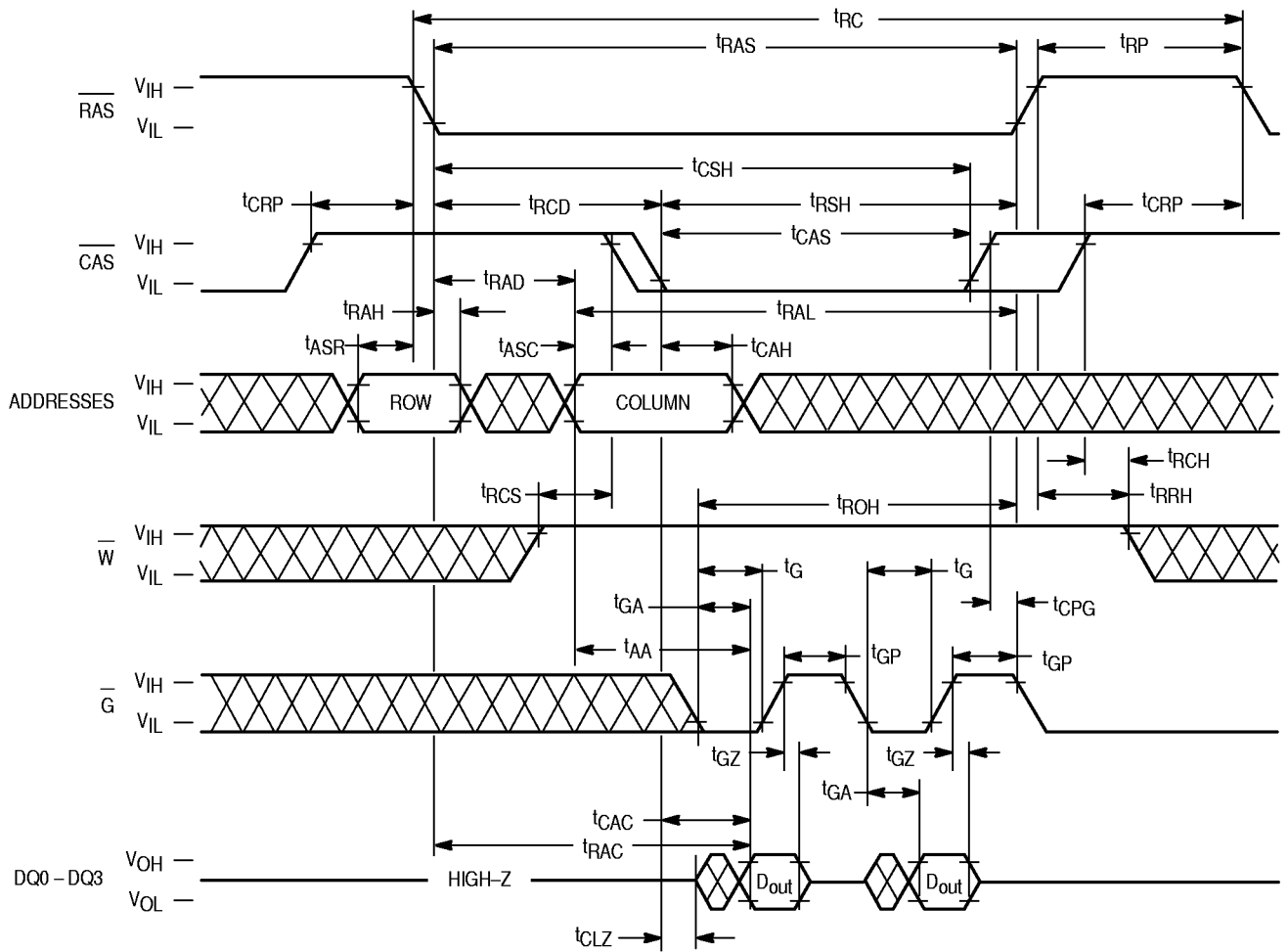
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} .
2. An initial pause of 200 μs is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements $t_T = 5.0 \text{ ns}$.
5. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through-out the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING DIAGRAMS

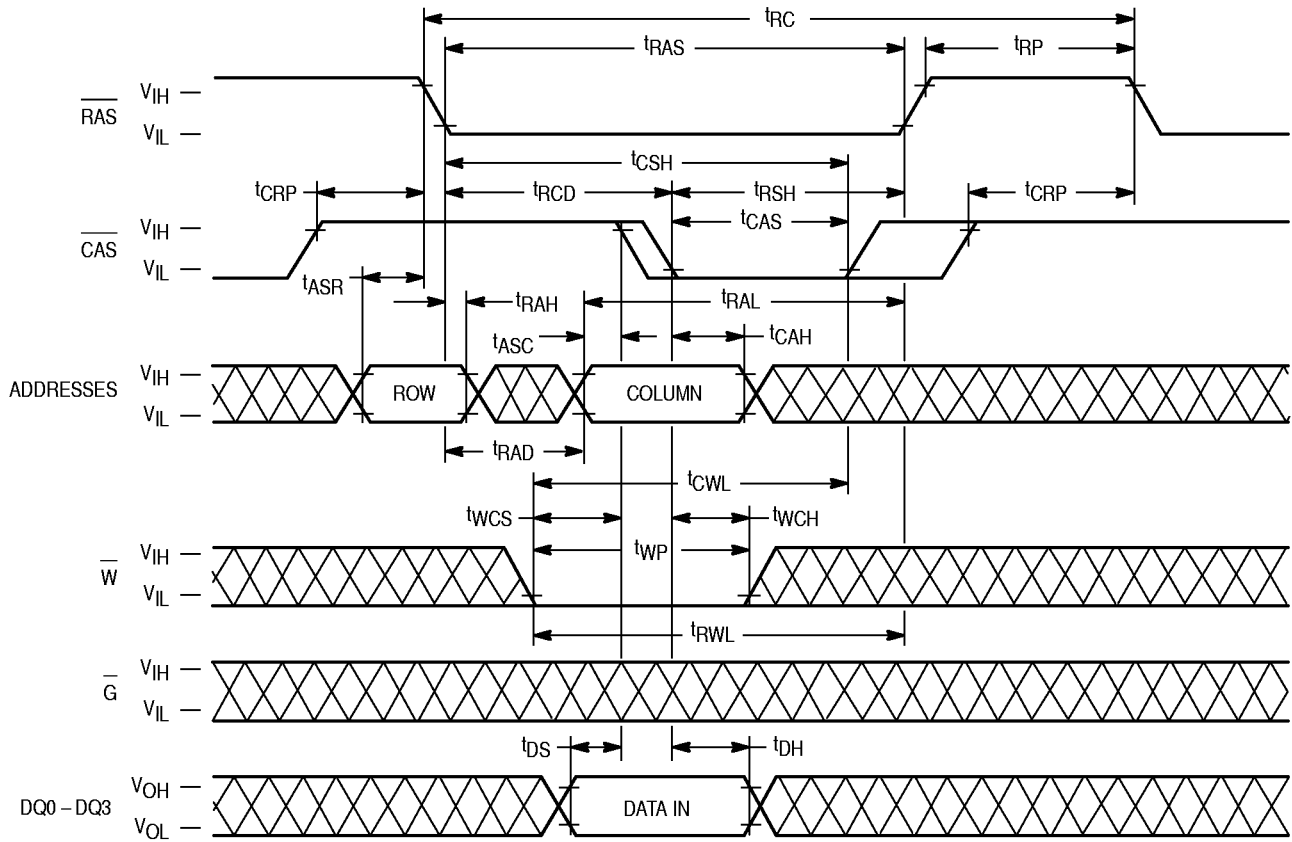
READ CYCLE



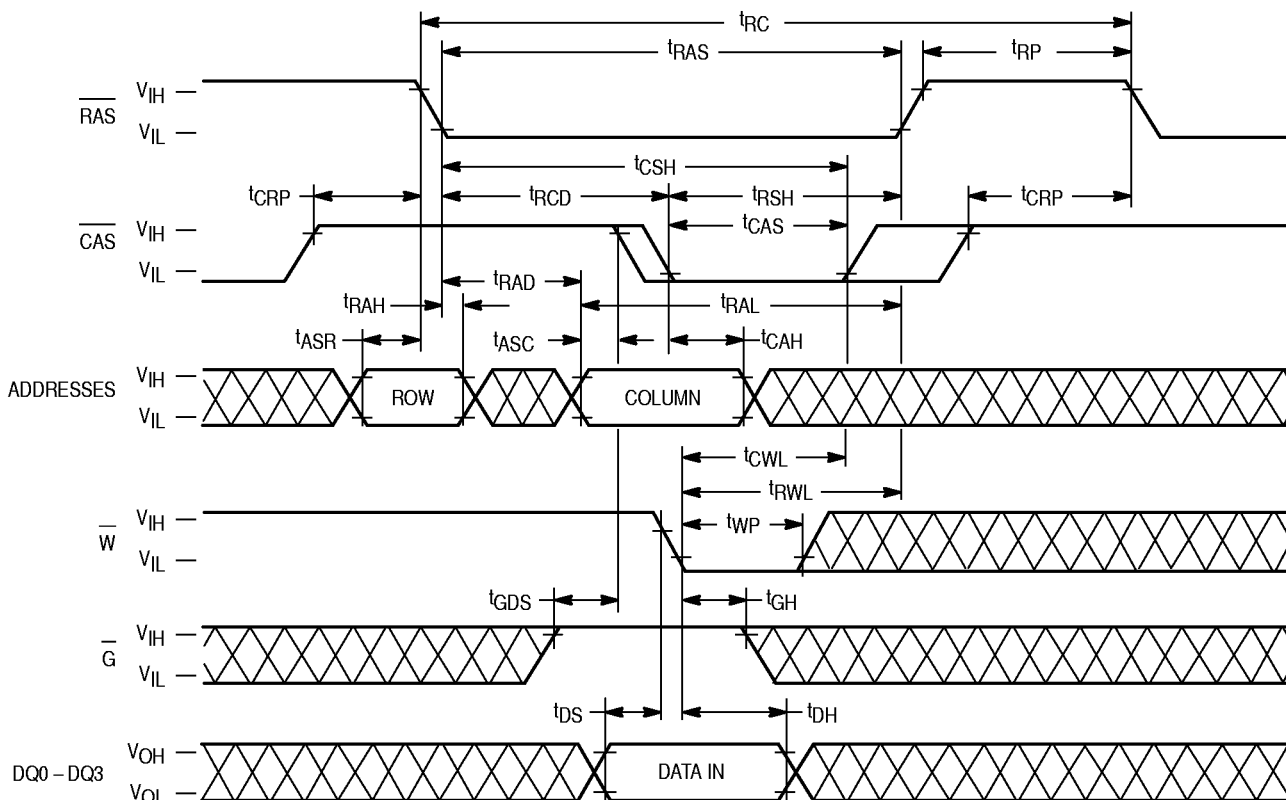
READ CYCLE (G CONTROLLED READ)



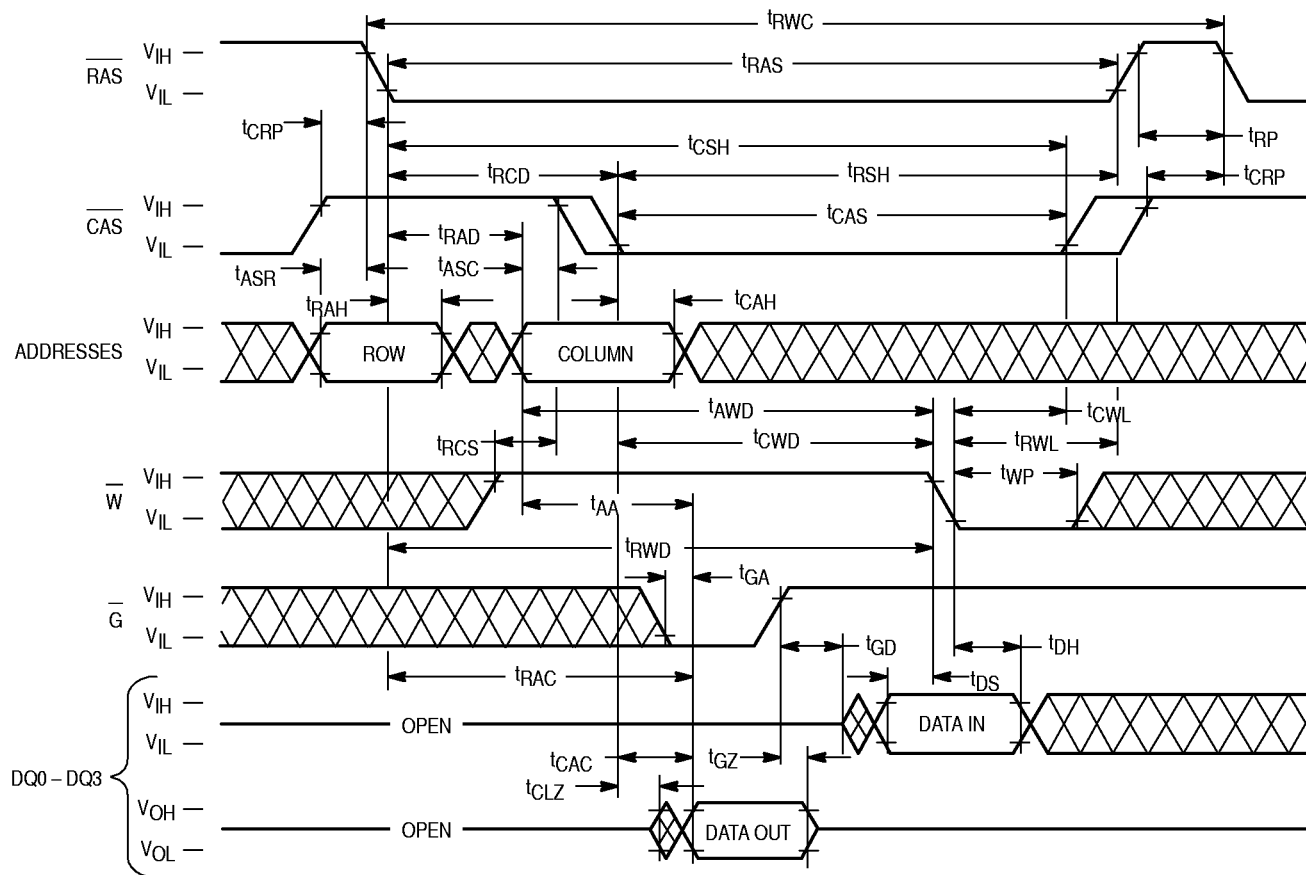
WRITE CYCLE (EARLY WRITE)



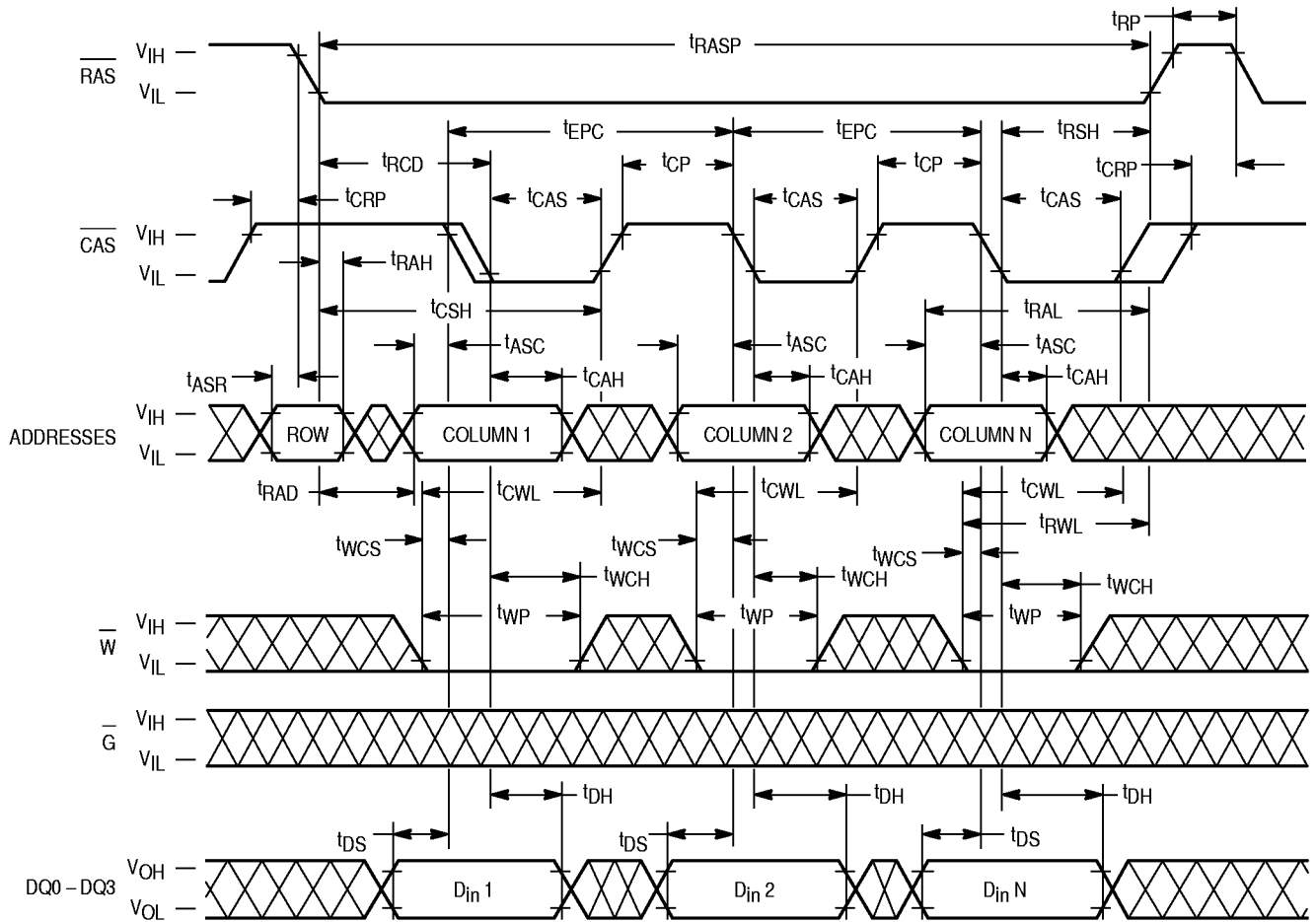
WRITE CYCLE (\bar{G} CONTROLLED WRITE)



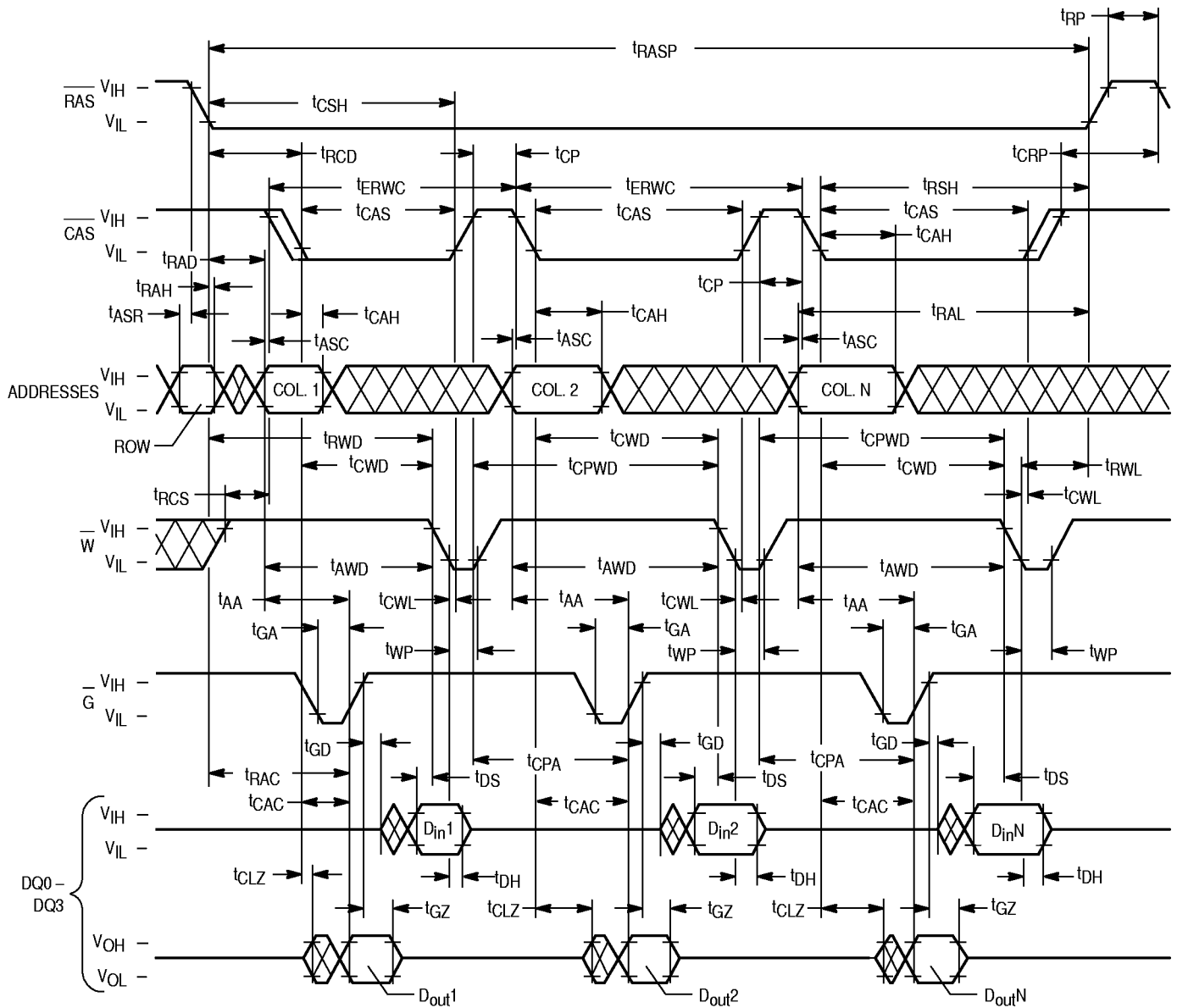
READ-WRITE CYCLE



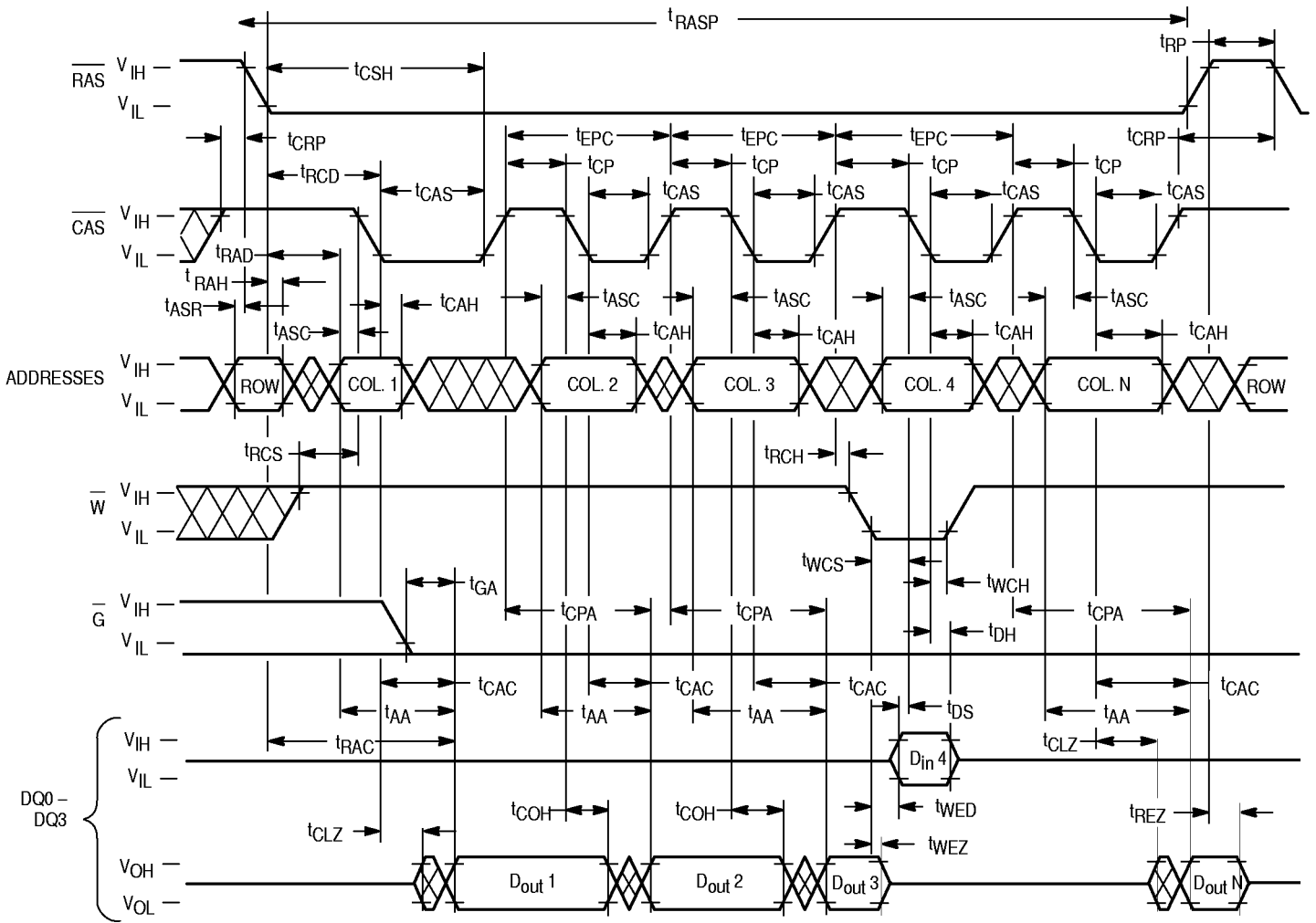
EXTENDED DATA OUT WRITE CYCLE (EARLY WRITE)



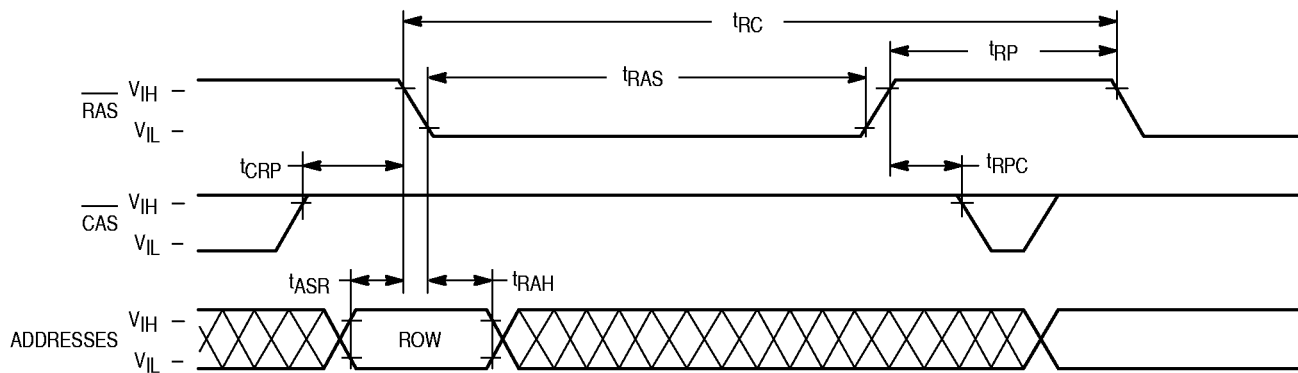
EXTENDED DATA OUT READ-WRITE CYCLE



EXTENDED DATA OUT READ WRITE MIXED CYCLE

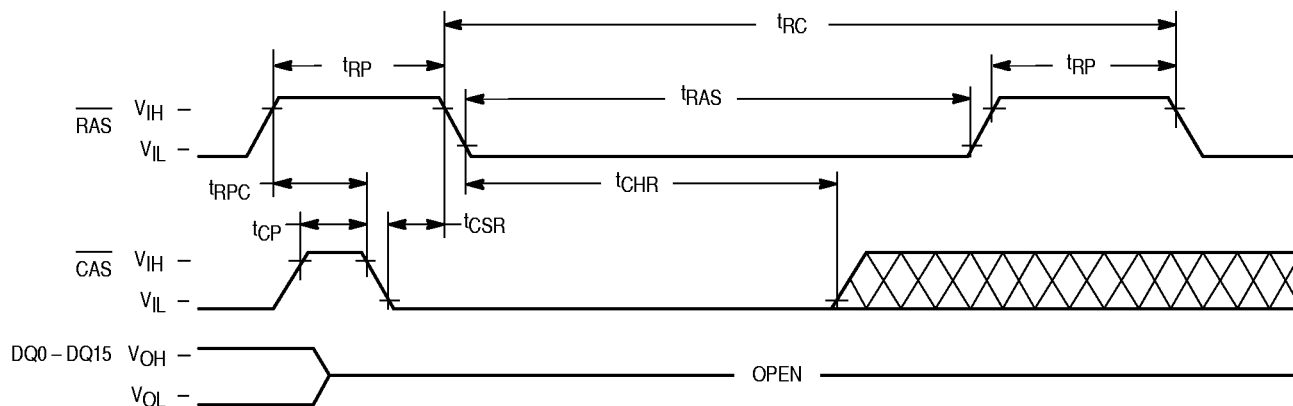


RAS-ONLY REFRESH CYCLE



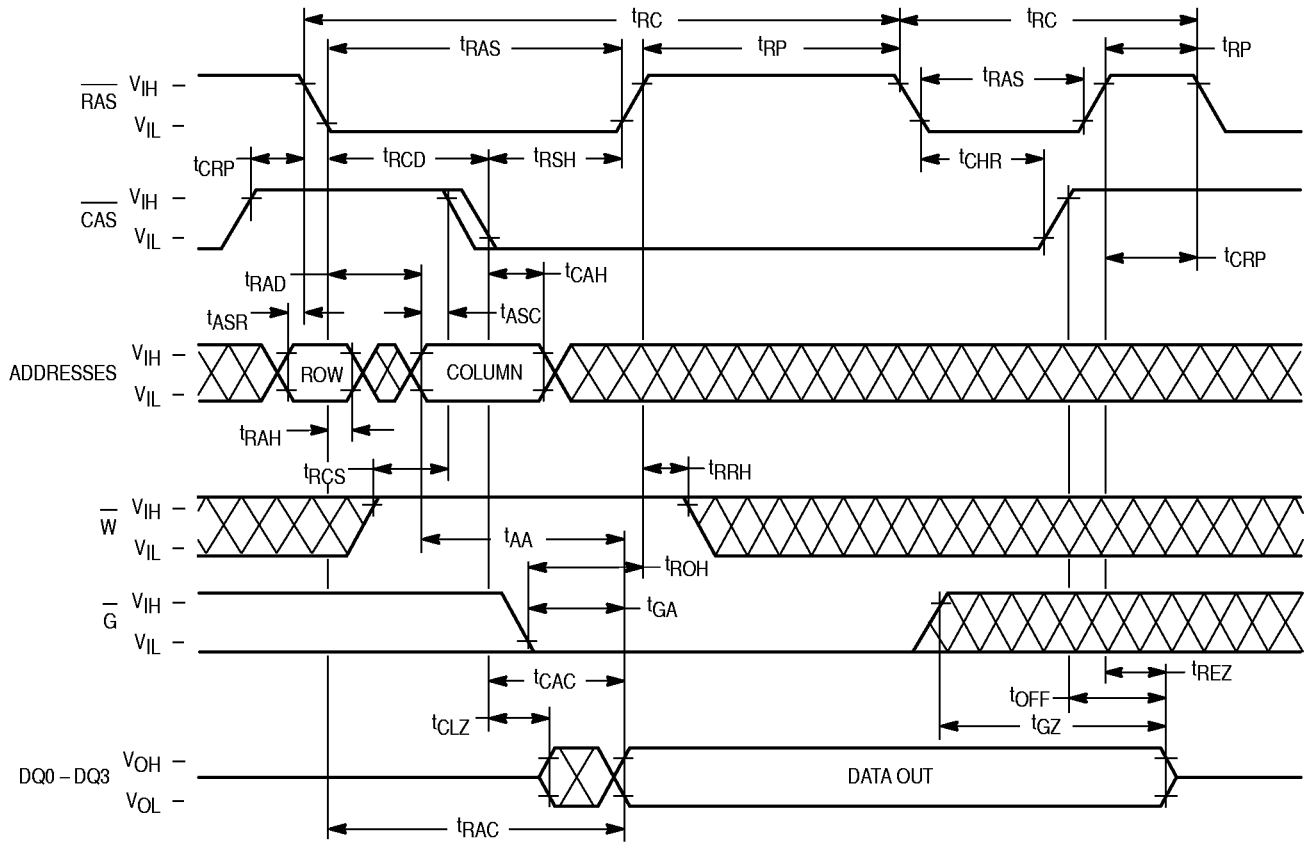
NOTE: \overline{W} , \overline{G} = H or L
 DQ0 - DQ3 = Open

CAS BEFORE RAS REFRESH CYCLE

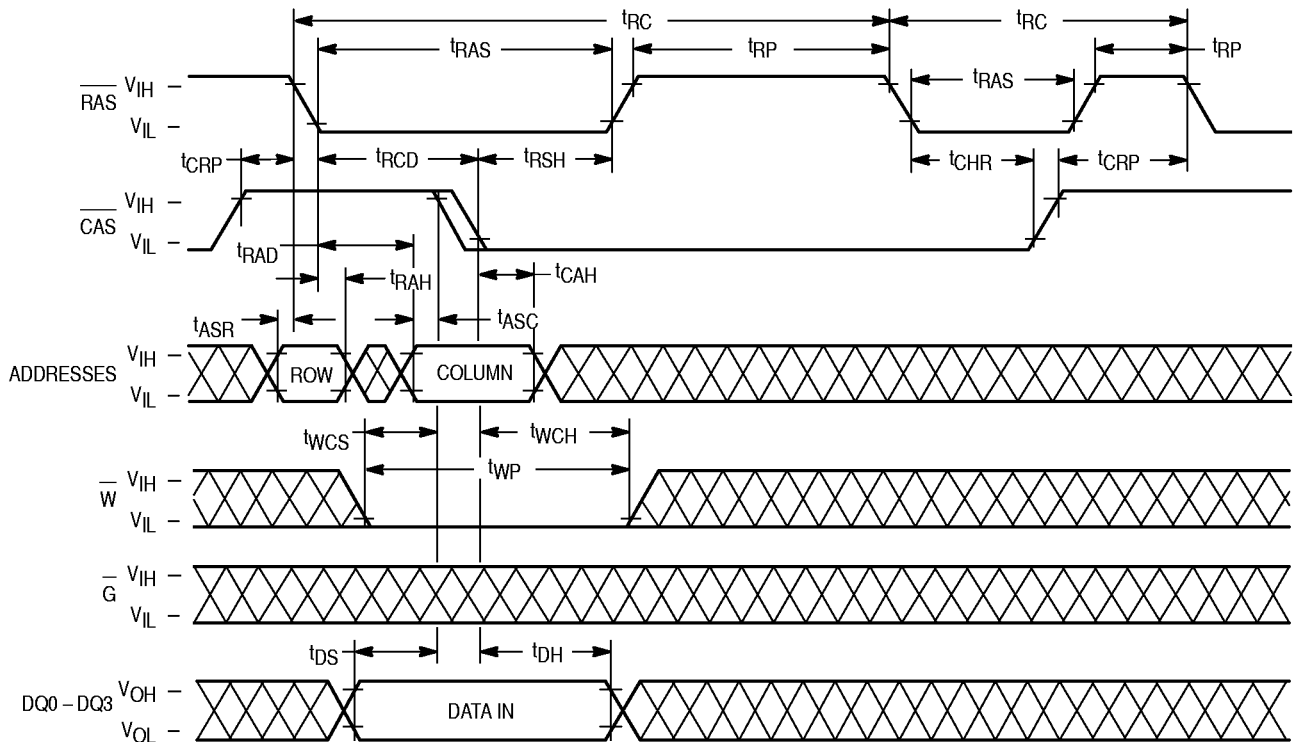


NOTE: \overline{W} , \overline{G} , Addresses = H or L

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

MCM317405C: The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 11-bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 four bit word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL} , t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the 16M DRAM Family per device: RAS-only refresh cycle, CAS before RAS refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, extended data out read cycle, read-write cycle, and extended data out read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS or active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read

access time of the device is independent of the address multiplex window.

Both CAS and output enable (\bar{G}) control read access time: CAS must be active before or at t_{RCD} maximum and \bar{G} must be active $t_{RAC}-t_{GA}$ (both minimum) after RAS active transition to guarantee valid data out (Q) at t_{RAC} . If the t_{RCD} maximum is exceeded and/or \bar{G} active transition does not occur in time, read access time is determined by either the CAS or \bar{G} clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, extended data out early write, and extended data out read-write. Early and late write modes are discussed here, while extended data out write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early and late write modes are distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS} , and precharge time t_{RP} , apply to write mode, as in the read mode.

An early write cycle is characterized by \bar{W} active transition at minimum time t_{WCS} before CAS active transition. Column address setup and hold times (t_{ASC} , t_{CAH}) and data in (D) setup and hold times (t_{DS} , t_{DH}) are referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL} , respectively, after the start of the early write operation to complete the cycle.

A late-write cycle (referred to as \bar{G} -controlled write) occurs when W active transition is made after CAS active transition. W active transition could be delayed for almost 10 microseconds after CAS active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) $\leq t_{RAS}$, if other timing minimums (t_{RCD} , t_{RWL} , and t_T) are maintained. D timing parameters are referenced to W active transition in a late write cycle. Output buffers are enabled by CAS active transition. 4M x 4 outputs are switched off by \bar{G} inactive transition, which is required to write to the device. Q may be indeterminate (see note 12 of AC Operating Conditions table). RAS and CAS must remain active for t_{RWL} and t_{CWL} , respectively, after W active transition to complete the write cycle. \bar{G} (4M x 4) devices must remain inactive for t_{GH} after W active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except W must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations on a selected row of the 16M DRAM family. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC} . Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL} . The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP} , while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP} . Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically refreshed (recharged) to maintain the correct bit state. Refresh time for the MCM317405C is 32 milliseconds.

This is accomplished by cycling through the 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 16M DRAM device family. Burst refresh, a refresh of all rows consecutively, must be performed every 32 milliseconds on the MCM317405C.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decodes. Three other methods of refresh, **RAS-only refresh**, **CAS before RAS refresh**, and **hidden refresh** are available on this device for greater system flexibility.

RAS-Only Refresh

RAS-only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a test mode cycle.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

TEST MODE

The internal organization of the MCM317405C allows the device to be tested as if it were a 1M x 16 DRAM. In Test Mode operation, column addresses A1 and A0 are ignored. During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same. See Test Mode block diagram.

W, CAS before RAS timing puts the device in Test Mode, as shown in the test mode timing diagram. A CAS before RAS refresh cycle or a RAS only refresh cycle places the device back in normal mode. Refresh is performed in test mode by using a W, CAS before RAS refresh cycle which uses the internal refresh address counter.

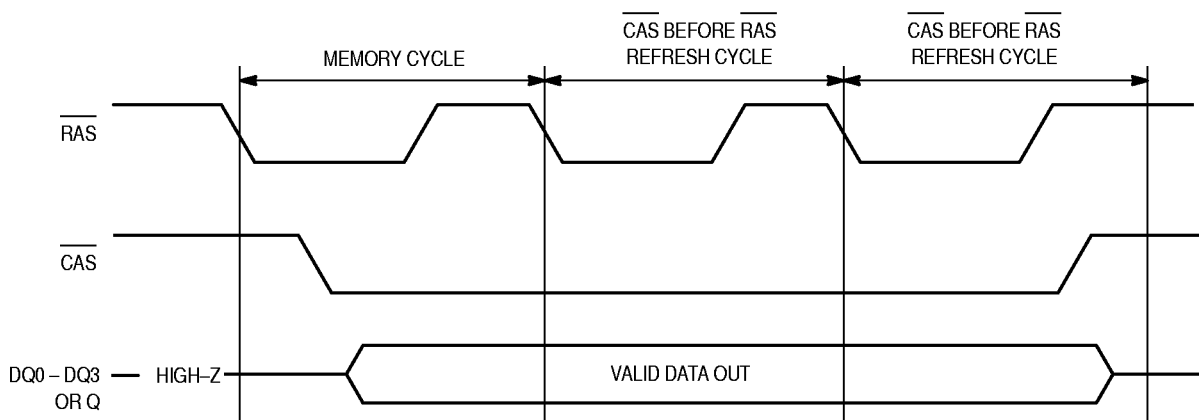
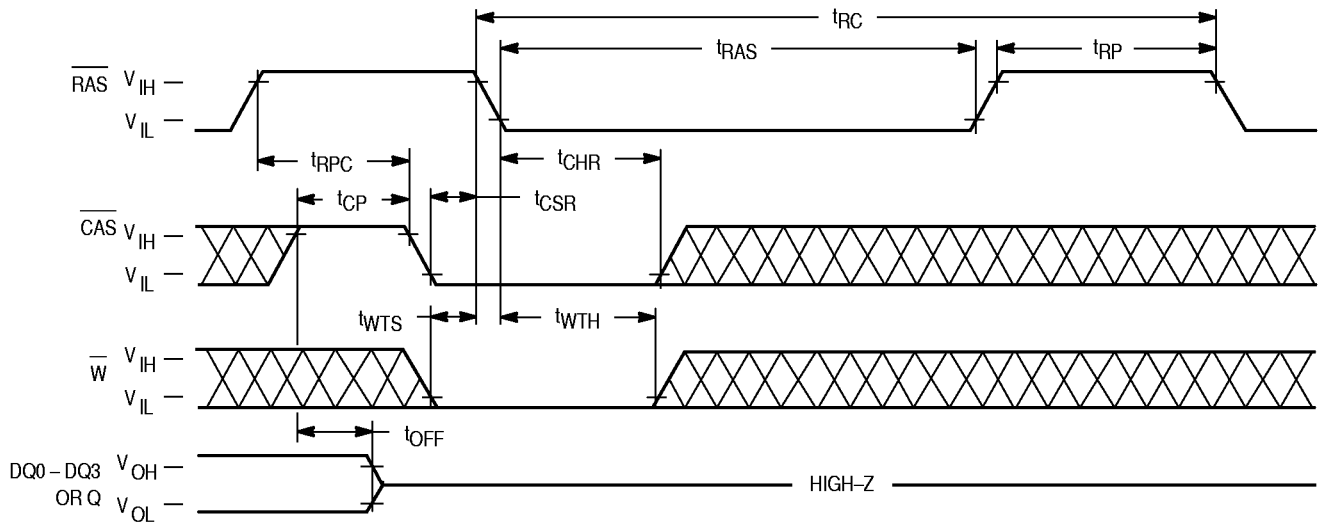


Figure 1. Hidden Refresh Cycle

TEST MODE TIMING DIAGRAMS

WRITE OR CAS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY) (G and A0 – A10 or 11 are Don't Care)



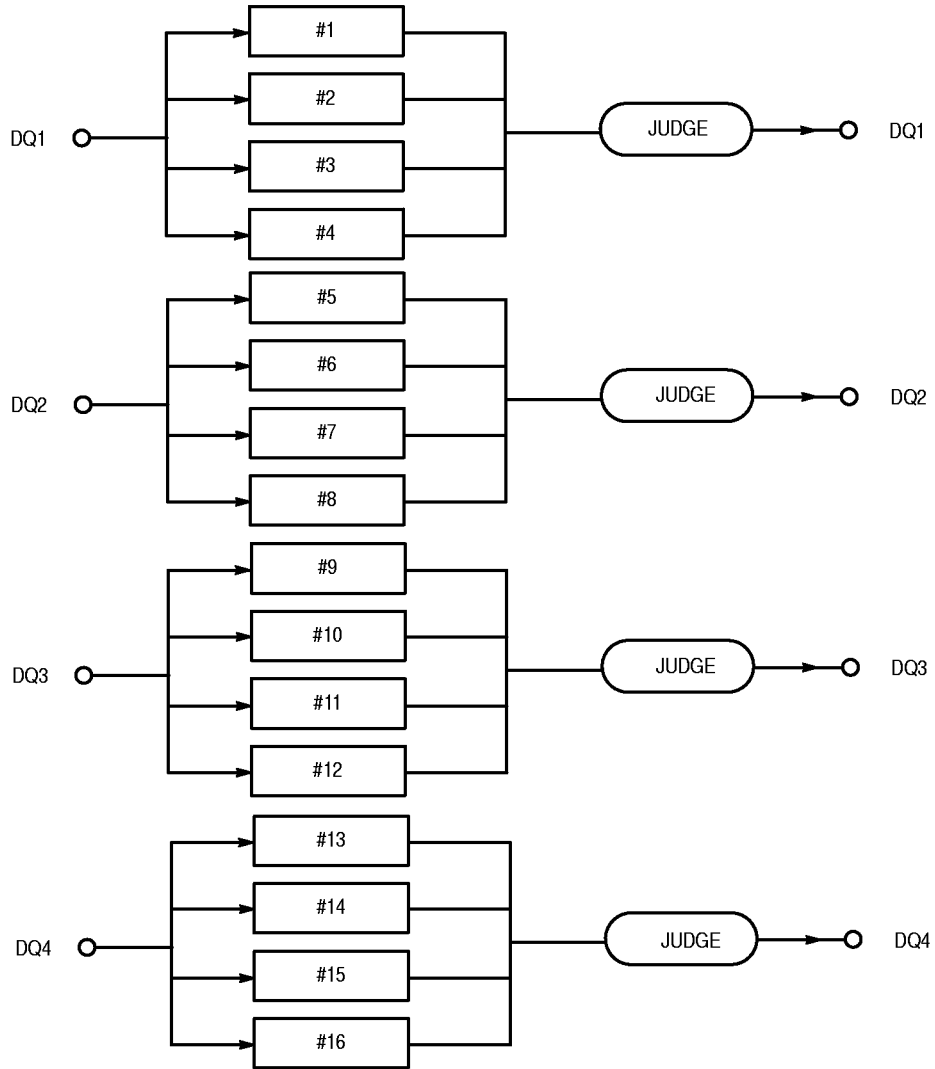
NOTE: Once the device is put into Test Mode with the Test Mode Entry Cycle, any of the standard cycles (Read, Write, Extended Data Out, etc.) may be used to test the part. The timing diagrams previously presented are valid for all cycles performed in Test Mode.

MODE DEPENDENT ON CAS AND W WHEN RAS FALLS

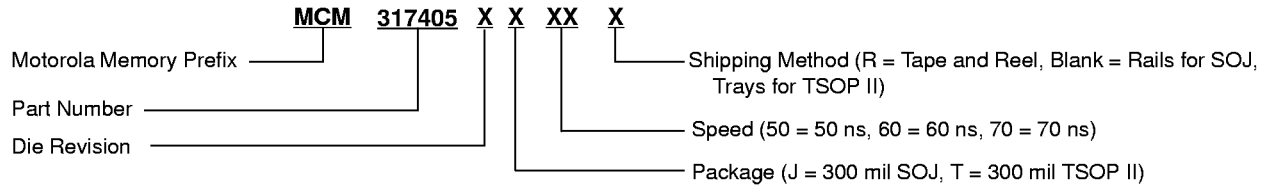
Mode	CAS	W*
Read, Write, RMW, FPM	1	0
CBR Refresh, Test Mode Exit	0	1
Test Mode Entry	0	0

*Logic state when RAS transitions low.

TEST MODE BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)

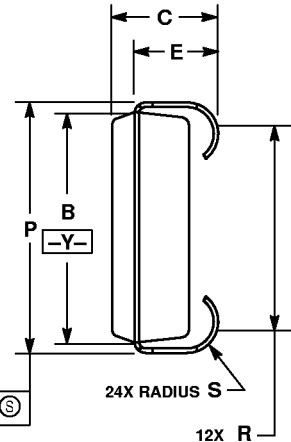
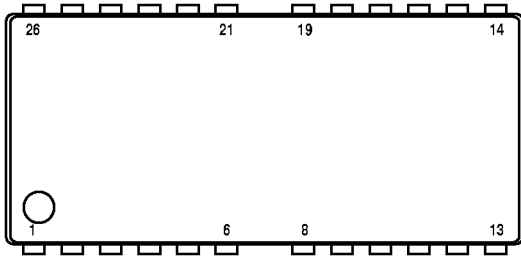


16M DEVICE NUMBERS

MCM317405CJ50	MCM317405CT50
MCM317405CJ60	MCM317405CT60
MCM317405CJ70	MCM317405CT70
MCM317405CJ50R	MCM317405CT50R
MCM317405CJ60R	MCM317405CT60R
MCM317405CJ70R	MCM317405CT70R

PACKAGE DIMENSIONS

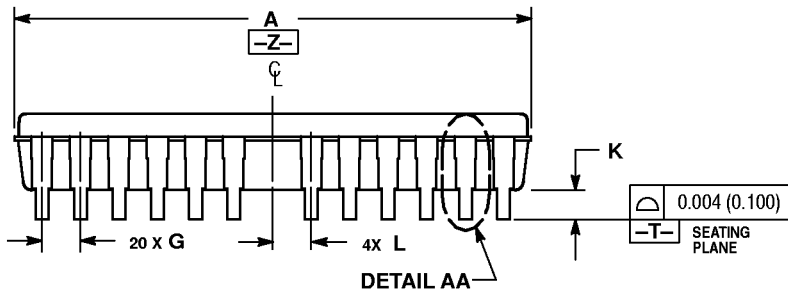
J PACKAGE
300 MIL SOJ
CASE 880A-02



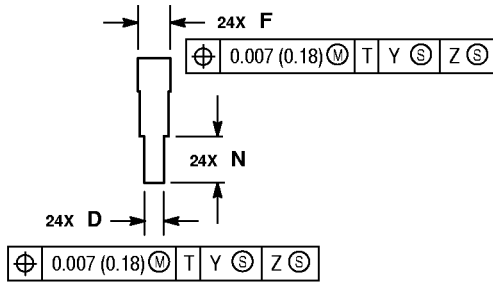
$\oplus 0.007 (0.18) \text{M T Y S Z S}$

$\oplus 0.007 (0.18) \text{M T Y S Z S}$

NOTE 3



DETAIL AA

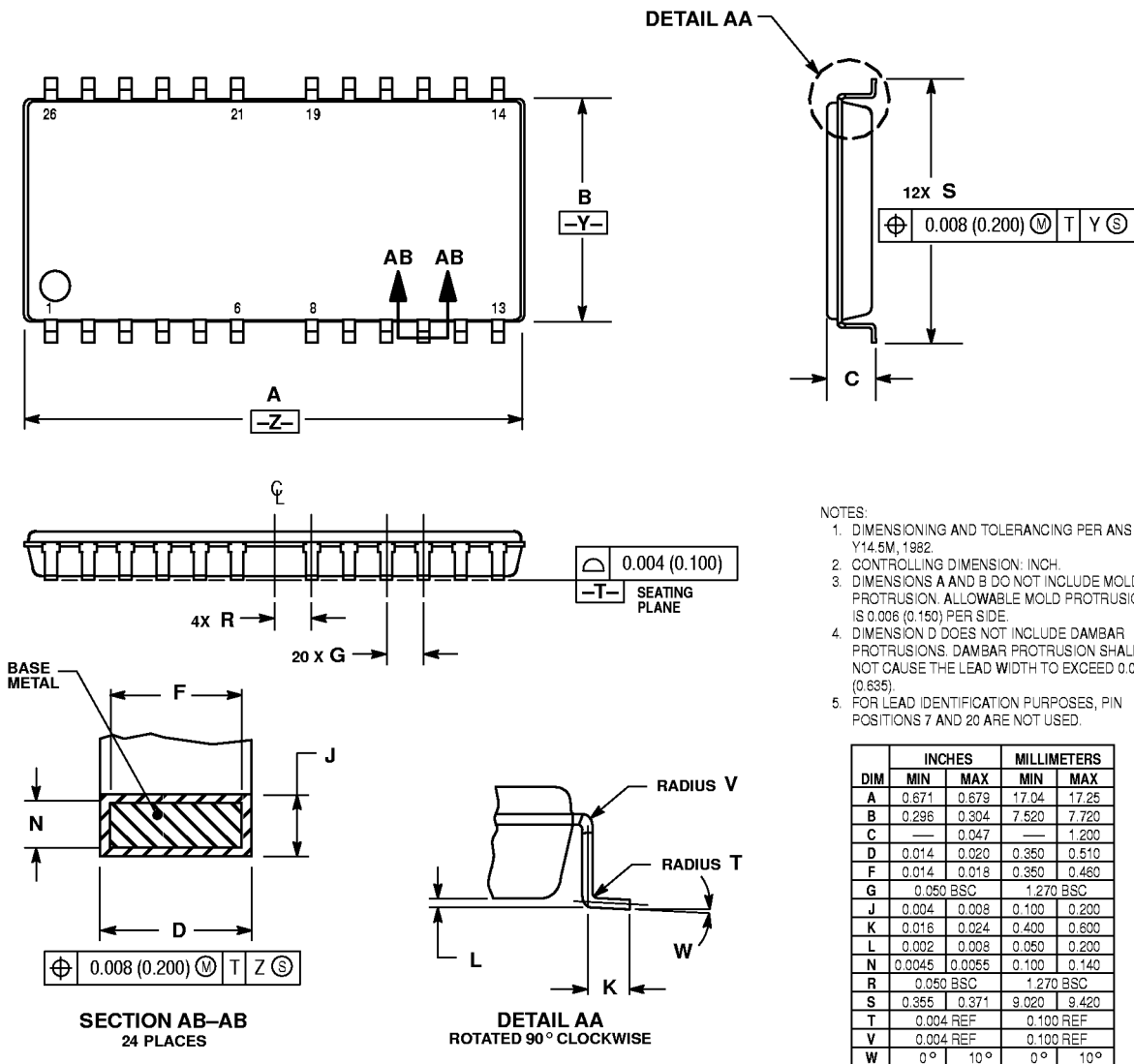


NOTE 3
 DETAIL AA

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. TO BE DETERMINED AT PLANE -T-
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.008 (0.160) PER SIDE.
 5. DIMENSIONS A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
 6. DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE F DIMENSION TO EXCEED 0.037 (0.94).
 7. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 7 AND 20 ARE NOT USED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.670	0.680	17.01	17.28
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.38	0.51
E	0.103	0.116	2.62	2.95
F	0.026	0.032	0.66	0.81
G	0.050 BSC		1.270 BSC	
K	0.031	0.045	0.80	1.14
L	0.050 BSC		1.270 BSC	
N	0.035	0.045	0.89	1.14
P	0.328	0.340	8.35	8.63
R	0.260	0.275	6.61	6.99
S	0.030	0.040	0.77	1.01

T PACKAGE
300 MIL TSOP II
CASE 892A-02



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.006 (0.150) PER SIDE.
 4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.025 (0.635).
 5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 7 AND 20 ARE NOT USED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.671	0.679	17.04	17.25
B	0.296	0.304	7.520	7.720
C	—	0.047	—	1.200
D	0.014	0.020	0.350	0.510
F	0.014	0.018	0.350	0.460
G	0.050 BSC		1.270 BSC	
J	0.004	0.008	0.100	0.200
K	0.016	0.024	0.400	0.600
L	0.002	0.008	0.050	0.200
N	0.0045	0.0055	0.100	0.140
R	0.050 BSC		1.270 BSC	
S	0.355	0.371	9.020	9.420
T	0.004 REF		0.100 REF	
V	0.004 REF		0.100 REF	
W	0°	10°	0°	10°

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