

63RS1681

2048x8 Registered PROM with Synchronous Enable

53/63RS1681 53/63RS1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (TIW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™)
11 Inputs, 8 Registered Outputs, 2048 product terms

Description

The 53/63RS1681 and 53/63RS1681A are 2Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous enable inputs and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous (\overline{ES}) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous enable inputs. Outputs may be set to the high impedance state by setting \overline{ES} HIGH before the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (\overline{IS}) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A10-A4). With all \overline{IS} column words (A3-A0) programmed to the same pattern, the \overline{IS} function will be independent of both row and column addressing and may be used as a single pin control. With all \overline{IS} words programmed HIGH a PRESET function is performed. The unprogrammed state of \overline{IS} words are LOW, presenting a CLEAR with \overline{IS} pin LOW.

Selection Guide

MEMORY		PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE		0°C to +75°C	-55°C to +125°C
16 K	2048x8	24 (28)	NS,JS, W, (NL),(L)	Enhanced	63RS1681A	53RS1681A
				Standard	63RS1681	53RS1681

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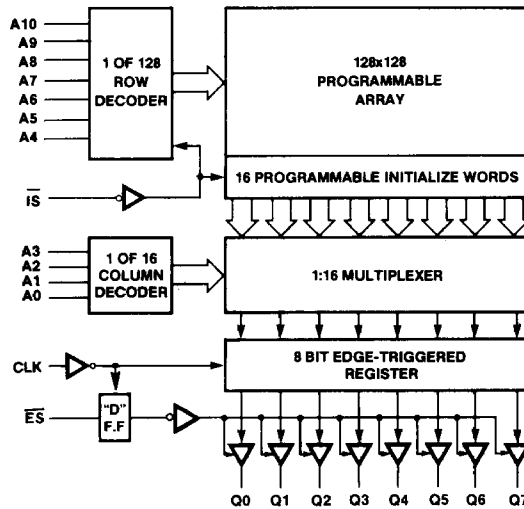
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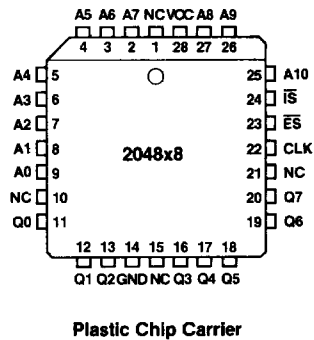
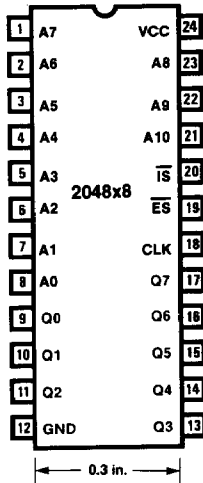
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Block Diagram



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Pin Configurations



Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7 V	12 V
Input voltage	-1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY		COMMERCIAL		UNIT				
			53RS1681A	53RS1681	63RS1681A	63RS1681					
			MIN	MAX	MIN	MAX					
t_w	Width of clock (high or low)	10	20	20	20	20	ns				
$t_{s(A)}$	Setup time from address to clock	28	40	45	35	40	ns				
$t_{s(\overline{ES})}$	Setup time from \overline{ES} to clock	7	15	15	15	15	ns				
$t_{s(\overline{IS})}$	Setup time from \overline{IS} to clock	20	30	35	25	30	ns				
$t_h(A)$	Hold time address to clock	-5	0	0	0	0	ns				
$t_h(\overline{ES})$	Hold time \overline{ES}	-3	5	5	5	5	ns				
$t_h(\overline{IS})$	Hold time \overline{IS}	-5	0	0	0	0	ns				
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	-55	125	-55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.2	V
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$			0.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$	Com $I_{OH} = -3.2 \text{ mA}$ Mil $I_{OH} = -2 \text{ mA}$	2.4			V
I_{OZL}	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	align="center"> μA
I_{OZH}			$V_O = 2.4 \text{ V}$			40	
I_{OS}	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$	-20		-90	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$. All inputs TTL. All outputs open.			140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25°C T_A .

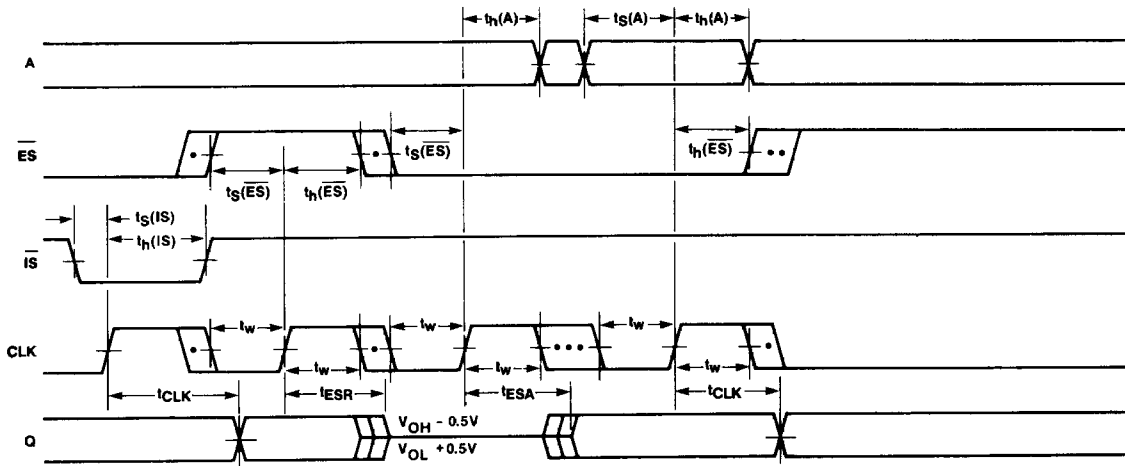
Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY		COMMERCIAL		UNIT
			53RS1681A	53RS1681	63RS1681A	63RS1681	
			MIN	MAX	MIN	MAX	
t _{CLK}	Clock to output Delay	10	20	25	15	20	ns
t _{ESA}	Clock to output access time (\overline{ES})	15	30	35	25	30	ns
t _{ESR}	Clock to output recovery time (\overline{ES})	15	30	35	25	30	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

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Definition of Waveforms



- Notes:
1. Input pulse amplitude 0 V to 3.0 V.
 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 3. Input access measured at the 1.5 V level.
 4. Switch S₁ is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
 5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.
t_{ER} and t_{ESR} are tested with C_L = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} - 0.5 V output level; S₁ is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.