MC54/74HC4511

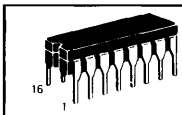
BCD-to-Seven-Segment Latch/ Decoder/Display Driver

High-Performance Silicon-Gate CMOS

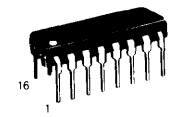
The MC54/74HC4511 is identical in pinout to the MC14511 metal-gate CMOS decoder/driver. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC4511 provides the functions of a 4-bit storage latch, a BCD-to-seven-segment decoder, and a display driver. It can be used either directly or indirectly with seven-segment light-emitting diode (LED), incandescent, fluorescent, gas discharge, or liquid-crystal readouts. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn off or pulse modulate the brightness of the display, and to store a BCD code, respectively.

- Latch Storage of BCD Inputs
- Blanking Input
- Lamp Test Input
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

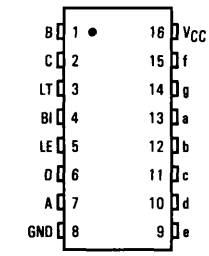
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

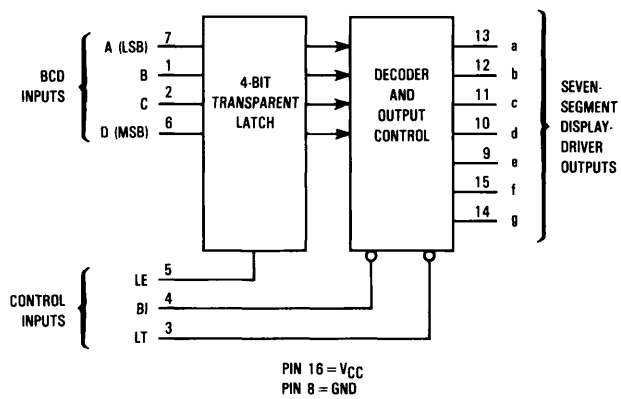
MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXD	SOIC

T_A = −55° to 125°C for all packages.
Dimensions in Chapter 6.

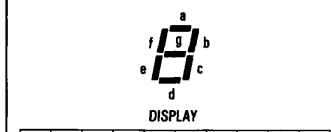
PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±70	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	V_{CC}=2.0 V	0	1000	ns
		V_{CC}=4.5 V	0	500	
		V_{CC}=6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25°C to −55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V, $\|I_{out}\| \le 20\ \mu A$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V, $\|I_{out}\| \le 20\ \mu A$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL}, $\|I_{out}\| \le 20\ \mu A$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		$V_{in}=V_{IH}$ or V_{IL}, $\|I_{out}\| \le 6.0$ mA	4.5	3.98	3.84	3.70	
		$V_{in}=V_{IH}$ or V_{IL}, $\|I_{out}\| \le 7.8$ mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in}=V_{IH}$ or V_{IL}, $\|I_{out}\| \le 20\ \mu A$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		$V_{in}=V_{IH}$ or V_{IL}, $\|I_{out}\| \le 4.0$ mA	4.5	0.26	0.33	0.40	
		$V_{in}=V_{IH}$ or V_{IL}, $\|I_{out}\| \le 5.2$ mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in}=V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in}=V_{CC}$ or GND, $I_{out}=0\ \mu A$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A, B, C, or D to Output (Figures 1 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Output (Figures 2 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Blanking Input to Output (Figures 3 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Lamp Test to Output (Figures 4 and 6)	2.0 4.5 6.0	600 120 102	750 150 129	900 180 153	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 70	pF

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, Input A, B, C, or D to Latch Enable (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Latch Enable to Input A, B, C, or D (Figure 5)	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 4.

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SWITCHING WAVEFORMS

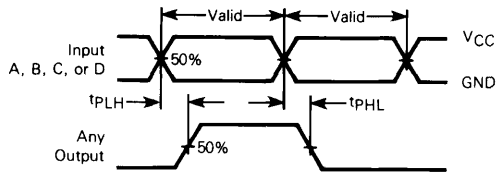

Figure 1.

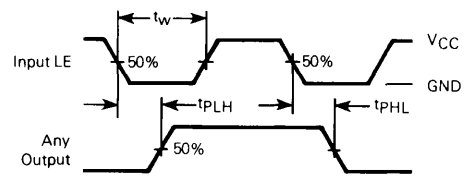

Figure 2.

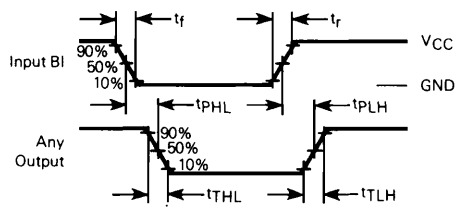

Figure 3.

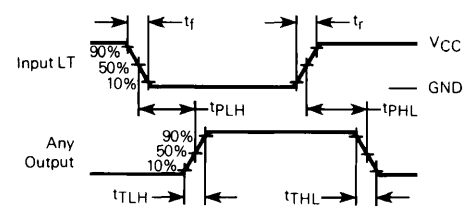

Figure 4.

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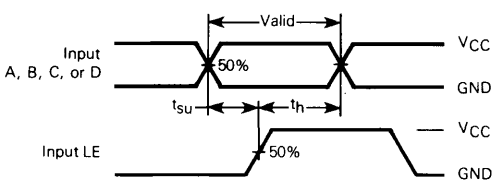
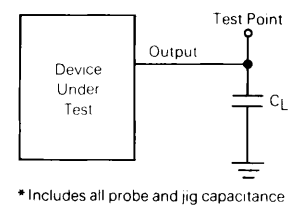


Figure 5.



* Includes all probe and jig capacitance

Figure 6. Test Circuit

FUNCTION TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X	*							*

* = Depends upon the BCD code previously applied while LE was at a low level.

PIN DESCRIPTIONS

INPUTS

A, B, C, D (PINS 7, 1, 2, 6) — BCD inputs. A (pin 7) is the least significant bit and D (pin 6) is the most significant bit. Hexadecimal code A-F at these inputs causes the outputs to assume a low level, offering an alternate method of blanking the display.

OUTPUTS

a, b, c, d, e, f, g (PINS 13, 12, 11, 10, 9, 15, 14) — Decoded, buffered seven-segment display-driver outputs. These outputs, unlike the MC14511, have CMOS drivers, which produce typical CMOS output voltage levels. These outputs are connected to various displays as shown in Figure 7.

CONTROL INPUTS

BI (PIN 4) — Active-low display blanking input. A low level on this input will cause all outputs to be held low, thereby blanking the display. LT is the only input that overrides the BI input.

LT (PIN 3) — Active-low lamp test. A low level on this input causes all outputs to assume a high level. This input allows the user to test all segments of a display with a single control input. This input is independent of all other inputs.

LE (PIN 5) — Latch enable input. This input controls the 4-bit transparent latch. A high level on this input latches the code present at the A, B, C and D inputs; a low level allows the code to be transmitted through the latch to the decoder.

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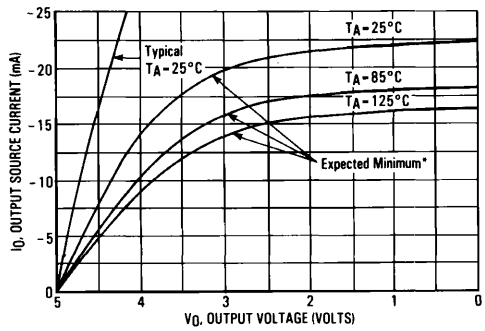
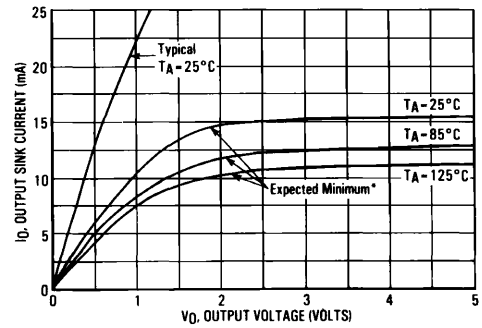
OUTPUT CHARACTERISTIC CURVES (V_{CC} = 5 V)

SOURCE CURRENT

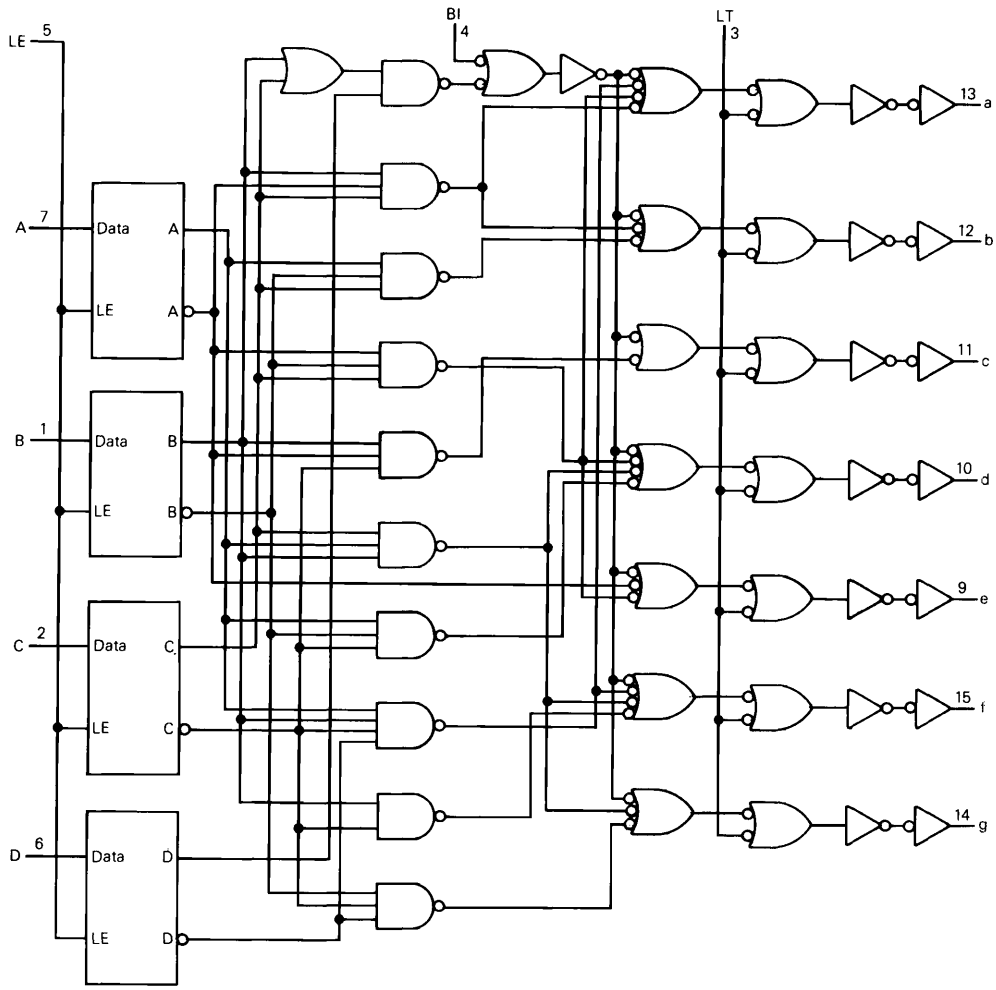


SINK CURRENT



* The expected minimum curves are not guarantees, but are design aids.

EXPANDED LOGIC DIAGRAM



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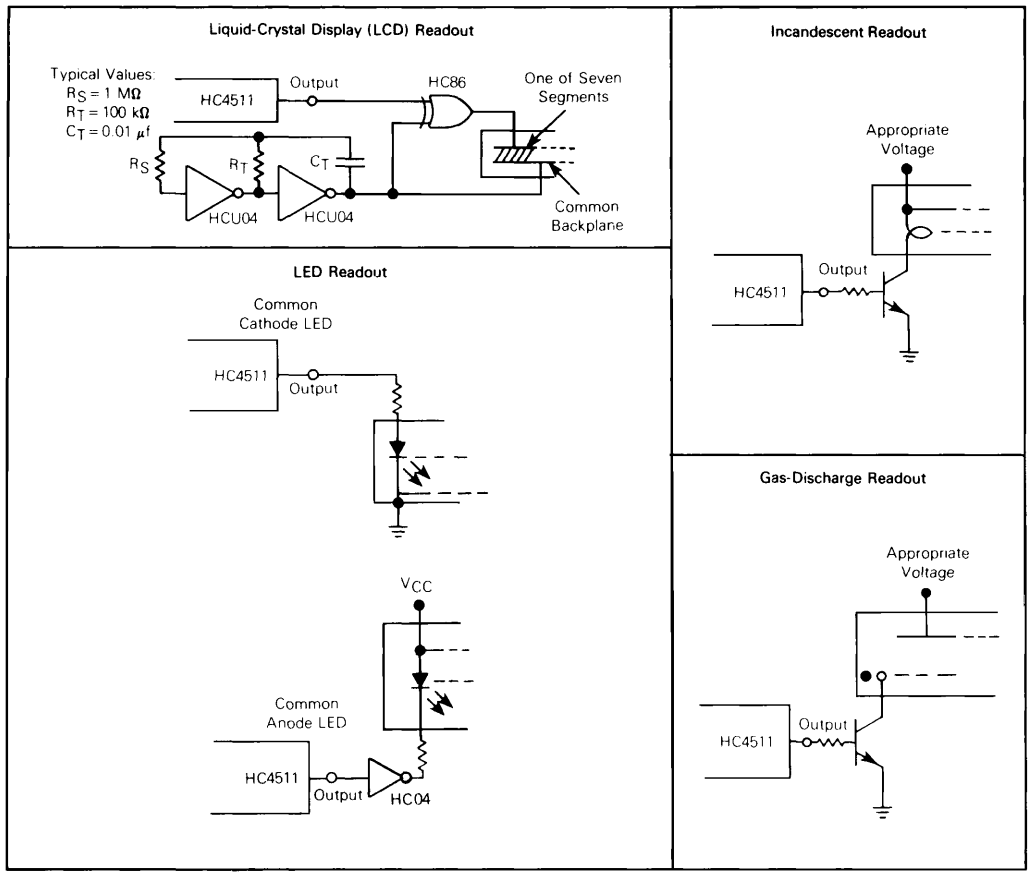

Figure 7. Connections to Various Display Readouts

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