

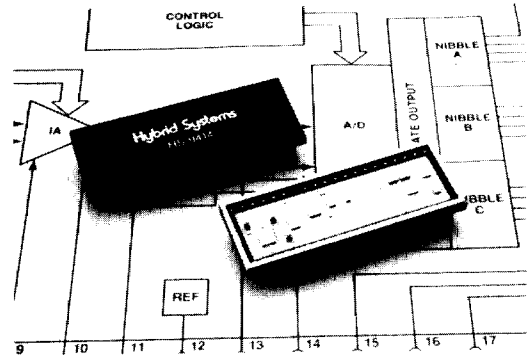
# SOFTWARE PROGRAMMABLE, 12-BIT, DATA ACQUISITION SYSTEM (DAS)

## FEATURES

- MUX, inst. amp, S/H, A/D in a compact 40-pin DIP
- Software programmable gain instrumentation amplifier (SPGIA)
- Input and output offset adjust
- 126 dB dynamic range

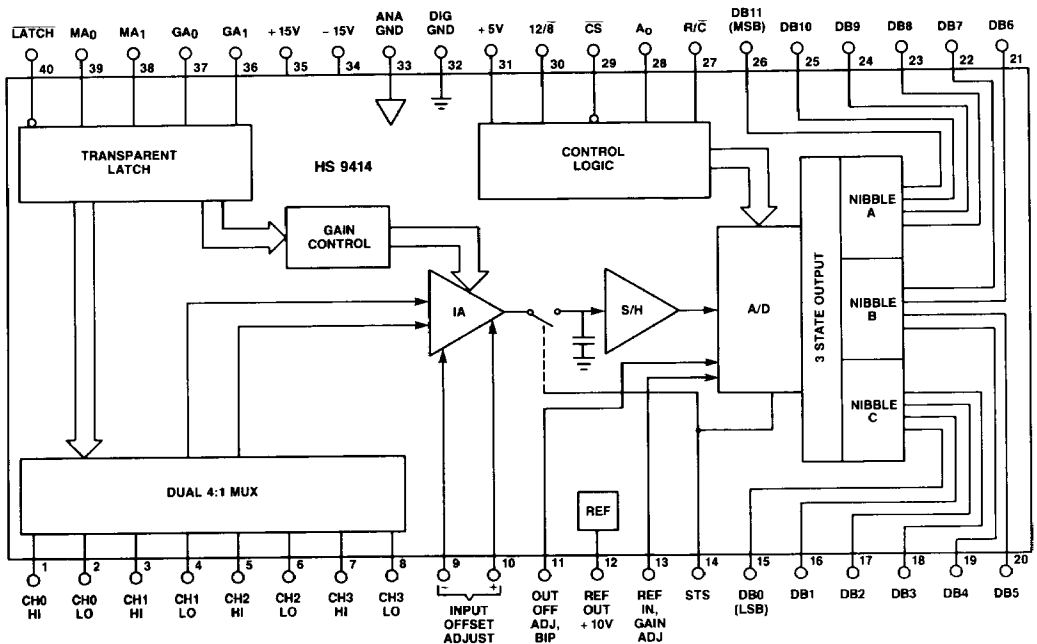
## DESCRIPTION

The HS9414 provides complete 12-bit data acquisition functionality in a 40-pin DIP. The HS9414 includes a 4-channel differential input multiplexer, a software programmable instrumentation amplifier, a sample and hold circuit and the HS574A, 12-bit, 25 $\mu$ sec A/D converter. Specifications are guaranteed for the complete system instead of for each individual component.



The HS9414 is offered in a ceramic package for commercial (0°C to +70°C) and military (-55°C to +125°C) applications with processing available in full compliance with MIL-STD-883C.

## FUNCTIONAL DIAGRAM



11

# SPECIFICATIONS

(Typical @ +25°C, V<sub>CC</sub> = +15V, V<sub>EE</sub> = -15V, V<sub>LOGIC</sub> = +5V unless otherwise specified)

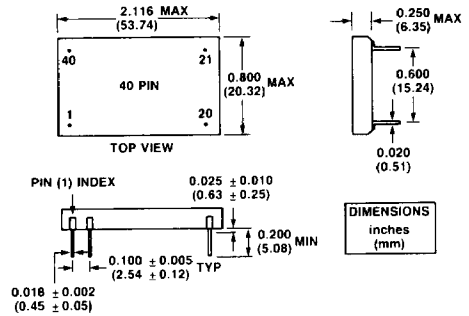
MODEL	HS 9414
<b>ANALOG INPUTS</b>	
Number of Inputs	4 Differential
Input Voltage Range (G = 1) <sup>1</sup>	0 to +10V or ±5V
Unipolar (-1)	±10V
Bipolar (-2)	$\pm(11 - \frac{V_{IN\ Diff} \times Gain}{2})$
Common Mode Voltage Range	$\pm(\frac{2(10 -  CMV_i )}{Gain})$
Differential Mode Voltage Range	$\pm(\frac{2(10 -  CMV_i )}{Gain})$
Input Offset Voltage (Unipolar) <sup>2</sup>	
G = 1	±0.5 LSB
G = 10	±100 μV
G = 100	±50 μV, 250 μV max
G = 500	±50 μV, 250 μV max
Input CH to CH Offset Voltage	2 μV
CMRR	
G = 1	-80 dB typ, -76 dB max
G = 10	-100 dB typ, -90 dB max
G = 100, G = 500	-120 dB typ
Input Dynamic Range	126 dB
Input Bias Current	60 nA
Input Resistance	1 GΩ
Input Capacitance	25 pF
Input Offset Current	60 nA
Input Noise Voltage	2 μV RMS, 10 μV p-p @G=500
<b>DIGITAL INPUTS</b>	
Logic Inputs	
CS, R/C, A <sub>D</sub> , 12/B	+2.0V min, +5.5V max
Logic '1'	-0.5V min, +0.8V max
Logic '0'	±50 A max
Current	5 pF
Capacitance	Hardwire to V <sub>LOGIC</sub> or DIG COM
Control Input, 12/B	
CS-Negative	120 nsec
R/C-Negative	120 nsec
LATCH	33 nsec
Data Set-Up Time	33 nsec
MA0, MA1, GA0, GA1	
Fan-Out	1 TTL Load
<b>SIGNAL DYNAMICS</b>	
A/D Conversion Time	25 μsec typ, 30 μsec max
System Throughput Rate <sup>2</sup>	
G = 1, 10 (0.01% Settling Accuracy)	28.6 kHz max
G = 100 (0.015% Settling Accuracy)	17 kHz max
G = 500 (0.02% Settling Accuracy)	10 kHz typ
Gain Switching Time and 1A Settling Time	
G = 1, 10	10 μsec typ
G = 100	50 μsec typ
G = 500	90 μsec typ
Amplifier Bandwidth (-3 dB)	
G = 1	3 mHz
G = 10	2.5 mHz
G = 100	100 kHz
G = 500	20 kHz
SIH Acquisition Time to 0.01%	10 μsec max
SIH Aperture Jitter	50 psec typ
SIH Feedthrough	76 dB
Crosstalk (V <sub>IN</sub> = 20V p-p sine wave)	-78 dB @40 kHz -90 dB @0.5 kHz
<b>ACCURACY</b>	
Integral Linearity	
HS 9414C (0°C to +70°C)	±½ LSB max
HS 9414B (0°C to +70°C)	±½ LSB max
(MIN to MAX)	±1 LSB max
Differential Linearity	
HS 9414C (0°C to +70°C)	±¼ LSB typ, ±1 LSB max
HS 9414B (0°C to +70°C)	±¼ LSB typ, ±1 LSB max
(MIN to MAX)	±¼ LSB typ, ±1 LSB max
No Missing Codes	
12-Bits	0°C to 70°C
11-Bits	-55°C to +125°C
Total Gain Error @G = 1 <sup>3</sup>	0.1% typ, 0.3% max
@other gains referred to G = 1	
G = 10	0.02% typ, 0.1% max
G = 100	0.03% typ, 0.1% max
G = 500	0.05% typ
Bipolar Offset <sup>3</sup>	±1 LSB typ, ±3 LSB max
MIN to MAX	15 LSB max
<b>DRIFT</b>	
Integral Nonlinearity	±2 ppm/°C
Differential Nonlinearity	±2 ppm/°C
Unipolar Output Offset	±10 ppm/°C
Bipolar Output Offset	±10 ppm/°C
Gain Tempco G = 1	±25 ppm/°C
<b>REFERENCE</b>	
Output Voltage	10.00V nominal, ±0.1V max
Tempco	±30 ppm/°C typ, ±50 ppm/°C max
Output Current:	1.5 mA

MODEL	HS 9414
<b>POWER REQUIREMENTS</b>	
Power Supply Range	±15V, ±5%
PSSR (All Supplies) %FSR/% Supply	0.002%/9% typ, 0.005%/9% max
Current Drain	
+15V	22 mA typ, 27 mA max
-15V	10 mA typ, 15 mA max
+5V	2 mA typ, 5 mA max
Power Dissipation	490 mW typ, 655 mW max
<b>TEMPERATURE RANGE</b>	
Operating	
9414C	-0°C to +70°C
9414B	-55°C to +125°C
Storage	-65°C to +165°C

## NOTES:

- Input range selected at factory.  
HS 9414C-1 = 0 to +10V or ±5V input  
HS 9414C-2 = ±10V input  
HS 9414B-1 = 0 to +10V or ±5V input  
HS 9414B-2 = ±10V input
- Assumes pipelining -- signal is applied to I.A., acquired by sample/hold and converted by A/D.
- Externally adjustable to zero. See Applications Information.

## PACKAGE OUTLINE



## PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	CH0 HI	40	LATCH
2	CH0 LO	39	MA0
3	CH1 HI	38	MA1
4	CH1 LO	37	GA0
5	CH2 HI	36	GA0
6	CH2 LO	35	V <sub>CC</sub> (+15V)
7	CH3 HI	34	V <sub>EE</sub> (-15V)
8	CH3 LO	33	Analog GND
9	Input Offset Adjust -	32	Digital GND
10	Input Offset Adjust +	31	V <sub>LOGIC</sub> (+5V)
11	Output Offset Adjust, Bipolar	30	12/B
12	Ref Out (+10V)	29	CS
13	Ref In, Gain Adjust	28	A <sub>0</sub>
14	Status	27	R/C
15	DB0 (LSB)	26	DB11 (MSB)
16	DB1	25	DB10
17	DB2	24	DB9
18	DB3	23	DB8
19	DB4	22	DB7
20	DB5	21	DB6

## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to Digital Common	0 to +16.5V
VEE to Digital Common	0 to -16.5V
V <sub>LOGIC</sub> to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$ , A <sub>0</sub> , 12/8, R/C, LATCH, MA0, MA1, GA0, GA1) to Digital Common	-0.5V to V <sub>LOGIC</sub> +0.5V
Analog Inputs (REF IN, BIP OFF, CHO-CH3) to Analog Common	±16.5V
Input Offset Adjust Pins 9, 10	V <sub>CC</sub> ±1V
REF OUT to Analog or Digital GND	Indefinite short circuit to ±V <sub>DD</sub> , 100 ms short circuit
Voltage on Digital Outputs in Tri-State Mode	+V <sub>CC</sub> +0.5V max
Lead Temperature, Soldering	300°C, 10 sec

## APPLICATIONS INFORMATION

### A/D CONTROL FUNCTIONS

The HS 9414 contains all control functions necessary to provide for complete microprocessor interface and also 'stand alone' operation including continuous conversions. All A/D control functions are defined in Table 1 and Table 2.

FUNCTION	DEFINITION	FUNCTION
$\overline{CS}$	Chip Select	1. Typically the address pin when used with $\mu$ P. 2. Must be low (0) for a conversion to start or read data at the output. 3. $\uparrow$ transition may be used to initiate conversion.
R/C	Read/Convert	1. $\uparrow$ initiate conversion 2. $\downarrow$ initiate read
A <sub>0</sub>	Address	1. Selects conversion mode. 12 Bits if low (0), 8 Bits if high (1). 2. In read mode A <sub>0</sub> selects the output format. If low (0) then 8 MSB's (high and middle byte) or if high (1) then only low byte and trailing zeros.
12/8	Output Format	1. May be hard wired. 2. Normal 12-Bit format if high (1). 3. 8-Bit format as set by A <sub>0</sub> if low (0).

Table 1. Defining A/D Control Functions

CONTROL INPUTS				HS 9414 OPERATION
CS	R/C	12/8	A <sub>0</sub>	
1	X	X	X	No Operation
0	$\uparrow$	X	0	Initiates 12-Bit Conversion
0	$\uparrow$	X	1	Initiates 8-Bit Conversion
$\uparrow$	0	X	0	Initiates 12-Bit Conversion
$\uparrow$	0	X	1	Initiates 8-Bit Conversion
0	$\downarrow$	Pin 31	X	Enables 12-Bit Parallel Output
0	$\downarrow$	Pin 32	0	Enables 8 MSB's
0	$\downarrow$	Pin 32	1	Enables 4 LSB's and 4 Trailing Zeros
$\uparrow$	1	Pin 31	X	Enables 12 Bit Parallel Output
$\uparrow$	1	Pin 32	0	Enables 8 MSB's
$\uparrow$	1	Pin 32	1	Enables 4 LSB's & 4 Trailing Zero's

- NOTES
- 1 indicates logic HIGH
  - 0 indicates logic LOW
  - X indicates don't care.
  - $\uparrow$  indicates operation commences on low to high transition
  - MSB  $\rightarrow$  XXXX    XXXX    XXXX  $\leftarrow$  LSB  
High Middle Low  
Byte Byte Byte
  - Not a common use of this function

Table 2. HS 9414 A/D Section Truth Table

## SPGIA CONTROL FUNCTIONS

The HS 9414 has a 4-Bit transparent latch that selects input MUX channel as well as Gain. The SPGIA control functions are defined in Table 3.

NAME	DEFINITION	FUNCTION
LATCH	MUX, Gain, Clock	1. $\uparrow$ Update input MUX & Gain 2. $\downarrow$ Hold input MUX & Gain 3. High (1) is hold mode 4. Low (0) is transparent mode
MA1, MA0	MUX Address	Select Input MUX Channel MA0    MA1    CH 0    0    0 0    1    1 1    0    2 1    1    3
GA1, GA0	Gain Address	Select Gain GA1    GA0    Gain 0    0    0(x1) 0    1    1(x10) 1    0    2(x100) 1    1    3(x500)

Table 3. Defining the SPGIA Control Functions

## TIMING

The timing diagrams are shown in Figure 1. Note that to start a conversion  $\overline{CS}$ , and R/C must have an overlap time of 120 nS minimum.  $\overline{CS}$  and R/C may be advanced or delayed if needed (by the application) but no specifications are given for this — only the coincidence of 120 nS must be met. Typically R/C is used to initiate a conversion — however other lines may be used. See truth table (Table 2).

In the READ mode note the access time  $t_{DD}$  is 125 nS typ, 150 nS max. This means that an entire conversion can be completed and read in 25.3  $\mu$ S typ, 30.35  $\mu$ S max including setup, conversion time and access time.

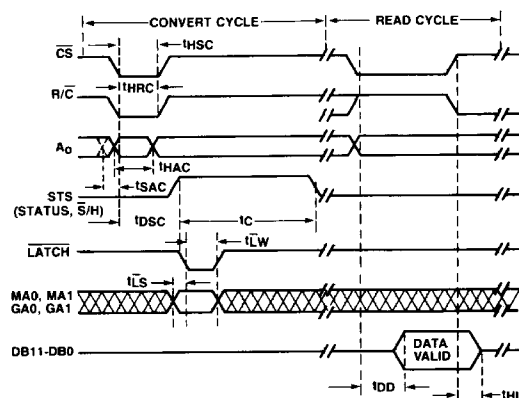


Figure 1a. HS 9414 Interface Timing

### CONVERT CYCLE

SYMBOL	PARAMETER	
$t_{HSC}$	$\overline{CS}$ Pulse Width	120 nS min
$t_{HRC}$	$R/\overline{C}$ LOW during $\overline{CS}$ LOW	120 nS min
$t_{HAC}$	$A_0$ valid during $\overline{CS}$ LOW	120 nS min
$t_{SAC}$	Maximum $A_0$ delay from $\overline{CS}$ Set up as shown (negative time wrt $\overline{CS}$ ) not needed	60 nS max
$t_{DSC}$	STS delay from $\overline{CS}$	150 nS min
$t_C$	Conversion time	
	8 Bit cycle	15 $\mu$ S typ, 25 $\mu$ S max
	12 Bit cycle	25 $\mu$ S typ, 30 $\mu$ S max
$t_{LS}$	LATCH Setup Time	33 nS min
$t_{LW}$	LATCH Pulse Width	33 nS min

NOTE: No setup for  $\overline{CS}$ ,  $R/\overline{C}$  or  $A_0$  is required. The only condition that must be satisfied is 120 nS coincidence, as shown.  $R/\overline{C}$ , or  $\overline{CS}$ , can be advanced or delayed as needed as long as this condition is met. Should  $A_0$  be delayed ( $t_{SAC}$  = 60 nS) then this must be added to  $\overline{CS}$  and  $R/\overline{C}$ . This condition not shown above.

### READ CYCLE

$t_{DD}$	Access time from $\overline{CS}$ LOW	125 nS typ, 150 nS max
$t_{HL}$	Output Float Delay	150 nS max

\* wrt = With Respect To.

Figure 1b. HS 9414 Interface Timing

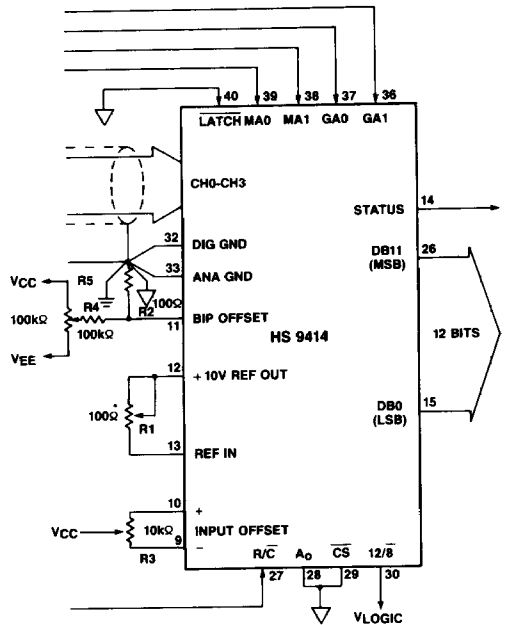


Figure 2b. Unipolar Stand-Alone Connections with Offset and Gain Adjustments

### STAND-ALONE OPERATION

The HS 9414 can be used in a 'stand-alone' mode. Connections and timing for this mode are shown in Figure 2.

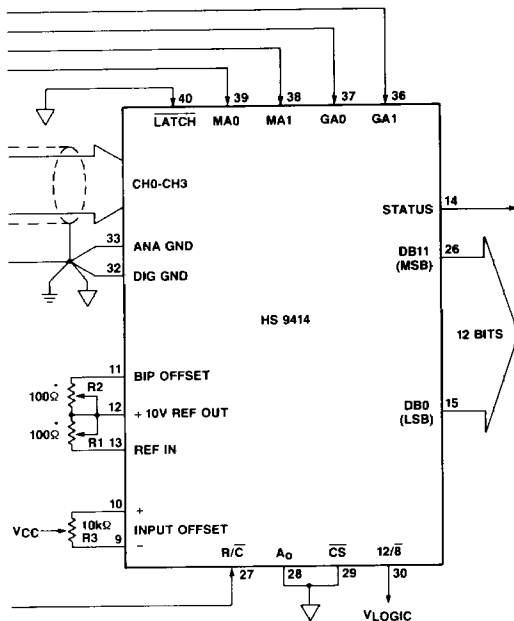


Figure 2a. Bipolar Stand-Alone Connections with Offset and Gain Adjustments

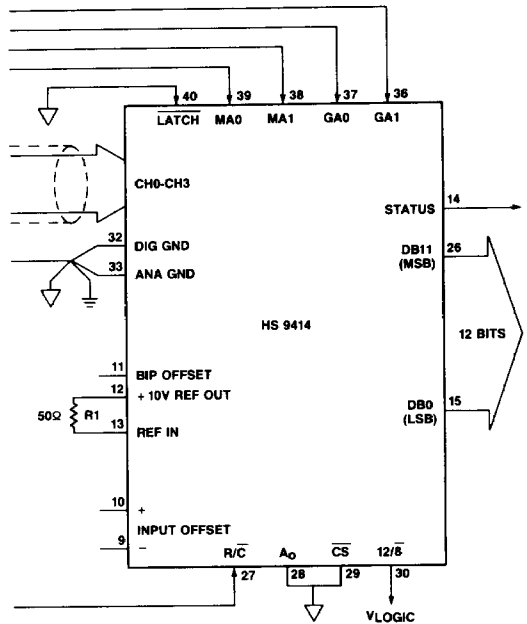


Figure 2c. No Trim Unipolar Connections

\* Trim pots can be 300 $\Omega$  for greater range adjustments.

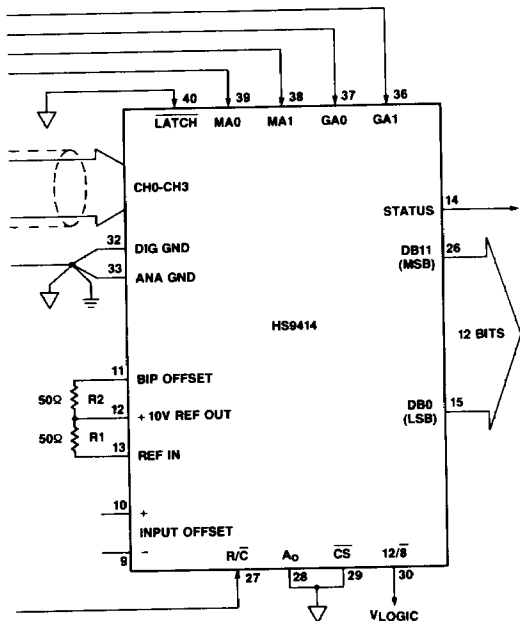
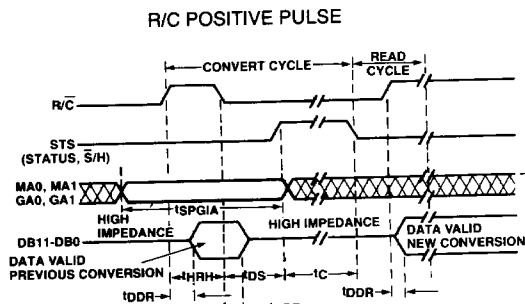


Figure 2d. No Trim Bipolar Connections



### CONVERT CYCLE

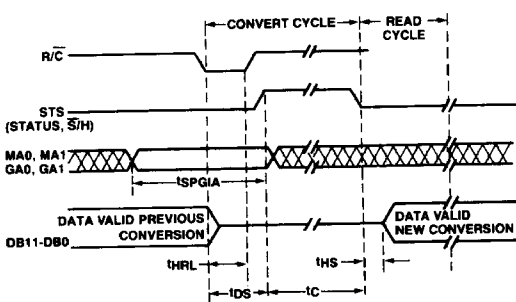
SYMBOL	PARAMETER	
$t_{HDR}$	Valid Data (Previous Conversion) after R/C low	100 nS min
$t_{HRH}$	High R/C Pulse Width	90 nS min
$t_{DS}$	STS Delay from R/C	200 nS max
$t_{DDR}$	Data Access Time	150 nS max
$t_C$	Conversion Time	30 $\mu$ S max
$t_{SPGIA}$	Software programmable gain instrumentation amplifier and S/H settling time after input MUX, gain or input signal change	

### READ CYCLE

1. Converter output remains in high impedance state after conversion (STS goes low) until R/C goes high (to read data).

Figure 3. HS 9414 Stand-Alone Operation  
Top: Using Negative R/C Pulse  
Bottom: Using Positive R/C Pulse

### R/C NEGATIVE PULSE



### CONVERT CYCLE

SYMBOL	PARAMETER	
$t_{HRL}$	Low R/C Pulse Width	100 nS min
$t_{DS}$	STS Delay from R/C	200 nS max
$t_C$	Conversion Time	30 $\mu$ S max
$t_{HS}$	Data valid after STS low	70 nS max
$t_{SPGIA}$	Software programmable gain instrumentation amplifier and S/H settling time after input MUX, gain or input signal change	

### READ CYCLE

1. Data always in read mode except during a conversion in which data lines revert to high impedance or when R/C goes low (0).
2. Output always valid after conversion is complete.

## INCREASING THROUGHPUT

To minimize added set-up delay, overlapping the multiplexer channels can significantly improve throughput. The technique involved is the same as normal operation; however, instead of waiting for the A/D to complete a conversion before selecting a new multiplexer channel, the new channel is selected at the start of the A/D conversion. By doing this, the A/D digitizes the analog voltage that is held in the sample and hold and the new multiplexer channel's voltage can start to settle through the multiplexer and instrumentation amplifier. An added 25  $\mu$ S (A/D conversion time) can be saved from the front end settling time required by preselecting the new channel. After the A/D is finished converting, the sample and hold will switch back to sample to acquire the newly selected channel's voltage and the process repeated.

11

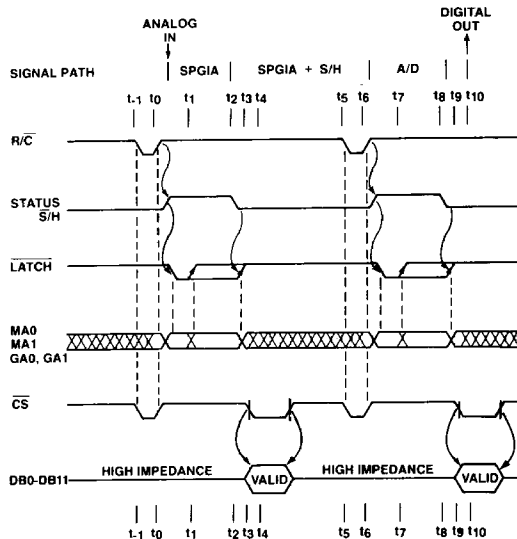


Figure 4. HS 9414 Pipeline Timing for Highest Throughput

- $t_1-t_0$   $R/\overline{C}$  pulse starts new conversion and sample and hold goes to hold mode.
- $t_0-t_2$  New SPGIA gain, new input MUX channel and new input signal while the A/D is converting.
- $t_3-t_6$  Sample and hold samples the new input signal.
- $t_3-t_4$  A/D data from the last signal is retrieved.
- $t_5-t_6$   $R/\overline{C}$  starts conversion of the new input signal.
- $t_6$  Sample and hold holds the new signal.
- $t_6-t_7$  Next SPGIA gain, next input MUX channel and next input signal.
- $t_7-t_9$  The new signal is converted.
- $t_{10}$  The new signal digital data is retrieved.

NOTE: Pipeline delay from  $t_0$  to  $t_{10}$   
 Throughput is  $1/t_6$  to Hz  
 SPGIA settling time from  $t_0$  to  $t_6$   
 S/H acquisition time from  $t_2$  to  $t_6$

## USING THE $A_0$ LINE

The state of the  $A_0$  line at the start of a conversion places the HS 9414 in either a full 12-Bit conversion or in an 8-Bit 'short cycle' mode. During a READ at the end of a conversion the  $A_0$  line is used to format the data as follows:

### 1. Prior to Conversion

$A_0 = 1$   
 $A_0 = 0$

### 2. After Conversion (READ)

$A_0 = 1$   
 $A_0 = 0$

### MODE

Short cycle 8-Bit conversion  
 Full 12-Bit conversion

Data = Low Byte (LSB)  
 followed by zeros  
 Data = High Byte (MSB's)  
 followed by middle and low byte.

In a  $\mu P$  application the  $A_0$  line can be considered a pair of  $\overline{WR}$  locations as follows:

### 1. Prior to Conversion (WRITE)

$\overline{WR} = 0$  in low address ( $A_0 = 0$ )  
 $\overline{WR} = 0$  in high address ( $A_0 = 1$ )

### 2. After Conversion (READ)

$\overline{WR} = 1$  in either address ( $A_0 = X$ )  
 $\overline{WR} = 1$  in high address ( $A_0 = 1$ )  
 $\overline{WR} = 1$  in low address ( $A_0 = 0$ )

### MODE

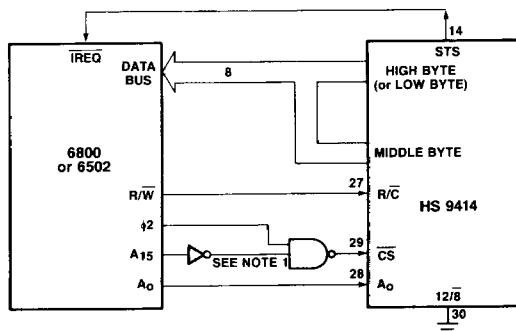
Full 12-Bit conversion  
 Short cycle 8-Bit conversion

Full 12-Bit word with  $12/\overline{8} - 1$   
 LSB's & zeros when  $12/\overline{8} = 0$   
 8 MSB's only when  $12/\overline{8} = 0$

## INTERFACING THE HS 9414 WITH 8-BIT MICROPROCESSORS

The HS 9414 which has 12-Bit data can be used directly with popular 8-Bit microprocessors. The data however, must be multiplexed by setting the output mode select  $12/\overline{8}$  pin to GND.

In the first case, a 6800 (or 6502) is used. See Figure 5.



NOTE 1. Decoding may be needed for a large system.

Figure 5. Interfacing the HS 9414 and a 6800  $\mu P$

The STATUS (STS) is tied directly to IREQ which is the interrupt line. When STS goes to 0 (at the end of a conversion) the 6800 may either service the interrupt or be timed for 30  $\mu S$  (since this IREQ is software maskable) the time required for a conversion.

Figure 6 shows the 8080A  $\mu P$  as interfaced with the HS 9414. In this case, a 8228 controller is shown with gates to generate needed signals.

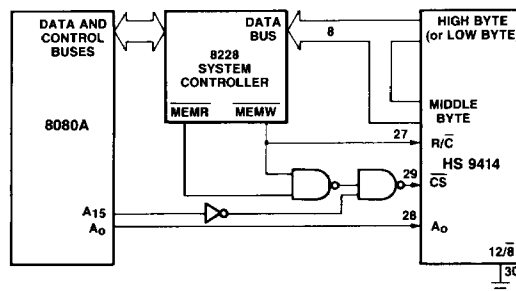


Figure 6. Interfacing the HS 9414 and 8080A  $\mu P$

Figure 7 shows the HS 9414 connected with a 8048  $\mu$ P. A single AND gate is used to generate  $\overline{CS}$ .

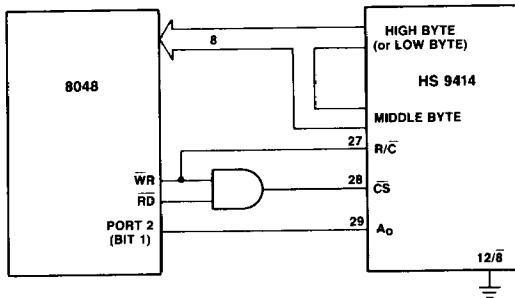


Figure 7. Interfacing the HS 9414 with a 8048  $\mu$ P.

A summary of  $\mu$ P types and connections is in Table 4.

MICRO-PROCESSOR	HS 9414 CONTROL INPUTS		
	R/C	CS	A <sub>0</sub>
8080 MEMORY MAPPED I/O PROGRAMMED I/O	$\overline{(MEMR)}$ $\overline{(I/O\overline{R})}$	DECODED ADDRESS	A <sub>0</sub>
6800	R/ $\overline{W}$	DECODED ADDRESS	A <sub>0</sub>
6502	R/ $\overline{W}$	DECODED ADDRESS	A <sub>0</sub>
Z80 MEMORY MAPPED I/O PROGRAMMED I/O	$\overline{(RD)}$ $\overline{(RD)}$	DECODED ADDRESS WITH MREQ DECODED ADDRESS WITH IOR	A <sub>0</sub> A <sub>0</sub>
8048	$\overline{(RD)}$	PORT 2 <sub>0-3</sub> *	PORT 2 <sub>0-3</sub> *

\*Port 2, Lines 0-3 can be used as a 4-Bit address bus. System address decoding requirements vary from no hardware to a fully latched 12-Bit address, depending on system complexity.

Table 4. Summary of HS 9414 Control Inputs with Various Microprocessors

### ENABLING DATA IN 8-BIT OUTPUT MODE

For an 8-bit system Figures 5, 6 and 7 show no direct connection of the low bytes. Hybrid Systems has provided internal multiplexing prior to the output tri-state drivers of the MSB's and LSB's. During the READ cycle when A<sub>0</sub> = 0 the 8 MSB's are enabled and appear on pins 19-26. When A<sub>0</sub> = 1 the LSB's are multiplexed onto pins 23-26, pins 20-23 to "0", and pins 15-18 float (High Z). The LSB's may be hardwired directly to the MSB's (23-26) with no loss in system performance but this will decrease the system versatility.

A recap of the output data in an 8-bit system is as follows:

### CONDITIONS

- 12/8 (pin 2) grounded or at "0"
- READ cycle.

A <sub>0</sub> State	OUTPUT		
	23-26 (High)	19-22 (Middle)	15-18 (Low)
0	MSB Data (Bits 1-4)	Middle Bit Data (Bits 5-8)	Float (High Z)
1	LSB Data (Bits 9-12)	0's	Float (High Z)

### USING THE LATCH LINE

The LATCH line controls the internal 4-Bit transparent latch that holds the input MUX channel number (MA0, MA1) and the gain selection word (GA0, GA1). A low (0) on this line updates this latch and a high (1) holds the new word.

If the system where the HS 9414 is being used already has fully implemented output ports, then the LATCH line may be hardwired low so that an output port may control the timing of the input MUX and SPGIA gain directly. (See Figure 8).

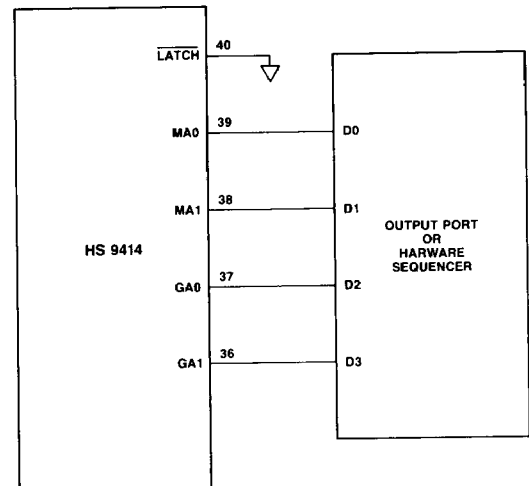


Figure 8.

If the system does not have available output ports for the input MUX channel and gain selection, then 4-Bits from the system data bus can be directly tied to the MA0, MA1, GA0 and GA1 lines. Port address control decoding circuitry is connected to the LATCH line so that the 4-Bit data is grabbed from the system bus at the proper time. (See Figure 9).

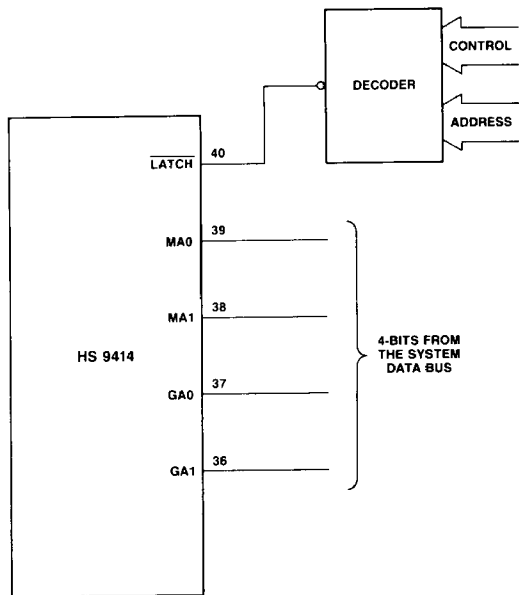


Figure 9.

### OUTPUT OFFSET AND GAIN ADJUSTMENT AT GAIN = 1

The output offset and gain adjustments are used to calibrate the A/D section at a gain of one. The HS 9414 is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. If no trims are used, the gain of one calibration will be within approximately  $\pm 2$  LSB zero offset error, and  $\pm 12$  LSB maximum full scale error. See Figure 2c & 2d for connection with no trims. If gain and zero adjustment potentiometers are used, they should be connected as shown in Figure 2a & 2b. The zero control has a range of about  $\pm 20$  LSB, and the gain control has a range of about  $\pm 13$  LSB.

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10 LSB at both ends of its range.

The HS 9414's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first.

### SPGIA INPUT OFFSET ADJUSTMENT AT HIGH GAIN

The HS 9414 provides input offset adjustment to allow calibration of input offset errors to less than  $5 \mu\text{V}$  ( $< 1/2$  LSB @G = 500) at high gains. The initial offset error before calibration is typically less than  $50 \mu\text{V}$  or  $250 \mu\text{V}$  maximum at G = 500. This input offset error may be adequate in some applications, and input offset adjustment may be omitted. See Figure 2 for the various adjustment options.

Proper use of the input and output offset adjustment pots results in an offset free system regardless of SPGIA gain setting or input channel. This can be achieved by calibrating the A/D section output offset and gain adjustments first and the input offset second. After the input offset is adjusted at G = 500 the output offset at G = 1 may need a minor adjustment.

### A/D CALIBRATION

1. Center input offset pot if used.
2. Set SPGIA gain to one.
3. Tie channel LO to analog ground (Pin 33) and apply the input voltage standard between HI and LO of that channel.
4. Make sure that the voltage standard is grounded externally only at the input channel LO.

### ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
  - a) Set input voltage precisely to  $+ 1/2$  LSB.
  - b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
  - a) Set input voltage precisely to  $1/2$  LSB above  $-F.S.$
  - b) Adjust zero control until converter is switching from 000000000000 to 000000000001

### GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to  $1/2$  LSB less than "all bits on" ideal value. Note that this is  $1 1/2$  LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.

Table 5 summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the HS 9414.

### SPGIA OFFSET CALIBRATION PROCEDURE

1. Calibrate the A/D section first.
2. Set the SPGIA gain to 500.
  - a) Apply  $1/2$  LSB to the input channel via a 500:1 attenuator as shown in Figure 10 or via the external front end circuitry.  $1/2$  LSB at gain of 500 is  $4.8 \mu\text{V}$  for 20V range units (HS 9414X-2) and  $2.4 \mu\text{V}$  for 10V range units (HS 9414X-1).
  - b) Unipolar configuration:  
Adjust input offset pot until converter is switching from 000000000000 to 000000000001
  - c) Bipolar configuration:  
Adjust input offset pot until converter is switching from 100000000000 to 1000000000001

Voltage Range	Adjustment	Ideal Input Voltage Value				Adjust input to point where converter is just on the verge of switching between the two codes shown. <sup>1</sup>
		GAIN = 1	GAIN = 10	GAIN = 100	GAIN = 500	
0 to +10V	ZERO	1.22mV	0.122mV	12.2 $\mu$ V	2.4 $\mu$ V	00000000000
	GAIN	9.9963V	0.99963V	99.963mV	19.9926mV	11111111110
$\pm 5V$	ZERO	-4.9988V	-0.49988V	-49.988mV	9.9976mV	00000000000
	GAIN	4.9963V	0.49963V	49.963mV	-9.9926mV	11111111110
$\pm 10V$	ZERO	-9.9976V	-0.9976V	-99.976mV	-19.9952mV	00000000000
	GAIN	9.9927V	0.99927V	99.927mV	19.99859mV	11111111110

NOTE 1. Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges. The term "0" is the transition between a logic 0 and a logic 1 state.

Table 5. Calibration Data

### POWER SUPPLY CONSIDERATION

Power supplies used for the HS 9414 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 5  $\mu$ V is 1 LSB for a 10 volt range, at a gain of 500.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10  $\mu$ F tantalum type in parallel with 0.1  $\mu$ F disc ceramic type.

### GROUNDING CONSIDERATIONS

To insure maximum accuracy, the HS 9414 has a separate analog and digital ground; these two grounds must be routed properly to prevent DC and transient errors.

DC errors can be caused by current flowing through a run resistance between the system ground reference

and the DAS ground reference. (One mA through 2.5 $\Omega$  will cause an LSB of error.) The best way to prevent this type of error is to connect the digital and analog grounds very close to the HS 9414 and use this point as the system ground. This can be done as a so-called "star ground" as shown in Figure 11. The single common ground reference insures no ground current or ground loop errors.

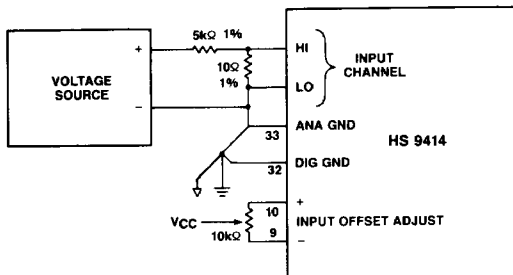


Figure 10. Suggested SPGIA Input Offset Calibration Circuit

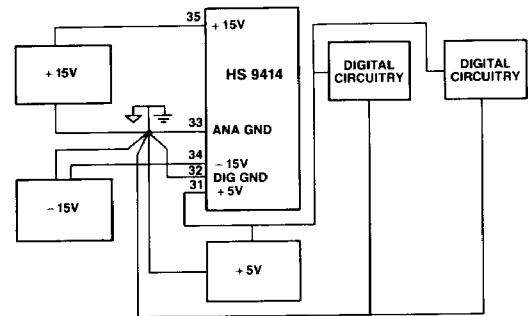


Figure 11.

### ANALOG FRONT END

If the circuit is to be used at or near its maximum throughput rate, care must be used to prevent dynamic errors due to source impedance at the multiplexer inputs. If a low-pass anti-alias filter is used at the analog inputs (Figure 12a), it is suggested that a buffer be used (Figure 12b) to eliminate charge-transfer errors between C<sub>FILTER</sub> and C<sub>MUX,AMP</sub> (Figure 12c).

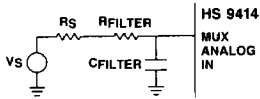


Figure 12a. (Not Recommended)

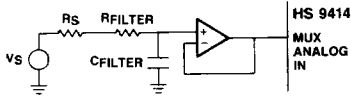


Figure 12b. (Recommended)

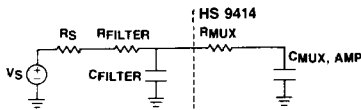


Figure 12c. (Equivalent Circuit of 12a)

The HI and LOW inputs for each channel are adjacent to each other in the package. This simplifies layout of closely spaced HI and LO lines and eases connection of shielded and twisted pairs for each channel. (See Figure 13). These wiring considerations are particularly important at high SPGIA gain settings. The close proximity and similarity of the HI and LO conductors also reduces thermoelectric errors due to Seebeck effect.

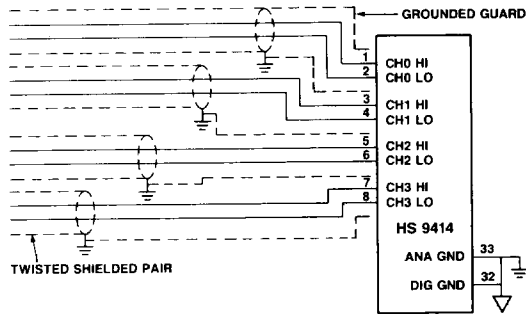


Figure 13. Recommended Input Wiring Layout

## DYNAMIC PERFORMANCE CONSIDERATIONS

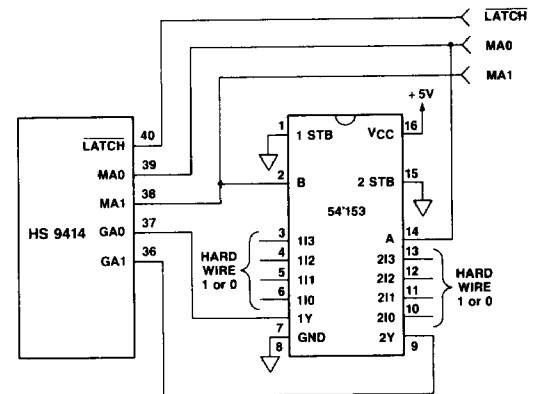
The analog signal path in the HS 9414 has a characteristic settling time for each gain setting. If maximum accuracy is desired, enough settling time for each gain setting must be allowed. If not, each new conversion may have vestigial amounts of signal from the previous conversion. This phenomenon also manifests itself as poor crosstalk performance among successively converted channels or input signals.

Coherent noise coupling and input MUX crosstalk is more detrimental at certain time slots of the DAS pipeline (Figure 4) than others. System coherent noise spikes and adjacent channel dynamic swings will affect the signal that is being converted more severely if they happen in the last 1 to 10  $\mu$ s before the status line goes high.

When switching the SPGIA to a higher gain it is important to make sure that the input MUX is not switched to the new low level signal later than the gain. Momentary saturation may occur while the signal presented to SPGIA is still high level and the new gain is high.

## FIXED GAIN ASSIGNMENT FOR EACH INPUT CHANNEL

The HS 9414 has four input channels and four independent gains. Any input channel can be software or hardware programmed for any gain in any sequence of DAS conversions. However, in some applications it suffices to preassign a fixed gain for each channel. This reduces the number of SPGIA control bits from four (MA0, MA1, GA0, GA1) to two (MA0, MA1). Figure 14 shows an implementation of this configuration using a dual 4-input multiplexer.



EXAMPLE:  
 210, 110 = 1, 1 CH0 HAS GAIN OF 500  
 211, 111 = 0, 0 CH1 HAS GAIN OF 1  
 212, 112 = 1, 0 CH2 HAS GAIN OF 100  
 213, 113 = 0, 1 CH3 HAS GAIN OF 10

INPUT CHANNEL	ASSIGNED GAIN AT:
CH0	210, 110
CH1	211, 111
CH2	212, 112
CH3	213, 113

Figure 14. Input Channel Assigned Gain

