HARRIS SEMICONDUCTOR

HS-82C54RH

Radiation Hardened CMOS Programmable Interval Timer

August 1995

Features

- Radiation Hardened
  - Total Dose > 10^5 RAD (Si)
  - Transient Upset > 10^8 RAD (Si)/sec
  - Latch Up Free EPI-CMOS
  - Functional After Total Dose 1 x 10^6 RAD (Si)
- Low Power Consumption
  - IDDSB = 20µA
  - IDDOP = 12mA
- Pin Compatible with NMOS 8254 and the Harris 82C54
- High Speed, "No Wait State" Operation with 5MHz HS-80C86RH
- Three Independent 16-Bit Counters
- Six Programmable Counter Modes
- Binary or BCD Counting
- Status Read Back Command
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range -55°C to +125°C

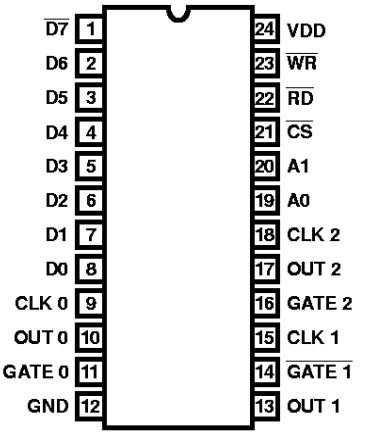
Description

The Harris HS-82C54RH is a high performance, radiation hardened CMOS version of the industry standard 8254 and is manufactured using a hardened field, self-aligned silicon gate CMOS process. It has three independently programmable and functional 16-bit counters, each capable of handling clock input frequencies of up to 5MHz. Six programmable timer modes allow the HS-82C54RH to be used as an event counter, elapsed time indicator, a programmable one-shot, or for any other timing application. The high performance, radiation hardness, and industry standard configuration of the HS-82C54RH make it compatible with the HS-80C86RH radiation hardened microprocessor.

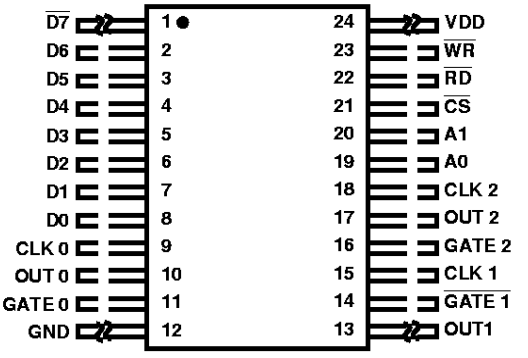
Static CMOS circuit design insures low operating power. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Pinouts

24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP) MIL-STD-1835 CDIP2-T24
TOP VIEW



24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK) MIL-STD-1835 CDFP4-F24
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HS1-82C54RH-Q	-55°C to +125°C	24 Lead SBDIP
HS1-82C54RH-8	-55°C to +125°C	24 Lead SBDIP
HS1-82C54RH-Sample	+25°C	24 Lead SBDIP
HS9-82C54RH-Q	-55°C to +125°C	24 Lead Ceramic Flatpack
HS9-82C54RH-8	-55°C to +125°C	24 Lead Ceramic Flatpack
HS9-82C54RH/Sample	+25°C	24 Lead Ceramic Flatpack
HS9-82C54RH/Proto	-55°C to +125°C	24 Lead Ceramic Flatpack

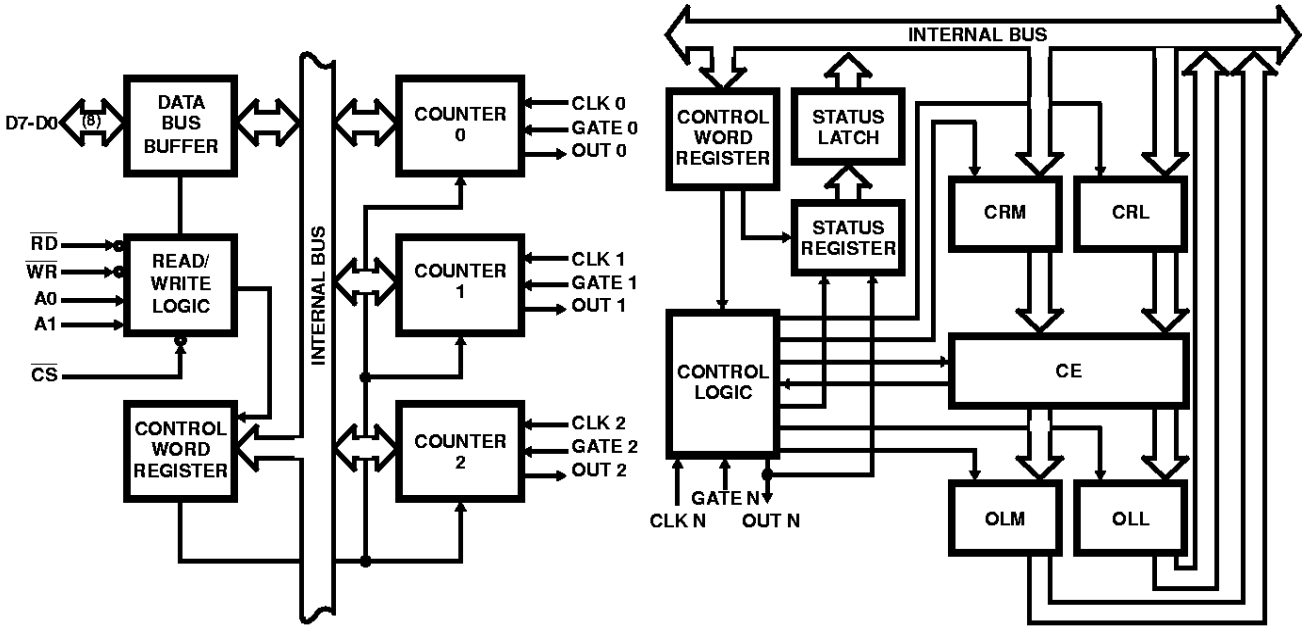
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Spec Number 518059
File Number 3043.1

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
D7-D0	1-8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A0, A1	19-20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus. **A1 A0 Selects** 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the HS-82C54RH to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
VDD	24		VDD: The +5V power supply pin. A 0.1µF capacitor between pins 12 and 24 is recommended for decoupling.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage
Applied for all Grades . . . . . VSS-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
Typical Derating Factor . . . . . 2.4mA/MHz Increase in IDDOP
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	40°C/W	6°C/W
Ceramic Flatpack Package	60°C/W	4°C/W

Maximum Package Power Dissipation at +125°C Ambient
SBDIP Package 1.25W
Ceramic Flatpack Package 0.83W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package 25.0mW/C
Ceramic Flatpack Package 16.7mW/C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage (VIL) . . . . . 0V to +0.8V
Input High Voltage (VIH) . . . . . VDD -1.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
TTL Output High Current	IOH1	VDD = 4.5V, VO = 3.0V, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-2.5	-	mA
CMOST Output High Current	IOH2	VDD = 4.5V, VO = 4.1V, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-100	-	µA
Output Low Current	IOL	VDD = 4.5V, VO = 0.4V, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	2.5	-	mA
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V or 5.5V Pins: 9, 11, 14-16, 18-23	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VIN = 0V or 5.5V Pins: 1-8	1, 2, 3	-55°C, +25°C, +125°C	-10	10	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, VIN = GND or VDD IO = 0mA, Counters Programmed	1, 2, 3	-55°C, +25°C, +125°C	-	20.0	µA
Operating Power Supply Current	IDDOP	VDD = 5.5V, VIN = GND or VDD IO = 0mA, CLK0 = CLK1 = CLK2 = 5MHz	1, 2, 3	-55°C, +25°C, +125°C	-	12.0	mA
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 5.5V, VIN = GND or VDD - 1.5 and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

AC's Tested at Worst Case VDD (s), Guaranteed Over Full Operating Range.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Stable Before $\overline{RD}$	TAVRL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	75	-	ns
$\overline{CS}$ Stable Before $\overline{RD}$	TSLRL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Hold Time After $\overline{RD}$	TRHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{RD}$ Pulse Width	TRLRH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	240	-	ns
Data Delay from $\overline{RD}$	TRLDV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

AC's Tested at Worst Case VDD (s), Guaranteed Over Full Operating Range.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Command Recovery Time	TRHRL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	320	-	ns
WRITE CYCLE							
Address Stable Before $\overline{WR}$	TAVWL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{CS}$ Stable Before $\overline{WR}$	TSLWL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Hold Time After $\overline{WR}$	TWHAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{WR}$ Pulse Width	TWLWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	240	-	ns
Data Setup Time Before $\overline{WR}$	TDVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	225	-	ns
Data Hold Time After $\overline{WR}$	TWHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	35	-	ns
Command Recovery Time	TWHWL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	320	-	ns
CLOCK AND GATE							
Clock Period	TCLCL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
High Pulse Width	TCHCL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Low Pulse Width	TCLCH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Gate Width High	TGHGL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Gate Width Low	TGLGH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Gate Setup Time to CLK	TGVCH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Gate Hold Time After CLK	TCHGX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	80	-	ns
Output Delay from CLK	TCLOV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	-	240	ns
Output Delay from Gate	TGLOV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
Data Delay from Address Read	TAVAV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	-	275	ns
Output Delay from $\overline{WR}$ High	TWHOV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	-	260	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	15	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	15	pF
I/O Capacitance	COUT	VDD = Open, f = 1MHz, All measurements referenced to device ground.	T_A = +25°C	-	20	pF
TIMING REQUIREMENTS						
$\overline{RD}$/ to Data Float	TRHDZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	8	145	ns
TIMING RESPONSES						
Clock Rise Time	TCH1CH2	VDD = 4.5V and 5.5V, 1.0V to 3.5V	-55°C < T_A < +125°C	-	25	ns
Clock Fall Time	TCL1CL2	VDD = 4.5V and 5.5V, 3.5V to 1.0V	-55°C < T_A < +125°C	-	25	ns

NOTE: The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: See +25°C limits in Table 1 and Table 2 for Post RAD limits (Sub Groups 1, 7 and 9).

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Standby Power Supply Current	IDDSB	±2µA
Output Leakage Current	IOZL, IOZH	±2µA
Input Leakage Current	IIH, IIL	±200nA
Output Low Current	IOL	±500µA or 10% of BBI Reading*
TTL Output High Current	IOH TTL	±500µA or 10% of BBI Reading*
CMOS Output High Current	IOH CMOS	±20µA or 10% of BBI Reading*

* Which ever is greater.

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100% 5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA	100% 5004	1, 7, Δ	-	1, 7	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	-	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)	N/A	
Subgroup B6	Sample 5005	1, 7, 9	-	N/A	
Group C	Sample 5005	N/A	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9	-	1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9	-	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.
2. Table 5 parameters only

Harris Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Die Attach

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

CSI and/or GSI PreCap (Note 6)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 72 Hours Min, +125°C Min, Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 1)

100% Dynamic Burn-In, Condition D, 240 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test 2(T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 2)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 3)

Sample - Group B, Method 5005 (Note 4)

Sample - Group D, Method 5005 (Notes 4 and 5)

100% Data Package Generation (Note 7)

CSI and/or GSI Final (Note 6)

NOTES:

1. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
2. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
3. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
4. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group B Samples, Group D Test and Group D Samples.
5. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
6. CSI and/or GSI inspections are optional and will not be performed unless required by theP.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI final inspection, GSI PreCap inspection, and/or GSI final inspection.
7. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Harris Space Level Product Flow -8

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Die Attach

Periodic- Wire Bond Pull Monitor, Method 2011

Periodic- Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition B

CSI an/or GSI PreCap (Note 5)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% External Visual

100% Initial Electrical Test

100% Dynamic Burn-In, Condition D, 160 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test

100% PDA, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 2)

Sample - Group B, Method 5005 (Note 3)

Sample - Group C, Method 5005 (Notes 3 and 4)

Sample - Group D, Method 5005 (Notes 3 and 4)

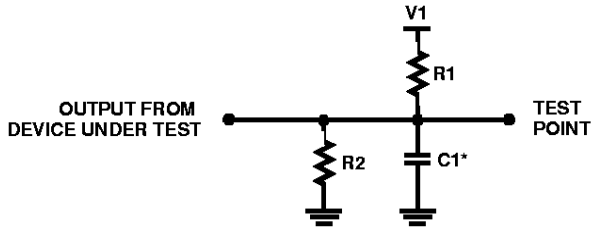
100% Data Package Generation (Note 6)

CSI and/or GSI Final (Note 5)

NOTES:

1. Failures from subgroup 1, 7 are used for calculating PDA. The maximum allowable PDA = 5%.
2. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
3. Group B, C and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.
4. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group C Generic Data and/or Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
5. CSI and/or GSI inspections are optional and will not be performed unless required by theP.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI final inspection, GSI PreCap inspection, and/or GSI final inspection.
6. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Group B, C and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

AC Test Circuits

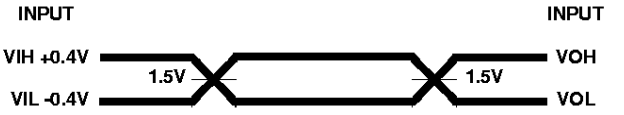


* Includes stray and jig capacitance

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	510	OPEN	150pF

AC Testing Input, Output Waveform



NOTE: AC Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1ns/V.

Waveforms

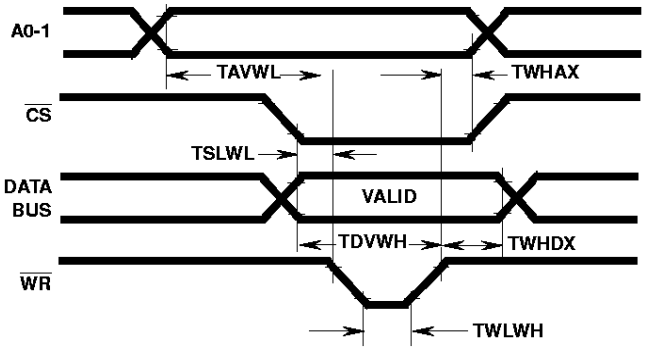


FIGURE 1. WRITE

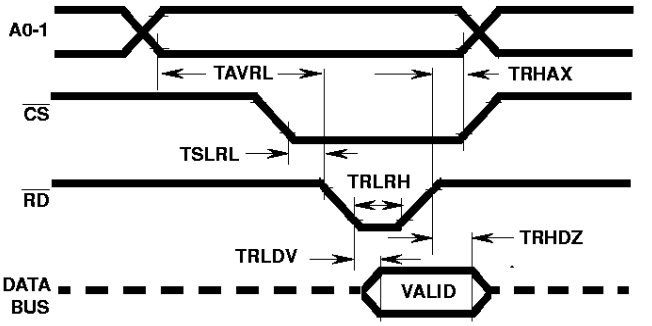


FIGURE 2. READ

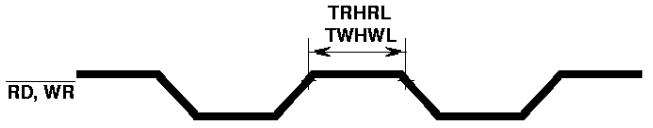


FIGURE 3. RECOVERY

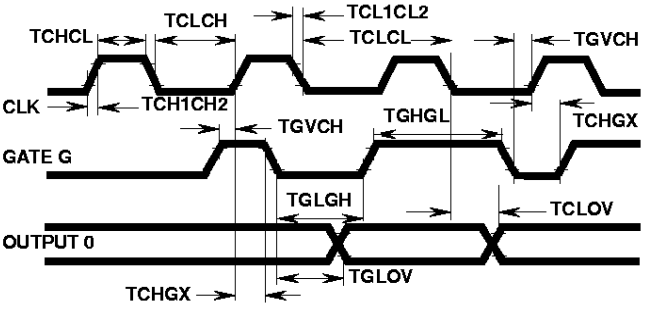
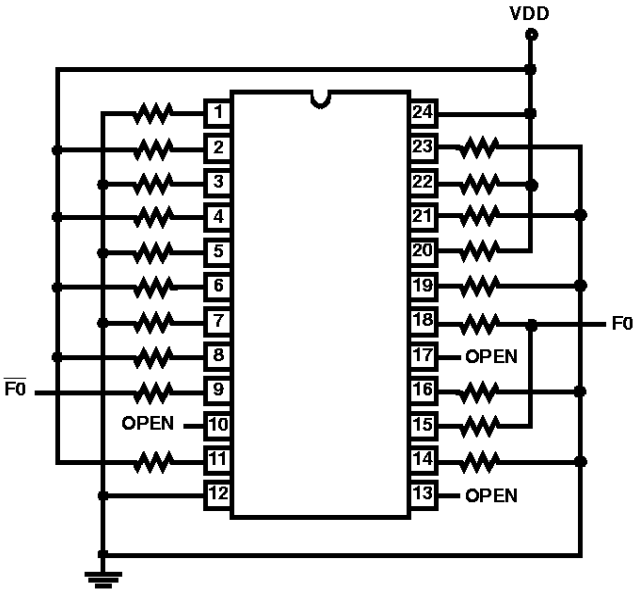


FIGURE 4. CLOCK AND GATE

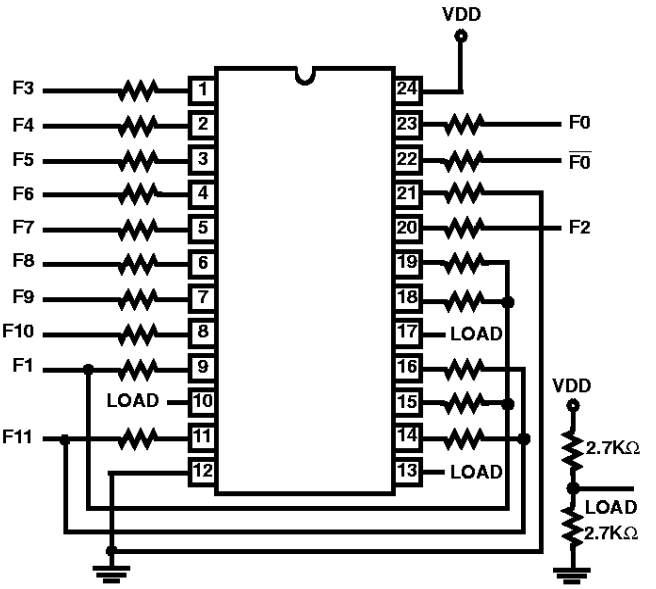
Burn-In Circuits



STATIC CONFIGURATION FOR BOTH FLATPACK & SBDIP PACKAGE

NOTES:

1. VDD = 6.5V ± 5%
2. T_A = +125°C Minimum
3. Resistors = 10kΩ
4. IDD < 100µA
5. AC: $\overline{F0}$ is compliment of F0
   F0 is a 50% duty cycle pulse burst
   F0 is left high after pulse burst

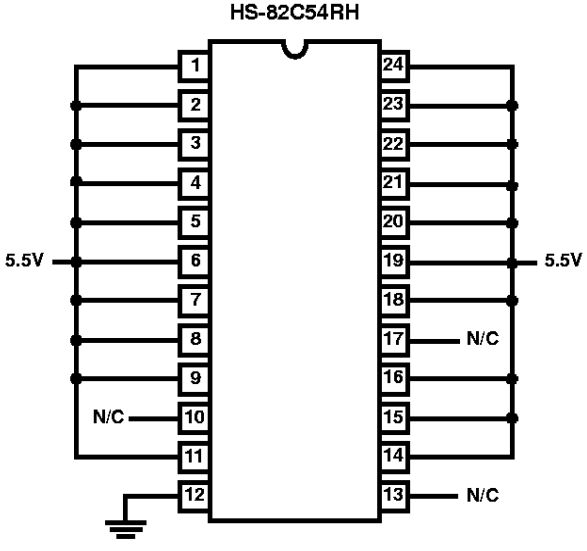


DYNAMIC CONFIGURATION FOR BOTH FLATPACK & SBDIP PACKAGE

NOTES:

1. VDD = 6.5V ± 5%(Burn-In)
2. VDD = 6.0V ± 5%(Life Test)
3. T_A = +125°C Minimum
4. IDD < 20mA
5. Resistors = 10KΩ, except for loads = 2.7kΩ
6. -0.3V ≤ VIL ≤ 0.8V
7. VDD -1.0V ≤ VIH ≤ VDD +0.5V
8. AC: $\overline{F0}$ is compliment of F0
   F0 = 100kHz ±10%, 50% Duty Cycle
   F1 = F0/2, F2 = F1/2 . . . F10 = F9/2

Irradiation Circuits



NOTES:

1. VDD = 5.5V ± 10%, T_A = +25°C
2. Group E Testing is performed in Sidebrazed DIP
3. Group E Sample Size is 2 die/wafer

Functional Description

General

The HS-82C54RH is a programmable interval timer/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The HS-82C54RH solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the HS-82C54RH to match his requirements and programs one of the counters for the desired delay. After the desired delay, the HS-82C54RH will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other timer functions common to micro-computers which can be implemented with the HS-82C54RH are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the HS-82C54RH to the system bus (see Figure 5).

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the HS-82C54RH. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the HS-82C54RH that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the HS-82C54RH that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the HS-82C54RH has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 6) is selected by the Read/Write Logic when A1, A0 = 11. If the CPU then does a write operation to the HS-82C54RH, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

Counter 0, Counter 1, Counter 2

These three functional clocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 7. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

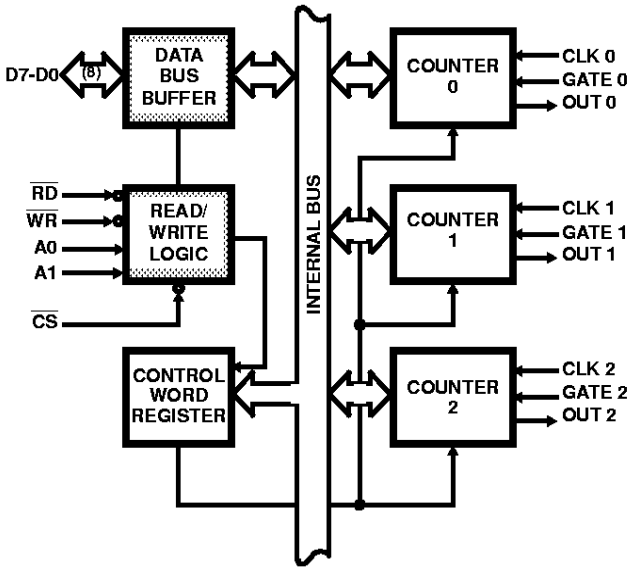


FIGURE 5. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTION

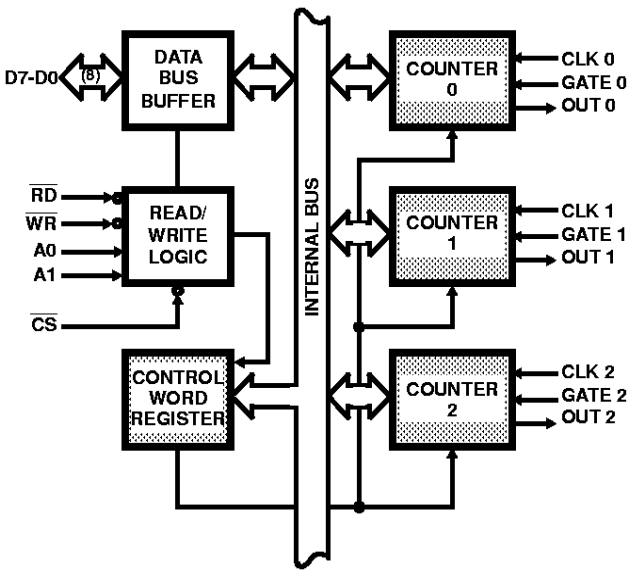


FIGURE 6. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

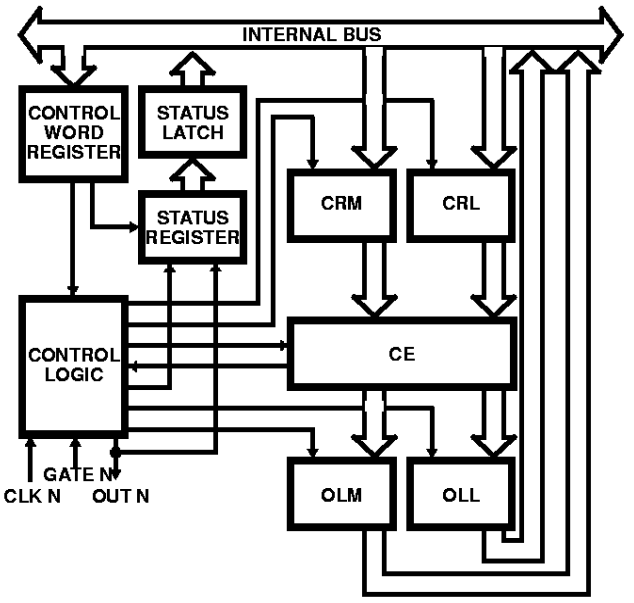


FIGURE 7. COUNTER INTERNAL BLOCK DIAGRAM

The Status Register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back Command.)

The actual counter is labeled CE for "Counting Element". It is a 16-bit presettable synchronous down counter.

OLM and OLL are two 8-bit latches. OL stands for "Output Latch", subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the HS-82C54RH, the OL latches the present count until read by the CPU and then returns to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CRM and CRL (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CRM and CRL are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLKn, GATEn, and OUTn are all connected to the outside world through the Control Logic.

HS-82C54RH System Interface

The HS-82C54RH is treated by the system software as an array of peripheral I/O ports; three are Counters and the fourth is a Control Word Register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder, such as a Harris HD-6440 for larger systems.

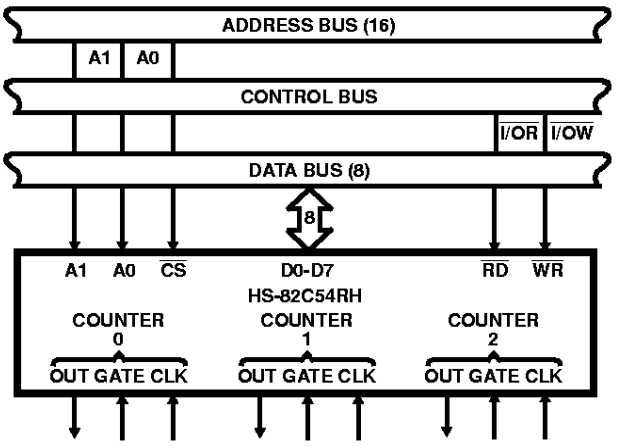


FIGURE 8. HS-82C54RH SYSTEM INTERFACE

Operational Description

General

After power-up, the state of the HS-82C54RH is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused Counters need not be programmed.

Programming The HS-82C54RH

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A1, A0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Write Operations

The programming procedure for the HS-82C54RH is very flexible. Only two conventions need to be remembered:

1. For each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counter shave separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

Control Word Format

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC2	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - Read/Write

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 9. CONTROL WORD FORMAT

	A1	A0
Control Word - Counter 0	1	1
LSB of count - Counter 0	0	0
MSB of count - Counter 0	0	0
Control Word - Counter 1	1	1
LSB of count - Counter 1	0	1
MSB of count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of count - Counter 2	1	0
MSB of count - Counter 2	1	0

	A1	A0
Control Word - Counter 2	1	1
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of count - Counter 2	1	0
MSB of count - Counter 2	1	0
LSB of count - Counter 1	0	1
MSB of count - Counter 1	0	1
LSB of count - Counter 0	0	0
MSB of count - Counter 0	0	0

	A1	A0
Control Word - Counter 0	1	1
Control Word - Counter 1	1	1
Control Word - Counter 2	1	1
LSB of count - Counter 2	1	0
LSB of count - Counter 1	0	1
LSB of count - Counter 0	0	0
MSB of count - Counter 0	0	0
MSB of count - Counter 1	0	1
MSB of count - Counter 2	1	0

	A1	A0
Control Word - Counter 1	1	1
Control Word - Counter 0	1	1
LSB of count - Counter 1	0	1
Control Word - Counter 2	1	1
LSB of count - Counter 0	0	0
MSB of count - Counter 1	0	1
LSB of count - Counter 2	1	0
MSB of count - Counter 0	0	0
MSB of count - Counter 2	1	0

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many possible programming sequences.

FIGURE 10. A FEW POSSIBLE PROGRAMMING SEQUENCES

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in anyway. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the HS-82C54RH.

There are three possible methods for reading the Counters. The first is through the Read-Back Command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A1, A0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A1, A0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC1	Counter
0	0	0
0	0	1
1	1	2
1	1	Read-Back Command

D5, D4 = 00 designates Counter Latch Command
X = Don't Care

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 11. COUNTER LATCH COMMAND FORMAT

The selected Counter's Output Latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the Counting Element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the HS-82C54RH is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The Read-Back Command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected Counter(s).

The command is written into the Control Word Register and has the format shown in Figure 12. The command applies to the Counters selected by setting their corresponding bits D3, D2, D1 = 1.

A0, A1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D5: 0 = Latch count of selected Counters(s)
D4: 0 = Latch status of selected Counters(s)
D3: 1 = Select Counter 2
D2: 1 = Select Counter 1
D1: 1 = Select Counter 0
D0: Reserved for future expansion; Must be 0

FIGURE 12. READ-BACK COMMAND FORMAT

The Read-Back Command may be used to latch multiple Counter Output Latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired Counter(s). This single command is functionally equivalent to several Counter Latch Commands, one for each Counter latched. Each Counter's latched count is held until it is read (or the Counter is reprogrammed). That Counter is automatically unlatched when read, but other Counters remain latched until they are read. If multiple count Read-Back Commands are issued to the same Counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first Read-Back Command was issued.

The Read-Back Command may also be used to latch status information of selected Counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a Counter is accessed by a read from that Counter.

The Counter status format is shown in Figure 13. Bits D5 through D0 contain the Counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the Counter's output via software, possibly eliminating some hardware from a system.

D7	D6	D5	D4	D3	D2	D1	D0
OUT PUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7 1 = Out Pin is 1
0 = Out pin is 0
D6 1 = Null count
0 = Count available for reading
D5-D0 = Counter programmed mode (See Figure 5)

FIGURE 13. STATUS BYTE

NULL COUNT bit D6 indicates when the last count written to the Counter Register (CR) has been loaded into the Counting Element (CE). The exact time this happens depends on the Mode of the Counter and is described in the Mode Definitions, but until the count is loaded into the Counting Element (CE), it can't be read from the Counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 14.

THIS ACTION:	CAUSES:
A. Write to the Control Word Register: (Note 1)	Null Count = 1
B. Write to the Count Register (CR): (Note 2)	Null Count = 1
C. New count is loaded into CE (CR $\rightarrow$ CE):	Null Count = 0

NOTES:

1. Only the Counter specified by the Control Word will have its Null Count set to 1. Null Count bits of other Counters are unaffected.
2. If the Counter is programmed for two-byte counts (least significant byte then most significant byte) Null Count goes to 1 when the second byte is written.

FIGURE 14. NULL COUNT OPERATION

If multiple status latch operations of the Counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the Counter at the time the first status Read-Back Command was issued.

Both count and status of the selected Counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5, D4 = 0. This is functionally the same as issuing two separate Read-Back Commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status Read-Back Commands are issued to the same Counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 15.

If both count and status of a Counter are latched, the first read operation of that Counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the Counter is programmed for one or two byte counts) return latched count. Subsequent reads return unlatched count.

COMMAND								DESCRIPTION	RESULT
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read-back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read-back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read-back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Command ignored, status already latched for Counter 1

FIGURE 15. READ-BACK COMMAND EXAMPLE

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

FIGURE 16. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the HS-82C54RH.

CLK PULSE:

A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:

A rising edge of a Counter's Gate input.

COUNTER LOADING:

The transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

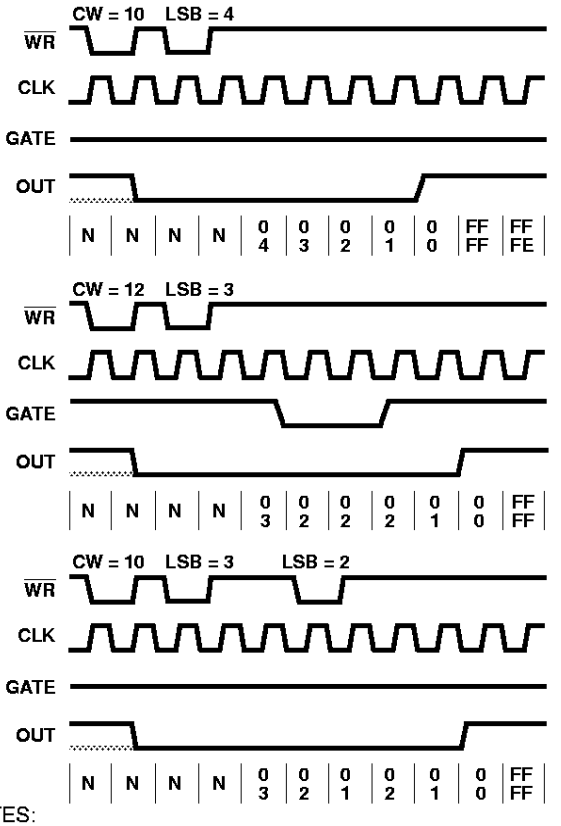
After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
2. Writing the second byte allows the new count to be loaded on next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still beloaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 17. MODE 0

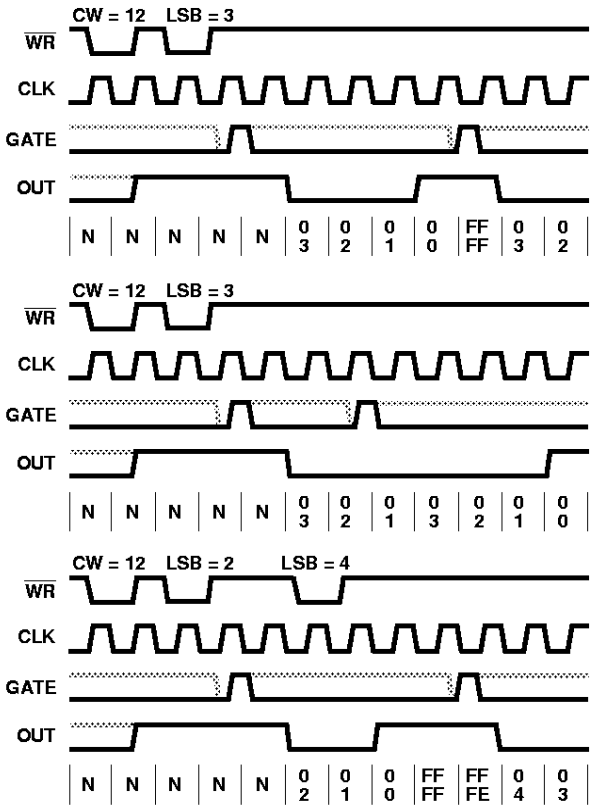
Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the Counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded

with the new count and the one-shot pulse continues until the new count expires.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 18. MODE 1

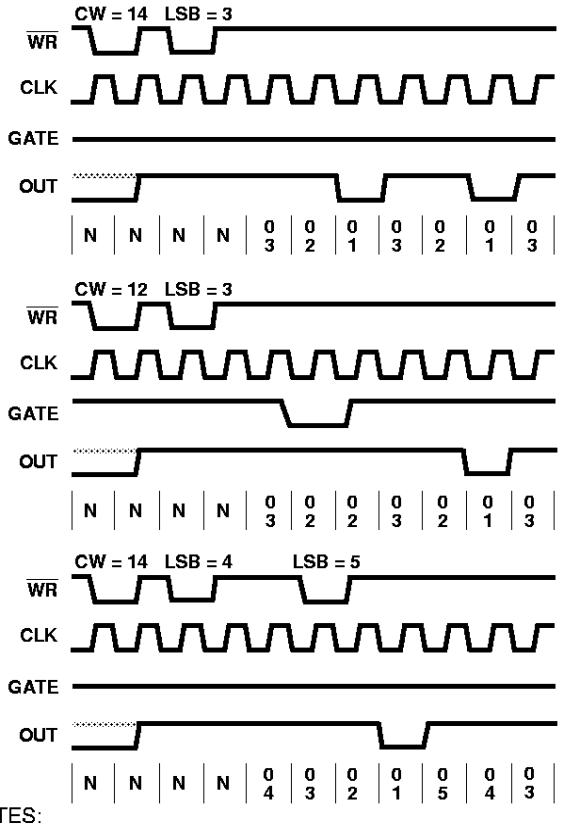
Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 19. MODE 2

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses.When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N-1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again.The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

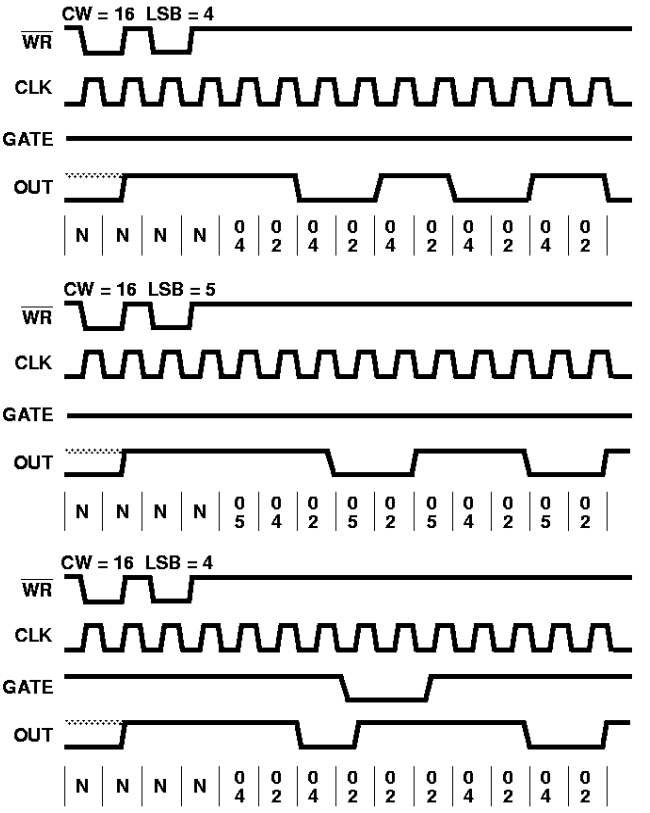
Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the Counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. This allows the counting sequence to be regretted. OUT strobes low N + 1 CLK pulses after any new trigger. GATE has no effect on the state of OUT.

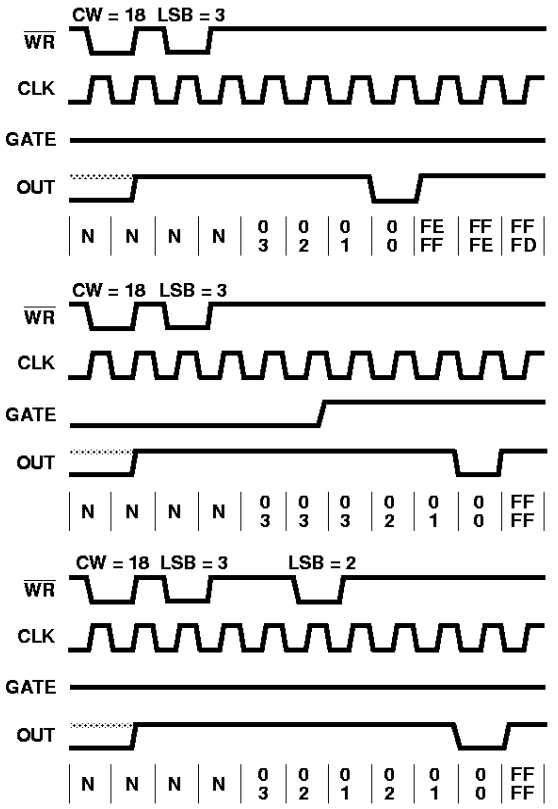
If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

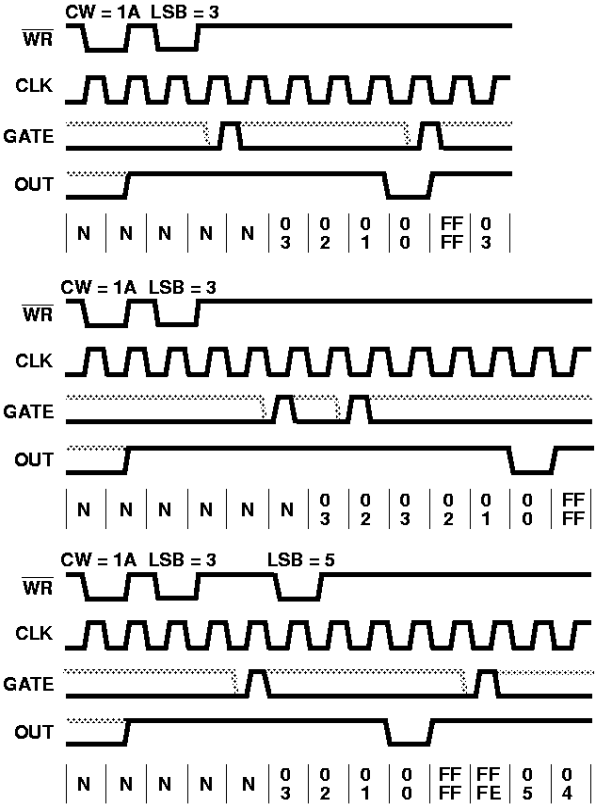
FIGURE 20. MODE 3



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 21. MODE 4



NOTES:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The Counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a Control Word of 10, Hex is written to the Counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the Counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 22. MODE 5

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The Counter does not stop when it reaches zero. In Modes 0, 1, 4 and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

GATE PIN OPERATIONS SUMMARY

SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables counting	-	Enables counting
1	-	1) Initiates counting 2) Resets output after next clock	-
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	1) Disables counting	-	Enables counting
5	-	Initiates counting	-

MINIMUM AND MAXIMUM INITIAL COUNTS

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Metallization Topology

DIE DIMENSIONS:
4700 x 5510µm x 485µm ± 25.4µm

METALLIZATION:
Type: Al/Si
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
7.9 x 10^4 A/cm^2

Metallization Mask Layout

HS-82C54RH