

SAB 82200 Local Bus Arbiter (LBA)

DMA mode

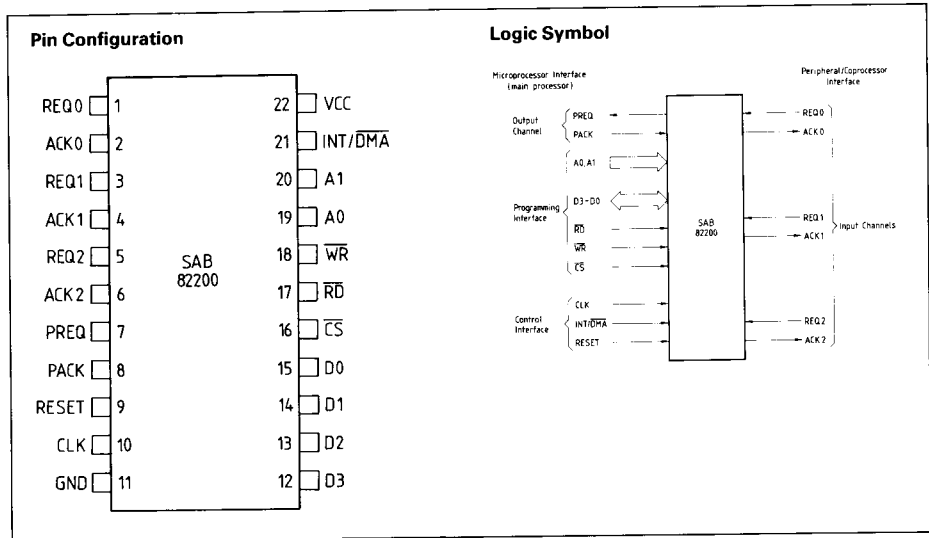
- Arbitrates local processor bus between up to four potential bus masters (CPU plus three coprocessors)

Interrupt mode

- Multiplexes up to three vectored interrupt sources to one processor interrupt channel

General features

- Flexible, programmable priority schemes
- Nested mode of operation possible
- Each input channel separately maskable
- Directly cascadable for expansion
- Glitch and race condition free operation due to synchronous logic (on-chip oscillator)



The SAB 82200 Local Bus Arbiter (LBA) is a system support component integrating functions for use in complex state-of-the-art microcomputer systems. In DMA mode it directly arbitrates the processor's local bus between the processor and up to three coprocessors, DMA controllers or peripherals with on-chip DMA controller. Easy adaption to system requirements is supported by flexible priority schemes and programmability. Arbitration for more than four bus masters is implemented by directly cascading two or more LBAs.

In interrupt mode, the LBA can be used to connect several interrupt controllers with vector capability to one processor interrupt channel without requiring compatibility with a specific cascading scheme. In interrupt mode the number of devices handled can be expanded also by cascading two or more LBAs. The flexible and programmable priority schemes are provided in this case, too. The LBA is fabricated in high-speed ASBC technology and comes in a 22-pin plastic package.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
REQ 0 – REQ 2	1, 3, 5	I	REQUEST (0 TO 2) Are the request inputs of the three input channels. A pending request must be active until it is acknowledged by the corresponding ACKn signal. Otherwise the PREQ output may glitch. The request inputs are sampled by the internal clock.
ACK 0 – ACK 2	2, 4, 6	O	ACKNOWLEDGE (0 TO 2) Are the acknowledge outputs of the input channels. The acknowledge output of the highest-priority non-masked channel with pending request is activated when PACK becomes active. The acknowledge outputs are glitch-free.
PREQ	7	O	PROCESSOR REQUEST This output is activated whenever there is a pending non-masked request on any of the request inputs. The processor request output is glitch-free if the request inputs REQn meet certain requirements.
PACK	8	I	PROCESSOR ACKNOWLEDGE The acknowledging signal for a request on PREQ is expected at this input. When the acknowledge input is activated the acknowledge output of the highest-priority channel with pending request is set high. Which channel is serviced first is decided on the rising edge of PACK (DMA mode) or on the first falling edge of PACK (interrupt mode).
RESET	9	I	RESET A high on this input sets the device into initial state.
CLK	10	I	CLOCK The CLOCK input should be connected to the bus clock of the arbitrated bus. CLK is used as timing reference only to prevent e.g. deadlock situations.
D0 – D3	12 – 15	I/O	DATA (0 TO 3) Control and status information is transferred on these bidirectional lines.
\overline{CS}	16	I	CHIP SELECT A low on this input enables read/write communication via D0 to D3 with the register selected by A0, A1.
\overline{RD}	17	I	READ CONTROL If \overline{CS} is low, a low on this input gates the contents of the selected register (A0, A1) to D0 to D3.
WR	18	I	WRITE CONTROL If \overline{CS} is low, a low on this input latches the data from D0 to D3 into the selected (A0, A1) register.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A0, A1	19, 20	I	ADDRESS LINE (0, 1) These inputs select the internal registers while \overline{CS} is active.
INT/DMA	21	I	INTERRUPT/DMA MODE This is a static operating mode strapping input. If tied low the DMA mode is selected; if high the interrupt mode is selected.
GND	11		GROUND (0V)
VCC	22		POWER SUPPLY (+5V)

Functional Description

Basic Operating Modes

The LBA has two basic operating modes

- DMA mode and
- interrupt mode.

In DMA mode the LBA is configured to handle HOLD/HLDA lines, in interrupt mode to handle INT/INTA lines.

In interrupt mode, the channel acknowledge lines exactly follow the actions on the processor acknowledge line PACK, whereas in DMA mode this is not necessarily the case.

Channel Priority

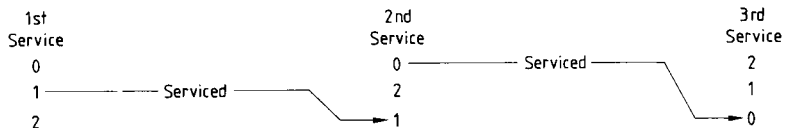
The decision which channel is acknowledged when the processor activates PACK depends on the priority of the channels. Two priority modes are programmable:

- Fixed priority
Channel 0 has highest, channel 2 lowest priority.
- Full rotating priority
In the beginning the priority scheme is the same as with fixed priority. The last channel serviced becomes the channel of lowest priority with the others shifted accordingly (see figure 1).

The resulting new channel priorities are assigned at the end of the acknowledge cycle performed on the serviced channel.

The priority modes are programmed via the command register.

Figure 1
Rotating Priority Scheme



Channel Service

DMA Mode

The DMA mode is selected by connecting pin INT/ $\overline{\text{DMA}}$ to ground. In DMA mode the LBA is intended to handle HOLD/HLDA signal pairs.

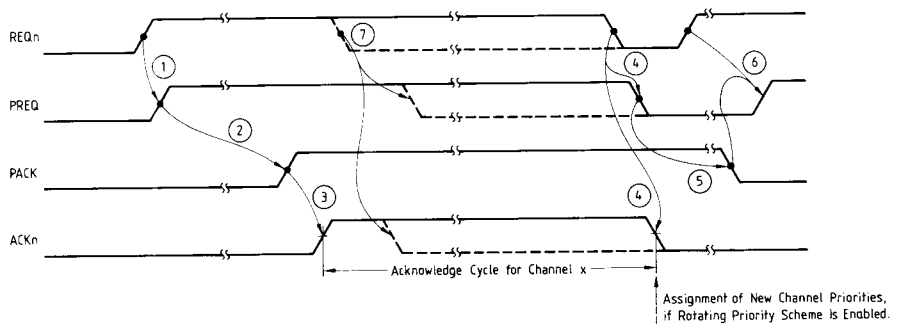
Single-channel operation

If the request line of an enabled channel is activated and no other channel is active at that time, the processor request line PREQ is set active high.

When the processor has relinquished control of the bus it must activate the PACK signal.

This causes the appropriate channel acknowledge signal to be activated (see figure 2). If the rotating priority scheme is selected, the new channel priorities are assigned at the end of the channel acknowledge cycle (falling edge of ACKn).

Figure 2
DMA Mode, Single-Channel Operation



- ① Activation of request input directly activates PREQ.
- ② When the processor has released the bus it activates PACK.
- ③ This acknowledge is immediately passed to the channel output ACKn.
- ④ ⑤ When the peripheral has finished its transfers, it deactivates the request. This causes PREQ and ACKn also to be deactivated and the processor can gain the control over the bus again.
- ⑥ A request activated in the time frame between deactivation of PREQ and PACK is processed only after the deactivation of PACK.
- ⑦ If REQn is deactivated ACKn is deactivated immediately, too. (No minimum ACKn high time).

Multiple channel operation

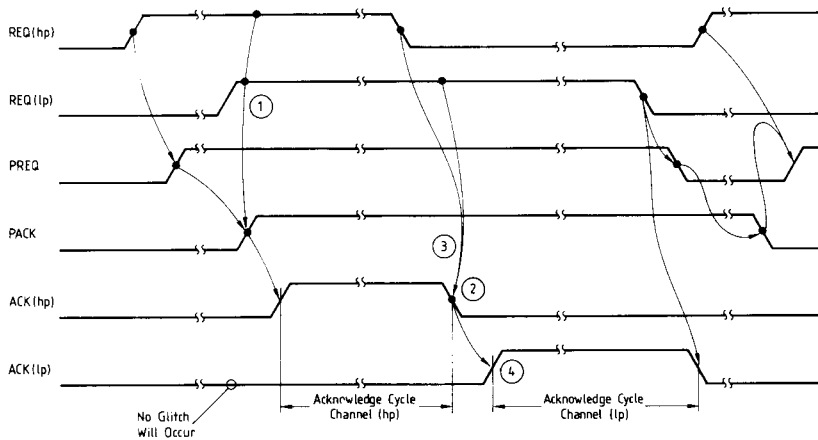
● **Non-nested mode**

If there is more than one request pending when the processor releases the bus, the highest priority request is acknowledged (see figure 3).

If the rotating priority scheme is selected, the new channel priorities are assigned at the end of the

acknowledge cycle of the highest priority request. When this acknowledge cycle is finished, the now highest priority request is acknowledged. This sequence will be continued as long as non-masked requests are pending.

Figure 3
DMA Mode, Multiple Channel Operation, Non-Nested Mode



- ① With the rising edge of PACK the highest priority request is acknowledged.
- ② With the falling edge of channel acknowledge ACK (hp) the new channel priorities are assigned if rotating priority is enabled.
- ③ With the falling edge of the highest priority acknowledge the pending request with the currently (new) highest priority is acknowledged.
- ④ The new channel priorities assigned if rotating priority is selected.

hp = highest priority
lp = lowest priority

If there is already an active channel the new request will be acknowledged as soon as it becomes the highest priority request. The active channel will not be interrupted if the new request has higher priority as the active one.

● **Nested mode**

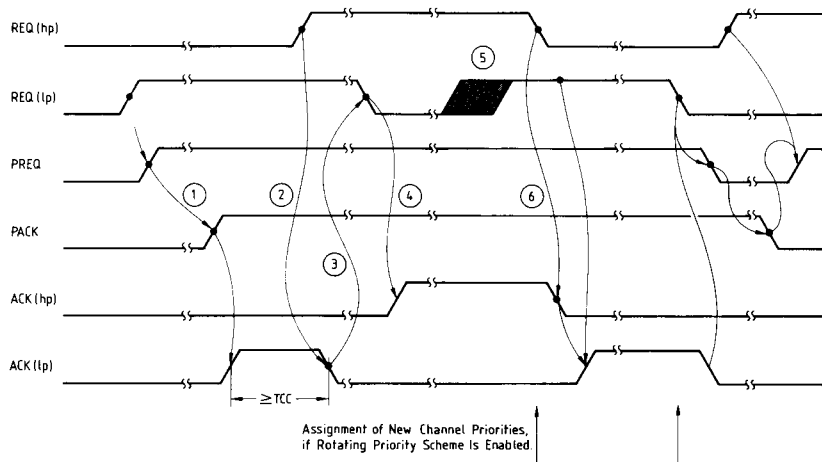
In nested mode, a higher priority request can interrupt a lower priority channel. This is done by deactivating the peripheral acknowledge line. Most DMA controllers and peripherals with integrated DMA controllers release the bus and drop the request line when their DMA acknowledge input is

deactivated. Thus a higher priority bus master can gain control over the bus (see figure 4).

To avoid deadlock situations an activated ACK line has to stay active until the coprocessor has recognized this activation. Therefore, the minimum time frame within which an activated ACK line remains in the high state is programmable from 1 to 4 CLK cycles.

If the rotating priority scheme is enabled, the assignment of the new channel priorities in nested mode is done upon deactivation of a request that has not been disrupted by a higher priority channel.

Figure 4
DMA Mode, Multiple Channel Operation, Nested Mode



- ① A lower priority peripheral gets control of the bus.
- ② A higher priority request causes the LBA to drop the lower priority acknowledge.
- ③ The peripheral releases the bus and drops the request line.
- ④ Now the higher priority request can be acknowledged.
- ⑤ The disrupted peripheral normally raises its request line again to continue.
- ⑥ After the higher priority peripheral has finished, the now highest priority request is processed.

To avoid deadlock situations an acknowledge has to remain in high state for a minimum time frame. This time programmable from 1 to 4 CLK cycles.

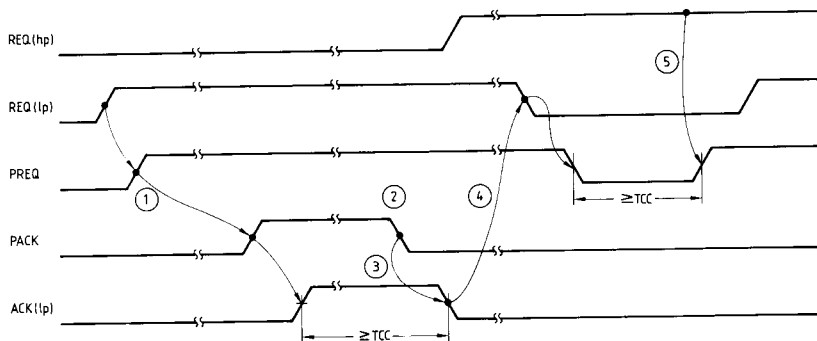
hp = highest priority
lp = lowest priority

● Premature deactivation of PACK

An active channel can be stopped by the premature deactivation of PACK, too. For each channel this PACK stop feature can be individually enabled or disabled via the PACK channel control register.

If the PACK stop is enabled for a channel and this channel is active, its ACK line is dropped when the PACK line goes inactive (see figure 5).

Figure 5
Premature Deactivation of PACK



- ① A peripheral gets control of the bus.
- ② Another (higher-priority) bus master needs the bus – PACK is deactivated.
- ③ If the PACK channel control is enabled the channel acknowledge line is deactivated. A minimum high time of TCC is guaranteed.
- ④ This causes the peripheral to release the bus.
- ⑤ Subsequent requests are processed only after PREQ was inactive for a certain amount of time to ensure proper synchronization.

hp = highest priority
lp = lowest priority

After the peripheral has dropped its request the PREQ output is deactivated to signal the release of the bus.

A subsequent channel request, occurring in the time frame between the deactivation of PACK and PREQ, is processed only after the PREQ output has

been inactive for a certain amount of time. This time TCC is programmable from 1 to 4 CLK cycles.

If the active channel has disabled the premature deactivation, the PREQ output will go inactive after the request is deactivated.

Interrupt Mode

The interrupt mode is selected by connecting pin INT/DMA to VCC. In interrupt mode the LBA is intended to handle INT/INTA signal pairs.

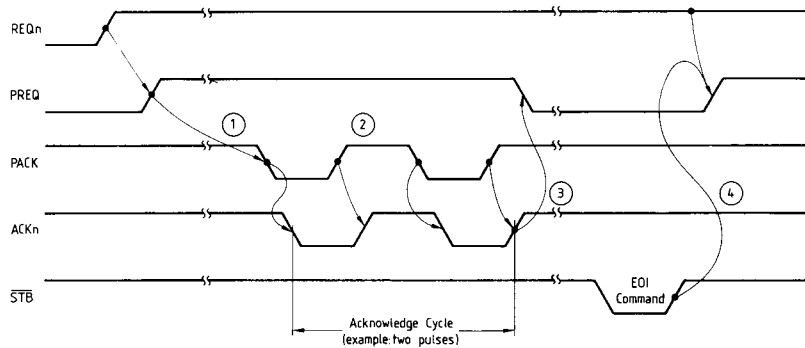
Single-channel operation

If the request line of an enabled channel is activated the processor request line PREQ is immediately set to active high. When the processor acknowledges

the interrupt request with the interrupt acknowledge pulse(s) on PACK they are immediately passed to the channel with the pending request (see figure 6).

During the acknowledge cycle no other requests are accepted. The acknowledge cycle lasts from the beginning of the first acknowledge pulse to the end of the last pulse. The number of pulses within on acknowledge cycle is programmable.

Figure 6
Interrupt Mode, Single-Channel Operation



- ① A request at one of the request inputs is passed to the CPU via PREQ.
- ② This causes the CPU to respond with an interrupt acknowledge cycle consisting of one or more INTA pulses.
- ③ At the end of the acknowledge cycle the PREQ output is deactivated regardless of the state of the request input (the related bit in the in-service register ISR is set).
- ④ After getting an EOI (end of interrupt) command for this channel (bit in ISR is reset) further requests on this channel are reenabled.

If no request is pending when the acknowledge cycle starts (premature deactivation of request), the acknowledge pulse(s) on PACK will not be passed to an output channel. If the request is deactivated while an acknowledge cycle is running, the cycle is aborted immediately on the peripheral channel (i.e. ACKn glitches are possible in this case).

At the end of the acknowledge cycle (rising edge of last pulse), the PREQ output is deactivated and the serviced channel is disabled by setting the related bit in the in-service register ISR.

Further requests on this channel are processed only after this bit has been reset by an EOI command.

Multiple channel operation

- Non nested mode

In the non-nested mode every enabled request is transferred to the processor regardless of the priority.

The priority scheme only decides which request is processed first if more than one request is active at the falling edge of the first pulse on PACK (see figure 7).

Every acknowledged request is disabled until it is reenabled by a specific EOI command defining which channel has to be reenabled. Thus a dynamic channel priority scheme can be implemented by software.

If the rotating priority scheme is selected, the new channel priorities are assigned at the end of each acknowledge cycle.

- Nested Mode

In the nested mode a request is transferred only if it is the currently highest-priority non-masked request and no higher priority request is being serviced.

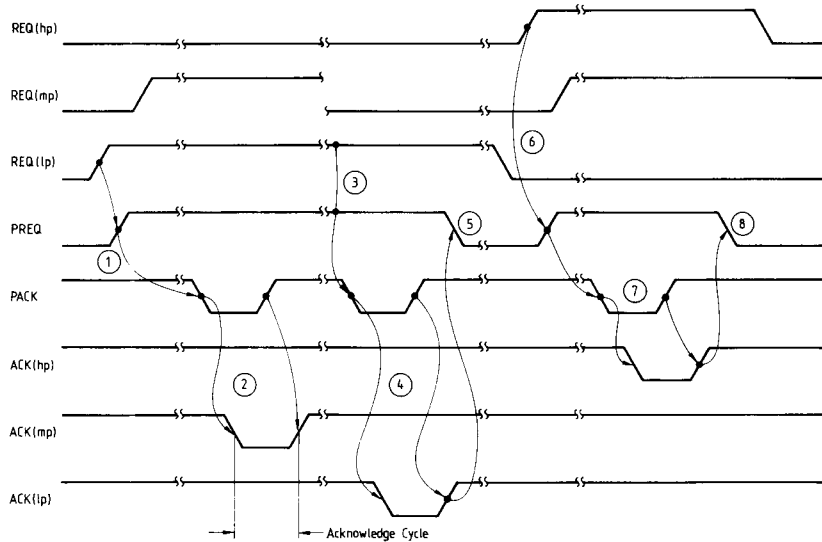
This means, that if more than one request is pending at the beginning of the acknowledge cycle only the highest priority request is serviced. The other request(s) is serviced only after the in-service bit of this request has been reset by an EOI command.

If a subsequent request has a higher priority than the highest request that is currently in-service, it will be transferred to the CPU (see figure 8).

In general, each request is masked by the in-service bits set related to its own level and of higher levels. The in-service bits can be reset by a non-specific EOI command (the highest priority bit that is set will be reset) or a specific EOI command (the bit specified in the command is reset).

In case of nested-mode fixed priority is automatically selected, no rotating priority is possible.

Figure 7
Interrupt Mode, Multiple Channel Operating, Non-Nested Mode

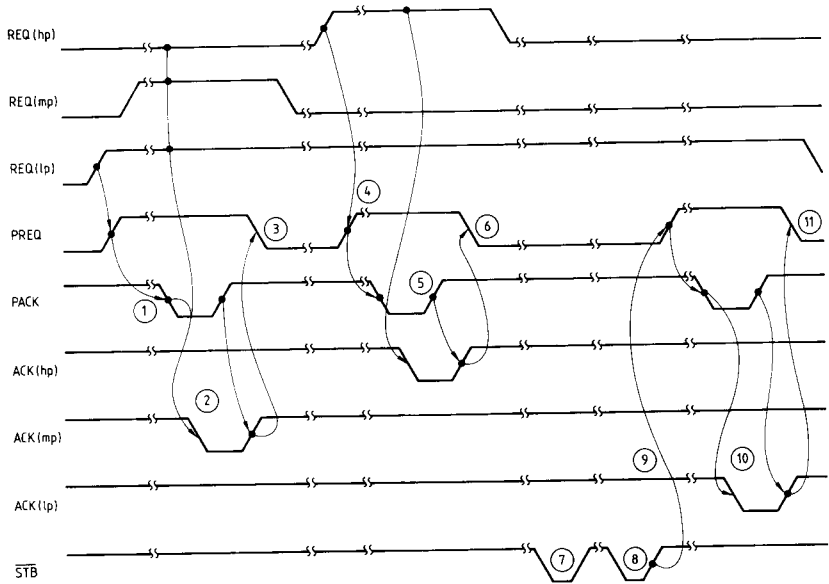


Assumptions: all request inputs enabled, 1 pulse acknowledge cycle, fixed priority.

- ① A pending request is passed to the CPU.
- ② The request with the highest priority at the beginning of the acknowledge cycle (falling edge of PACK) is serviced.
- ③ PREQ stays in active state because another unmasked, unacknowledged request is pending.
- ④ The second request is acknowledged.
- ⑤ PREQ is deactivated because no unmasked request is pending. REQ (lp) is masked via its in-service bit.
- ⑥, ⑦ REQ (hp) is transferred to the CPU and acknowledged.
- ⑧ PREQ goes inactive regardless of the pending request REQ (mp) because its still masked via its in-service bit. Further requests will be processed only when the appropriate in-service bits will be reset by a specific EOI command.

hp = highest priority
 mp = medium priority
 lp = lowest priority

Figure 8
Interrupt Mode, Multiple Channel Operation, Nested Mode



Assume fixed priority, channels enabled.

- ① A request at REQ (lp) is passed to the CPU.
 - ② The acknowledge signal from the CPU is passed to the highest priority request pending (REQ (mp)).
 - ③ PREQ is deactivated because no request with higher priority than the highest in-service request is pending.
 - ④ REQ (hp) is passed to the CPU because it has higher priority than the highest in-service request.
 - ⑤ The request is acknowledged.
 - ⑥ PREQ is deactivated (see ④).
 - ⑦ EOI command for highest priority level is issued.
 - ⑧ EOI command for medium priority level is issued.
 - ⑨ No higher request than REQ (lp) is being serviced or pending thus it is passed to the processor.
 - ⑩ The request is acknowledged.
 - ⑪ PREQ is deactivated because no unserviced request is pending.
- hp = highest priority
 mp = medium priority
 lp = lowest priority

$\overline{\text{INTA}}$ cycle conversion mode

For easy connection of interrupt vector sources requiring only one $\overline{\text{INTA}}$ pulse with processors that issue two $\overline{\text{INTA}}$ pulses, the LBA can be set into the $\overline{\text{INTA}}$ cycle conversion mode.

In this mode the first of the two $\overline{\text{INTA}}$ pulses on $\overline{\text{PACK}}$ is suppressed when passed to channel 1 or channel 2. Only the second pulse (related to the transfer of the interrupt vector) is passed to ACK1 or ACK2.

However, both $\overline{\text{INTA}}$ pulses will be issued on channel 0 in order to still have the possibility of connecting standard interrupt controllers or of cascading LBAs in this mode.

Cascading SAB 82200 Local Bus Arbiters

Two or more LBAs can easily be cascaded by connecting the PREQ/PACK lines to an input channel of another LBA.

In DMA mode, this daisy chaining has only effect on the response time. In interrupt mode, the skew between the request pulses (INTA pulses) and the associated data (cascade information, interrupt vector) limits the number of cascaded LBAs.

The nested DMA mode is supported by the possibility of deactivating an active channel if PACK is lost.

Programming the SAB 82200 Local Bus Arbiter

The LBA contains several registers that allow software control of most of the LBA's functions:

Write Registers	Read Registers
1) Command Register	1) Command Register
2) Channel Mask Register	2) Channel Mask Register
3) Channel Control Register (DMA mode only)	3) Channel Control Register (DMA mode only)
End-of-Interrupt Register (interrupt mode only)	In-service Status Register (interrupt mode only)
	4) Request Status Register

The basic operating modes are defined using the command register; with the channel mask register each of the three channels can be disabled separately.

The third register has a different meaning for interrupt mode and for DMA mode. In interrupt mode it is used for EOI commands, in DMA mode as control register to enable and disable the premature channel deactivation via PACK.

The read registers show the status of the device: the programming; which requests are pending; which channels are enabled (DMA mode); and which request levels are just in-service (interrupt mode). The following sections detail the registers separately for DMA mode and interrupt mode.

Programming in DMA Mode

The DMA mode of the LBA is selected by connecting the INT/DMA input to ground. The following tables show the register definitions for DMA mode.

Register selection

The LBA registers in DMA mode are accessed according to the following table:

CS	A1	A0	RD	WR	Register
0	0	0	1	0	Command Register
0	0	1	1	0	Channel Mask Register
0	1	0	1	0	Channel Control Register
0	1	1	1	0	Reserved
0	0	0	0	1	Command Register
0	0	1	0	1	Channel Mask Register
0	1	0	0	1	Channel Control Register
0	1	1	0	1	Request Status Register
1	X	X	X	X	No Access

Command register (CR)

The operating mode of the LBA is defined with the command register.

D3	D2	D1	D0
C1	C0	NNM	PM

● **PM: Priority mode**

PM = 0: Fixed priority
PM = 1: Rotating priority

● **NNM: Non-nested mode enable**

NNM = 0: Nested mode
NNM = 1: Non-nested mode

● **C1, C0: Cycle count value**

These bits define the value of the timing parameter TCC.

C1	C0	Length of TCC
0	0	2 CLK Cycles
0	1	4 CLK Cycles
1	0	1 CLK Cycles
1	1	3 CLK Cycles

Channel mask register (CMR)

Each channel can be enabled and disabled separately using the channel mask register.

D3	D2	D1	D0
DISC	DIS2	DIS1	DIS0

● **DISn: Channel enable/disable**

DISn = 0: Channel n enabled
 DISn = 1: Channel n disabled

● **DISC: Disable chip**

DISC = 0: The channels are enabled or disabled according to D0–D2.
 DISC = 1: All channels are disabled, regardless of the status of D0–D2.

Channel control register (CCR)

The premature deactivation of the channel upon the premature deactivation of PACK can be enabled or disabled separately using the channel control register.

D3	D2	D1	D0
O	PCC2	PCC1	PCC0

● **PCCn: PACK channel control for channel n**

PCCn = 0: PACK channel control for channel n is enabled.
 PCCn = 1: PACK channel control for channel n is disabled.

Request status register (RSR)

Reading the request status register gates the physical state of the request inputs onto the data lines.

D3	D2	D1	D0
X	REQ2	REQ1	REQ0

REQn = 0: Low input level on pin REQn
 REQn = 1: High input level on pin REQn

Reading the channel mask and channel control registers

On reading these registers the contents of the selected register is gated onto the data bus.

Programming in Interrupt Mode

The interrupt mode of the LBA is selected by connecting the INT/DMA input to VCC. The following tables show the register definitions for the interrupt mode.

Register selection

The LBA registers are accessed according to the following table:

CS	A1	A0	RD	WR	Register
0	0	0	1	0	Command Register
0	0	1	1	0	Channel Mask Register
0	1	0	1	0	End-of-Interrupt Register
0	1	1	1	0	– Reserved –
0	0	0	0	1	Command Register
0	0	1	0	1	Channel Mask Register
0	1	0	0	1	In-Service Register
0	1	1	0	1	Request Status Register
1	X	X	X	X	No Access

Command register

The operating mode of the LBA is defined with the command register.

D3	D2	D1	D0
C1	C0	NNM	PM

PM: Priority mode
 NNM: Non-nested mode

NNM	PM	Mode
0	X	Nested Mode, Fixed Priority
1	0	Non-Nested, Fixed Priority
1	1	Non-Nested, Rotating Priority

● **C1, C0: Acknowledge cycle definition**

These bits define the number of the processor interrupt acknowledge pulses on PACK and the number of acknowledge pulses on ACKn. In the case of reduction in pulse count the first pulse of PACK is suppressed.

C1	C0	Processor Acknowledge Cycle Count	Peripheral Acknowledge
0	0	PACK: 2	ACKn: 2 ¹⁾
1	0	PACK: 1	ACKn: 1
0	1	PACK: 2	ACK0: 2 ACK1,2: 1
1	1	PACK: 2	ACKn: 1

¹⁾ Default after reset

Channel mask register

Each channel can be enabled and disabled separately using the channel mask register.

DISC	D2	D1	D0
DISC	DIS2	DIS1	DIS0

● **DISn: Channel enable/disable**

DISn = 0: Channel n enabled
 DISn = 1: Channel n disabled

● **DISC: Disable chip**

DISC = 0: The channels are enabled or disabled according to D0–D2.
 DISC = 1: All channels are disabled regardless of the status of D0–D2.

End-of-interrupt register

The end-of-interrupt (EOI) register is required to reset the in-service bits of the different channels.

D3	D2	D1	D0
RHPI	RIS2	RIS1	RIS0

● **RISn: Reset in-service bit n**

RHPI	RIS2	RIS1	RIS0	Action	Type
0	0	0	1	Reset In-Service Bit 0	Specific EOI Commands
0	0	1	0	Reset In-Service Bit 1	
0	1	0	0	Reset In-Service Bit 2	
1	x	x	x	Reset Highest Priority In-Service Bit that Is Set	Non-Specific EOI Command

If no in-service bit is set in the in-service register, a write operation to the EOI register is like a NOP.
 If non-nested mode is programmed, a non-specific EOI acts like a NOP.
 If the RHPI bit is set, setting of RISn bits has no effect.

Request status register

Reading the request status register gates the physical state of the request inputs onto the data bus.

D3	D2	D1	D0
X	REQ2	REQ1	REQ0

REQn = 0: Low input level on pin REQn
 REQn = 1: High input level on pin REQn

In-service status register

Reading the in-service status register gates the state of the in-service bits onto the data bus.

D3	D2	D1	D0
X	ISB2	ISB1	ISB0

● **ISBn: In-service bit n**

ISBn = 0: Channel n is not being serviced
 ISBn = 1: Channel n is serviced
 (a request has been acknowledged and no EOI command for this channel has been given yet)

Reading the command and channel mask register

On reading these registers the content of the selected register is gated onto the data bus D0–D3.

Reset

A high level on the RESET input sets the LBA into a defined state.

In the **DMA mode** this initial state is:

- all channels enabled
- fixed priority
- non-nested mode
- premature channel deactivation via PACK disabled
- TCC = 2 CLK cycles
- PREQ line inactive

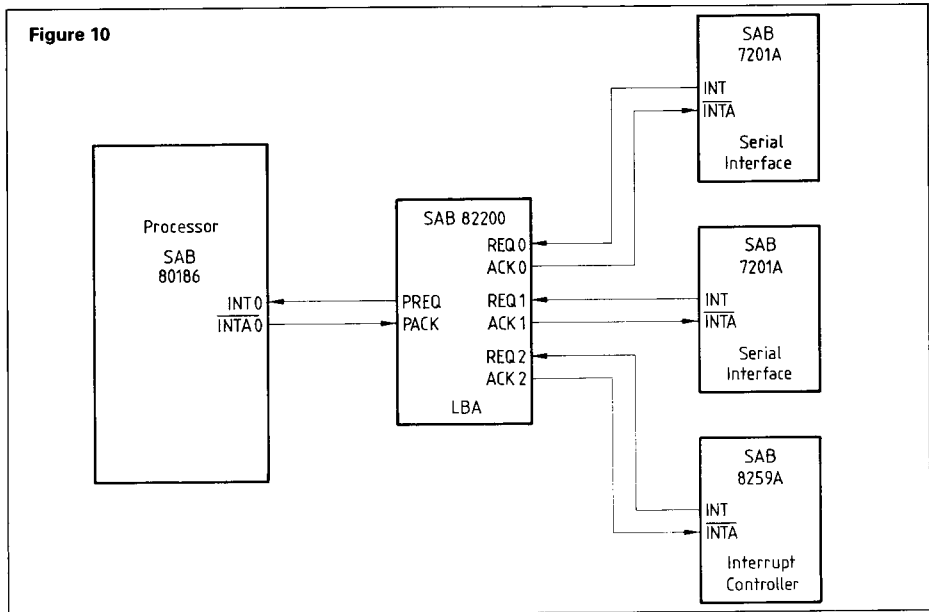
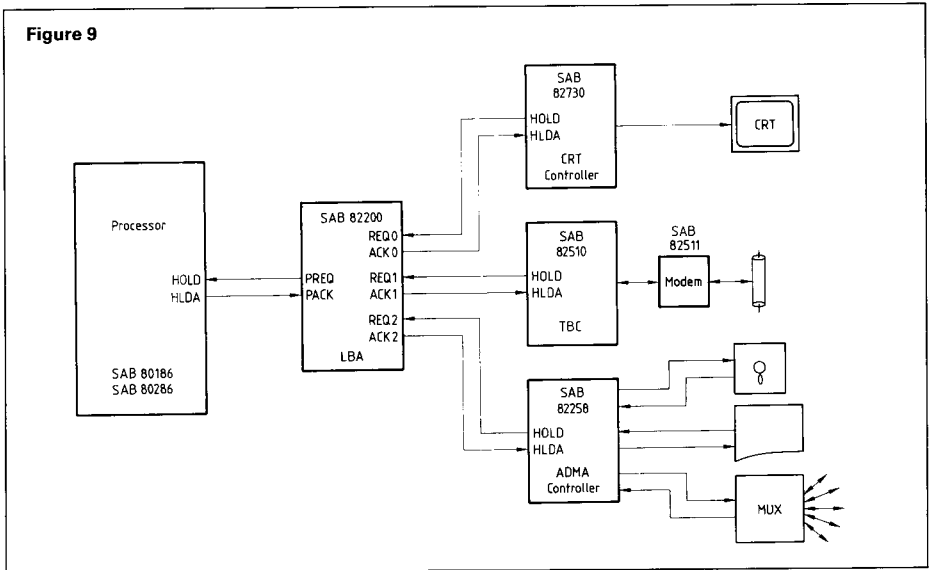
In **interrupt mode** the initial state is:

- all channels enabled
- fixed priority
- nested mode
- acknowledge cycle length is two pulses
- PREQ line inactive

If this initial state is applicable no further programming is necessary.

Circuit Examples

Figures 9 and 10 show two possible applications



Absolute Maximum Ratings¹⁾

Temperature under bias	0 to +70°C
Storage temperature	-65 to +125°C
All output and supply voltages	-0.5 to +7V
All input voltages	-1.0 to +5.5V
Power dissipation	1W

DC Characteristics

TA = 0 to 70°C, VCC = +5V ±10%

Symbol	Parameter	Limit values		Unit	Test Conditions
		min.	max.		
VC	Input clamp voltage	-	-1	V	IC = -5 mA
ICC	Power supply current	-	145	mA	VCC = 5.5 V, all outputs open; TA = 25°C
IF	Forward input current	-	-0.2	mA	VF = 0.45 V
IR	Reverse input current	-	50	µA	VR = VCC
VOL	Output low voltage, D0-D3 other outputs	-	0.45	V	IOL=32 mA, CL=300 pF IOL=10 mA, CL=100 pF
VOH	Output high voltage, D0-D3 other outputs	2.4	-	V	IOH=-5 mA, CL=300 pF IOH=-1 mA, CL=100 pF
IOFF	Output off current	-	±50	µA	VOFF = 0.45 to VCC
VIL	Input low voltage	-	0.8	V	-
VIH	Input high voltage	2.0	-	V	-
CIN	Input capacitance	-	12	pF	f = 1 MHz VBIAS=2.5 V, VCC=5V TA = 25°C
CIO	Input/output capacitance	-	20	pF	f = 1 MHz VBIAS=2.5 V, VCC=5V TA = 25°C

¹⁾ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

TA = 0 to 70°C, VCC = +5V ±10%

Symbol	Parameter	Limit values		Unit
		min.	max.	
t1	\overline{RD} or \overline{WR} pulse width	100	–	ns
t2	Address and \overline{CS} setup time to \overline{RD} ↓ or \overline{WR} ↓	10	–	ns
t3	Address and \overline{CS} hold time after \overline{RD} ↑ or \overline{WR} ↑	0	–	ns
t4	Data setup time to \overline{WR} ↑	50	–	ns
t5	Data hold time after \overline{WR} ↑	10	–	ns
t6	Data valid after \overline{RD} ↓	–	60	ns
t7	Data bus active after \overline{RD} ↓	20	–	ns
t8	Request setup time for recognition as highest priority request	100	–	ns
t9	PACK ↓ (premature) till ACK(n) ↓	–	150	ns
t10	Data valid after \overline{RD} ↑	10	–	ns
t11	Data bus inactive after \overline{RD} ↑	–	60	ns
t12	REQn ↑ to PREQ ↑	–	180	ns
t13	PACK ↑ to ACKn ↑ (DMA mode)	–	170	ns
t14	ACKn high time (DMA mode)	¹⁾	–	ns
t15	REQ(hp) ↑ to ACK(lp) ↓ (DMA mode)	–	270	ns
t16	REQ(lp) ↓ to ACK(hp) ↑ (DMA mode)	–	180	ns
t17	REQn low time (DMA mode)	250	–	ns
t18	REQn ↓ to ACKn ↓ (DMA mode)	–	240	ns
t19	REQ(hp) ↓ to ACK(lp) ↑ (DMA mode)	120	290	ns
t20	REQn ↓ to PREQ ↑ (DMA mode)	–	160	ns
t21	PACK ↓ to PREQ ↑ again (request pending)	45	210	ns
t22	PACK ↓ to ACKn ↓ (interrupt mode)	–	55	ns
t23	PACK low time (interrupt mode)	50	–	ns
t24	PACK ↑ to ACKn ↑ (interrupt mode)	–	50	ns
t25	End of acknowledge cycle (ACKn ↑) to PREQ ↓	–	100	ns
t26	EOI command (\overline{WR} ↑) to PREQ ↑ again (request pending, interrupt mode)	–	110	ns

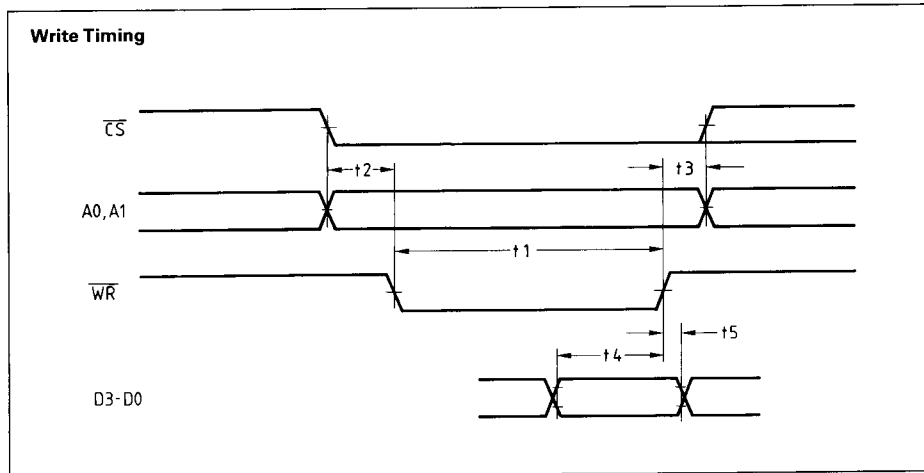
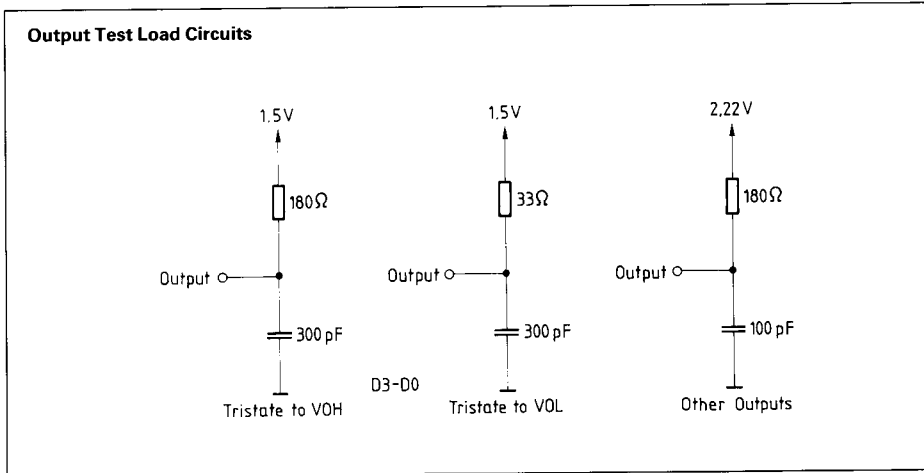
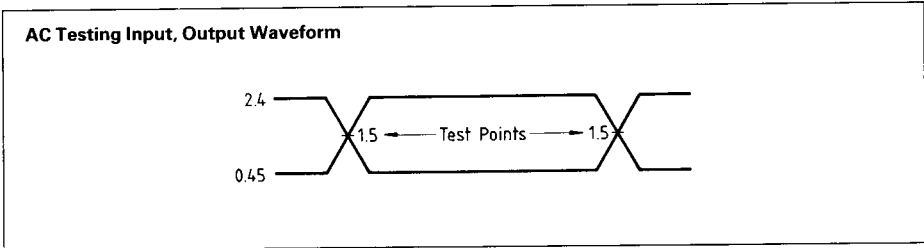
¹⁾ TCC is programmable from 1 to 4 CLK cycles.

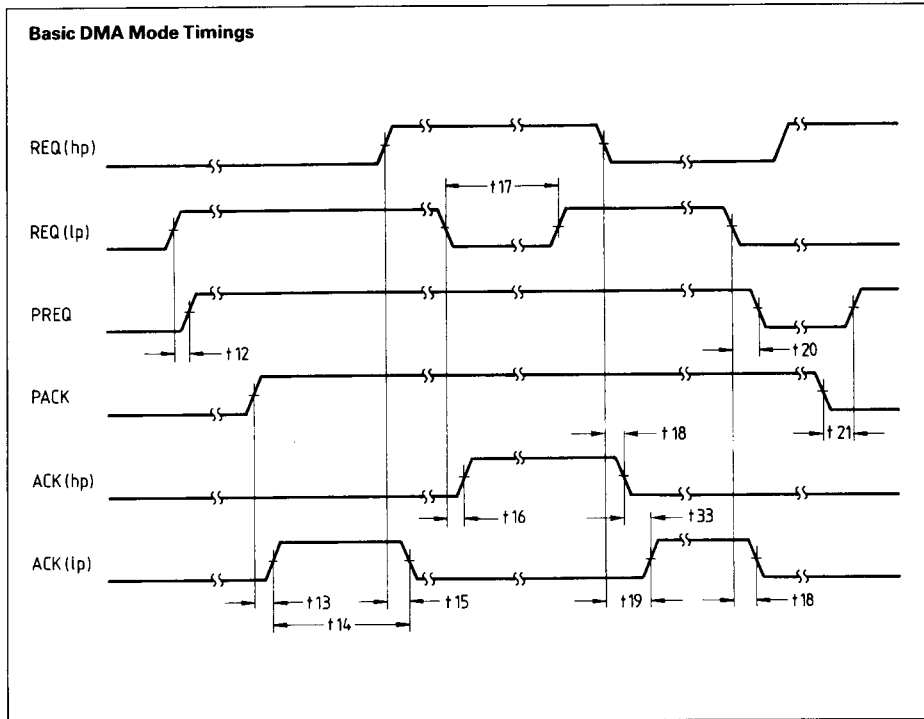
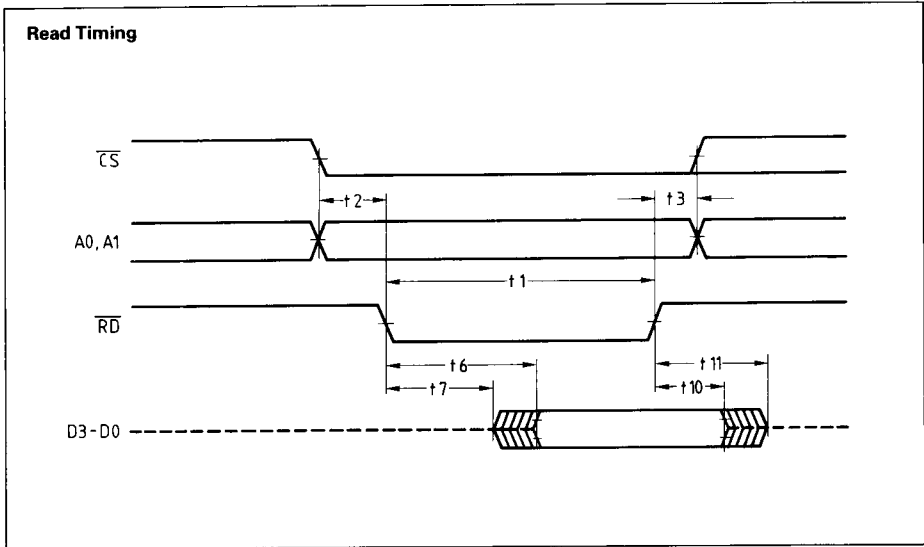
AC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit
		min.	max.	
t27	CLK cycle time	50	–	ns
t28	CLK high time	20	–	ns
t29	CLK low time	20	–	ns
t30	RESET high time	200	–	ns
t31	PREQ minimum low time (DMA mode)	¹⁾	–	ns
t32	PACK minimum high time (interrupt mode)	70	–	ns
t33	Minimum time interval between two active acknowledge outputs	15	–	ns
t34	Processor acknowledge minimum high time (DMA mode)	100	–	ns
t35	PREQ ↑ to PACK ↓ (interrupt mode)	200	–	ns
t36	REQn minimum high time for recognition	100	–	ns
t37	PACK minimum high time between different cycles	270	–	ns

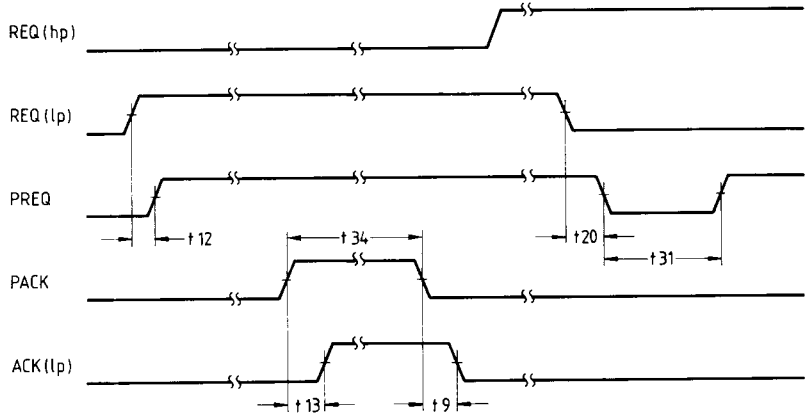
¹⁾ TCC is programmable from 1 to 4 CLK cycles.

Waveforms

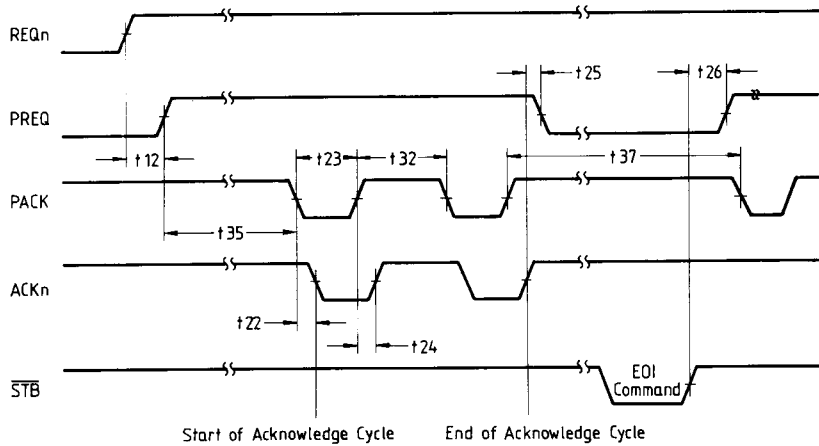


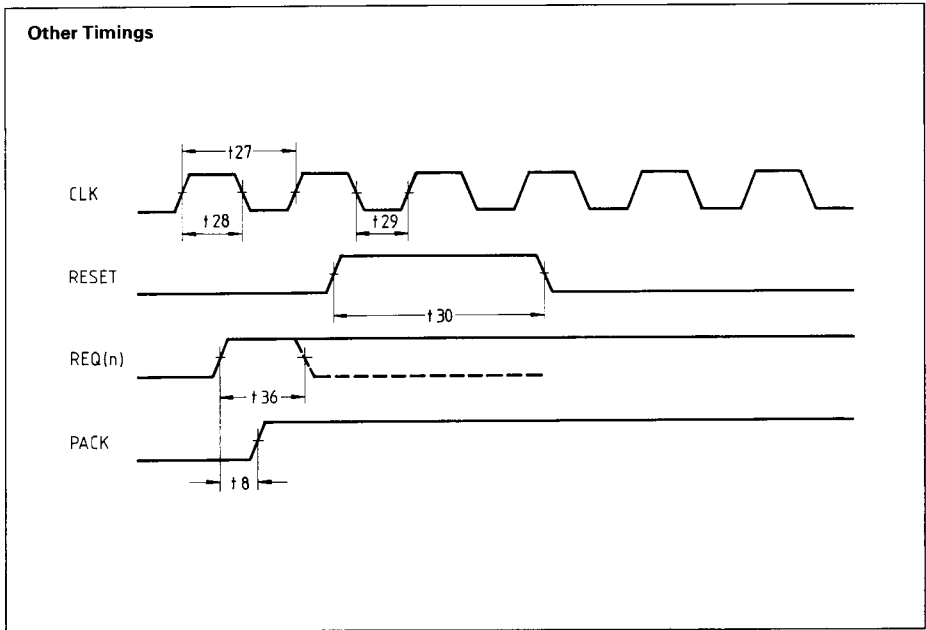


Premature Deactivation of PACK



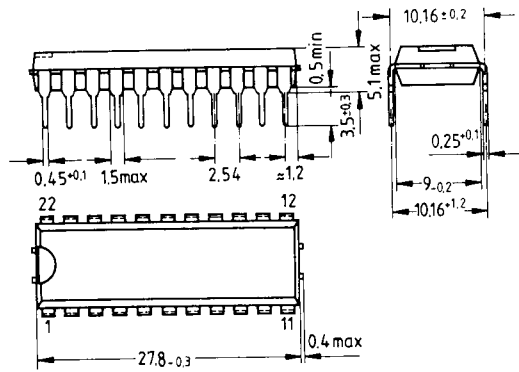
Interrupt Mode Timings





Package Outline

Plastic Package, DIP, 22 pins



Dimensions in mm

SAB 82200

Ordering Information

Type	Ordering code	Description
SAB 82200-P	Q67020-Y171	Local bus arbiter