

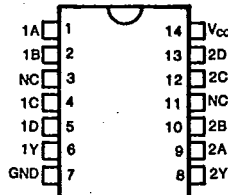
**KS54HCTLS
KS74HCTLS 20**

T-43-21
Dual 4-Input NAND Gates

FEATURES

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74HCTLS: -40°C to +85°C
KS54HCTLS: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



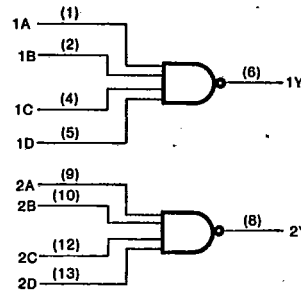
DESCRIPTION

These devices contain two independent 4-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A + B + C + D}$ in positive logic.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{cc} and ground.

LOGIC DIAGRAM



FUNCTION TABLE

(Each gate)

INPUTS				OUTPUT Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

KS54HCTLS 20
KS74HCTLS

Dual 4-Input NAND Gates

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} -65°C to $+150^\circ\text{C}$
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): $-12\text{mW}/^\circ\text{C}$ from 65°C to 85°C
 Ceramic Package (J): $-12\text{mW}/^\circ\text{C}$ from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage* V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN}, V_{OUT} .. 0V to V_{CC}
 Operating Temperature
 Range KS74HCTLS: -40°C to $+85^\circ\text{C}$
 KS54HCTLS: -55°C to $+125^\circ\text{C}$
 Input Rise & Fall Times, t_r, t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$			Unit	
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		2.0	20.0	40.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	mA

AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 6$ ns), HCTLS20

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0V$			Unit
			Typ	KS74HCTLS $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	KS54HCTLS $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $V_{CC} = 5.0V \pm 10\%$	
Maximum Propagation Delay Any Input to Y	t_{PLH}	$C_L = 50\text{pF}$	11	15	19	ns
	t_{PHL}		11	15	19	
Maximum Input Capacitance	C_{IN}		5			pF
Power Dissipation Capacitance*	C_{PD}	(per gate)				pF

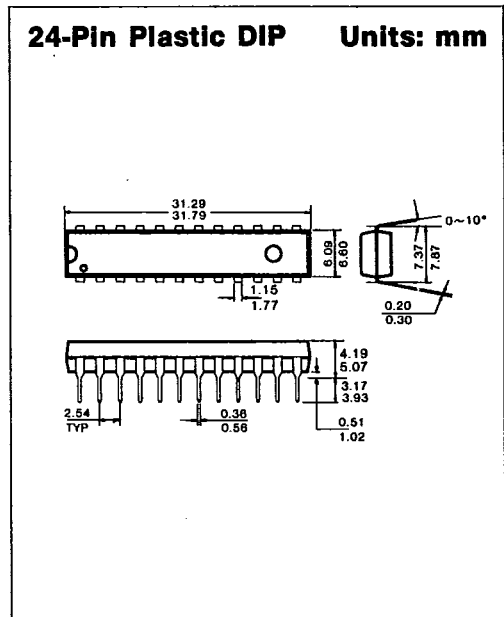
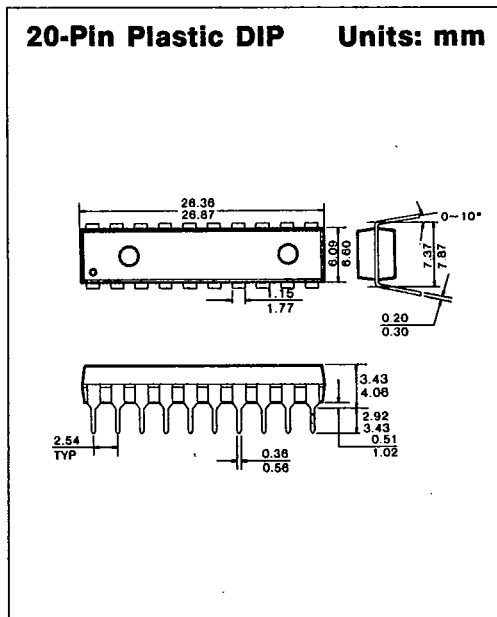
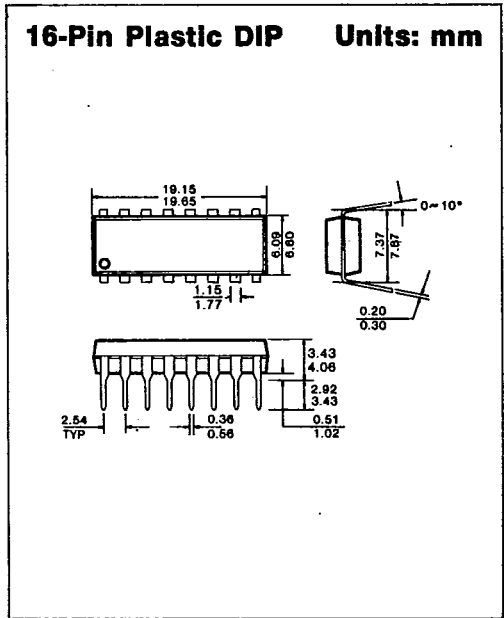
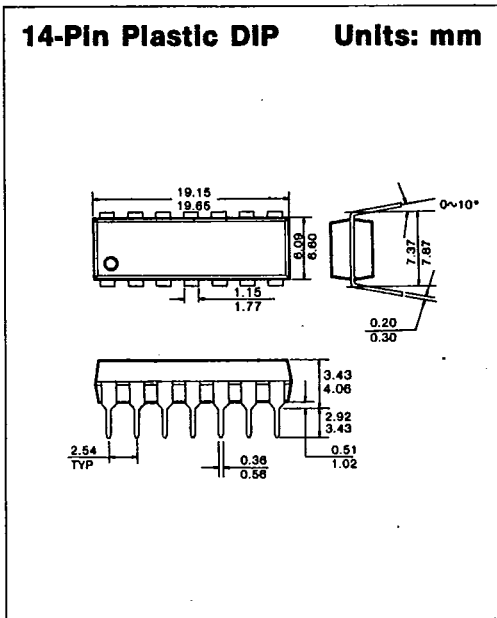
* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES

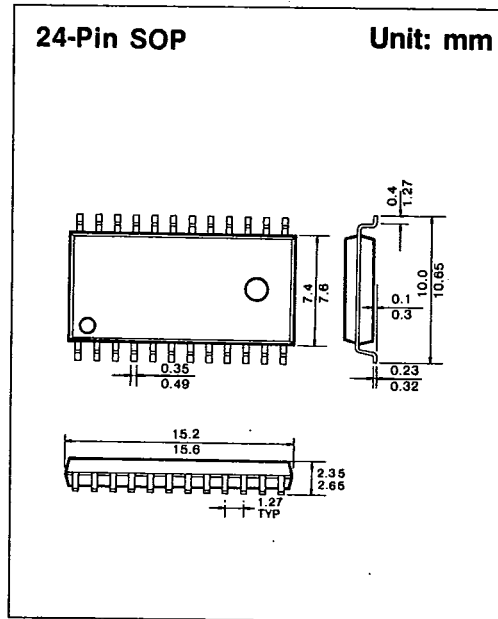
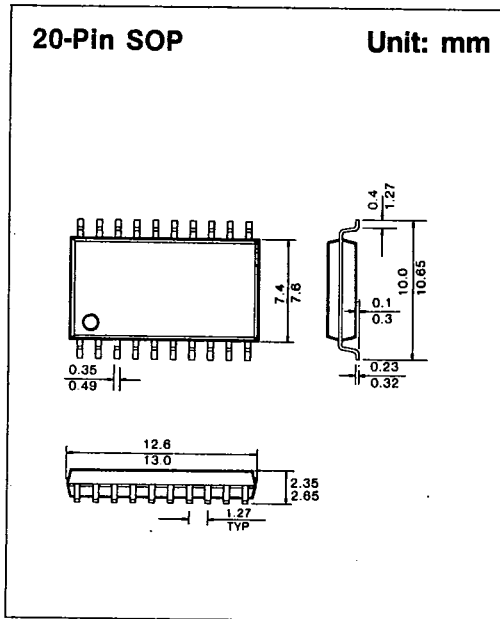
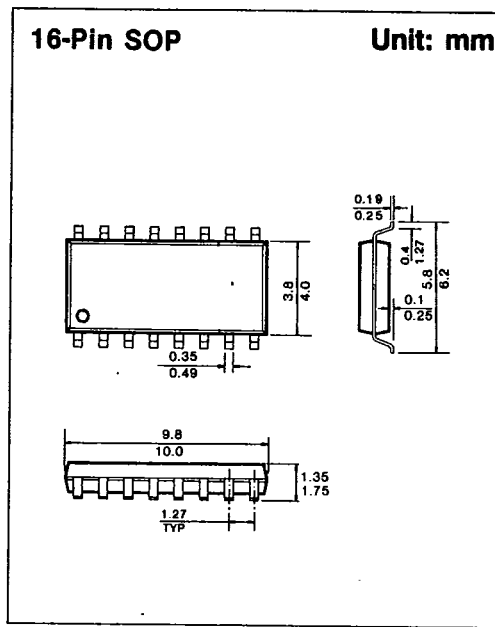
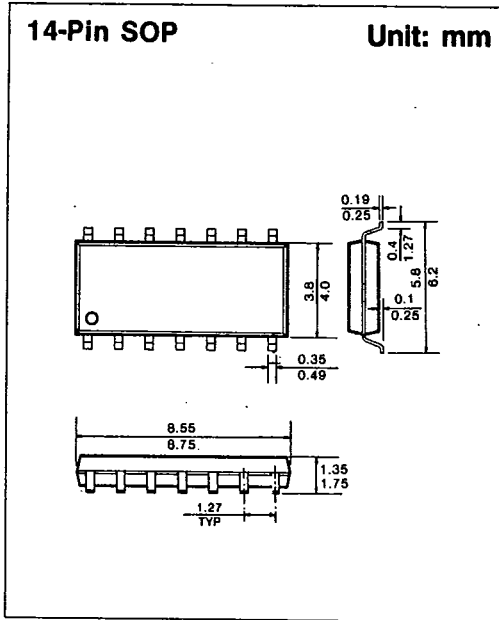


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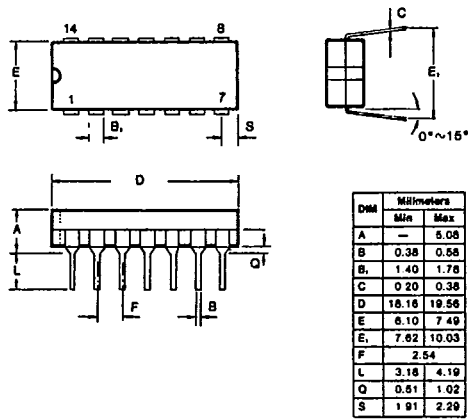


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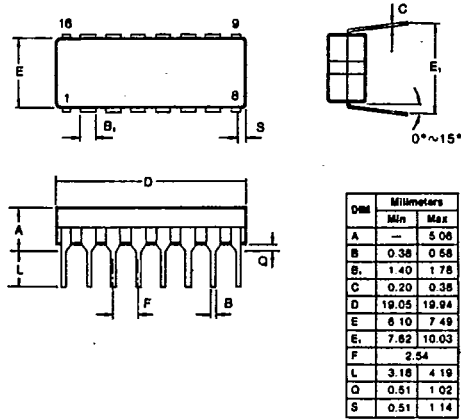
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2. CERAMIC PACKAGES

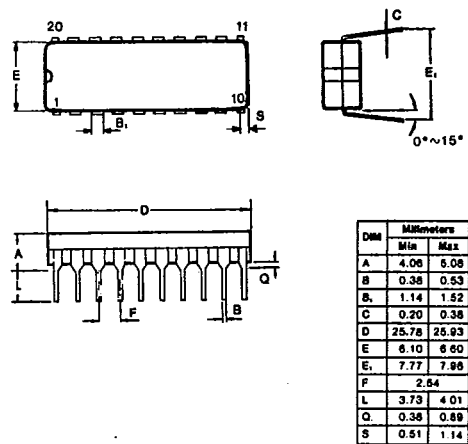
14-Pin Ceramic DIP Units: mm



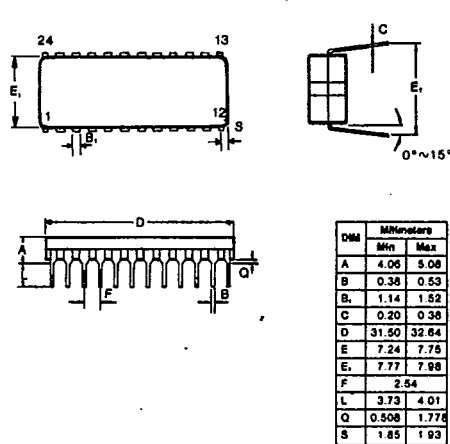
16-Pin Ceramic DIP Units: mm



20-Pin Ceramic DIP Units: mm



24-Pin Ceramic DIP Units: mm



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