

VIDEO TRACK/HOLD HYBRID
10 NSEC ACQUISITION TIME
0.1 % LINEARITY ERROR

DESCRIPTION

The TH-8530 is a video speed track/hold (T/H) amplifier packaged in a hermetic 24-pin DDIP. Its 10 nanosecond acquisition time to 0.1% of final value makes it perfect for high speed applications. With 0.1% linearity error and 100 MHz bandwidth, the TH-8530 is ideal for applications with sampling rates to 50 MHz.

For military applications, models are available with -55°C to +125°C operating temperature range screened in accordance with MIL-PRF-38534. Additional features

include a 9 nanosecond track-to-hold mode settling time, 1 millivolt per microsecond droop rate, and a slew rate of 400 volts per microsecond.

APPLICATIONS

The TH-8530's high speed, accuracy, and wide operating temperature range, and small hermetic package make it ideal for the most demanding military and commercial data acquisition requirements. Typical applications include pulse processing, radar and TV digitizing and very high speed instrumentation.

FEATURES

- 20 PSec Aperture Jitter
- 100 MHz Bandwidth
- 50 MHz Sampling Rate
- 9 NSec Settling Time
- -55°C to +125°C Operating Temperature Range
- MIL-PRF-58354 Screening Available
- ECL Compatible

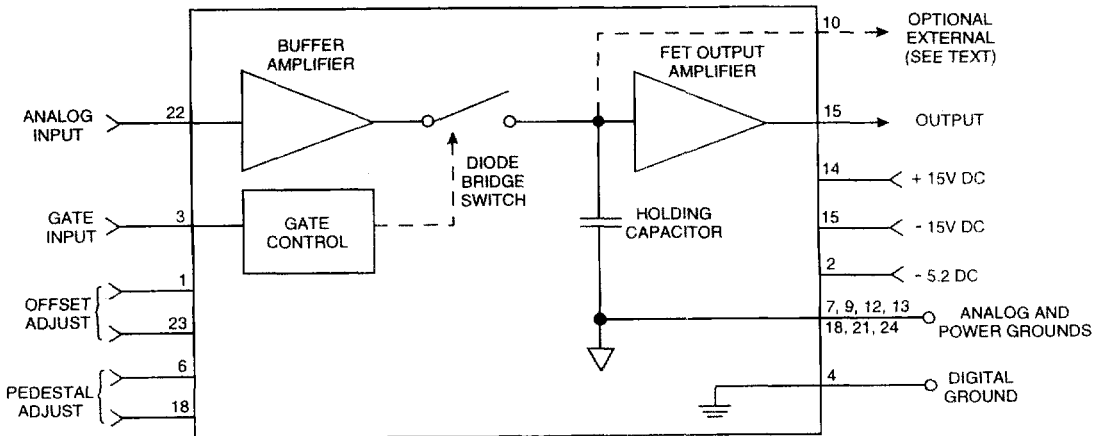


FIGURE 1. TH-8530 BLOCK DIAGRAM

TABLE 1. TH-8530 SPECIFICATIONS

| PARAMETER | UNIT | VALUE |
|--|-----------|---|
| ACCURACY | | |
| Gain | | |
| No Load | | +0.97 typ |
| With 200 Ohm Rated Load | | +0.95 typ; +0.92 min |
| Gain Temperature Coefficient | ppm/°C | 25 typ; 50 max |
| Linearity Error | | |
| 1 ma Max Load | % of F.S. | 0.012 |
| At Rated Load | % of F.S. | 0.2 max |
| Linearity Temperature Coefficient | ppm/°C | 5 typ; 15 max |
| Offset (See Note 1) (Trimable To Zero) | mV | 25 typ; 100 max |
| Offset Temperature Coefficient | mV/°C | 0.2 typ; 0.5 max |
| Pedestal (See Note 1) (Trimable To Zero) | mV | 25 typ; 100 max |
| Pedestal Temperature Coefficient | µV/°C | 60 typ; 150 max |
| DYNAMICS | | |
| Small Signal Bandwidth (f_t) | MHz | 100 typ; 80 min |
| Slew Rate | V/µsec | 400 min |
| Update Change | V | 2 max |
| Max Sampling Rate (See NOTE 2) | MHz | 50 typ; 33min |
| Min Cycle Time | ns | 20 typ; 33 max |
| Acquisition Turn-On Delay | ns | 3.5 typ; 7 max |
| Acquisition Time To 0.1 % Of Final Value | | |
| 2 V Input Change | ns | 10 typ; 15 max |
| 0.2 V Input Change | ns | 5 typ; 8 max |
| Aperture Time Delay | ns | 3.5 typ; 5 max |
| Aperture Time Uncertainty (Jitter) | ps | 20 typ; 35 max |
| Feedthrough Attenuation In Hold Mode | dB | 60 min thru 10 MHz |
| Settling Time To 0.1 % Of Final Value (See Note 3) | ns | 9 typ; 15 max |
| Droop Rate At 25°C (Case) | mV/µsec | 1 typ; 10 max |
| Droop Rate Vs. Temperature | | Doubles every 10°C |
| Glitch (From Track To Hold) | | |
| Amplitude | mV | 20 |
| Duration | ns | 15 (to less than 2 mV) |
| ANALOG INPUT | | |
| Range For Rated Accuracy | V | ±1 max |
| Absolute Max Without Damage | V | ±2.5 |
| Input Impedance | kOhms | 100 typ; 20 min |
| Capacitance | pF | 5 typ; 8 max |
| Bias Current | mA | ±0.1 typ; ±0.5 max |
| GATE INPUT | | |
| Type | | ECL compatible (external pulldown required) |
| Logic Levels | V | -0.8 = Logic 1 = Hold -1.6 = Logic 0 = Track |
| OUTPUT | | |
| Voltage Range | V | ±1 max |
| Steady State Current | mA | ±5 max |
| Transient Current | mA | ±50 max |
| Output Impedance | Ohms | 4 typ; 10 max |

TABLE 1. TH-8530 SPECIFICATIONS (CONTD)

| PARAMETER | UNIT | VALUE |
|--|-------------|--|
| POWER SUPPLIES | | |
| Supply Voltages | V | +15 -15 -5.2 |
| Voltage Tolerance | % | ±5 ±5 ±5 |
| Absolute Maximun Voltage | V | +18 -18 -7 |
| Current | mA | 55 typ 55 typ 45 typ 65 max 65 max 65 max |
| Power Dissipation | W | 1.9 average |
| TEMPERATURE RANGE (CASE) | | |
| Operating | °C | -55 to +125 |
| -1 Option | °C | 0 to +70 |
| -3 Option | °C | -65 to +150 |
| Storage | °C | -65 to +150 |
| PHYSICAL | | |
| Type | | 24-pin DDIP |
| Size | inches (mm) | 1.4 x 0.8 x 0.2 (36 x 20.5 x 5) |
| Weight | oz (gm) | .42 typ (11.9) |
| Notes: | | |
| 1. Measured during 50 ns track time with input grounded. | | |
| 2. Sampling rate for 0.1% dynamic error. | | |
| 3. Settling time into Hold mode. | | |

INTRODUCTION

The TH-8530 track amplifier, see FIGURE 1, includes a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltages are both buffered by amplifiers. The switch is controlled by an ECL logic gate signal which determines whether the holding capacitor voltage and output voltage will track the input signal (switch closed, logic 0) or will be held constant, retaining the value of the input at the moment the switch opens (switch open, logic 1).

The TH-8530 is available in several optional configurations. Provision for the use of an external holding capacitor is available on pin 10, see FIGURE 5. Because the external capacitor is connected in parallel with the internal capacitor, this option reduces the effects of droop and extends holding time. Acquisition time, however, is increased by the presence of additional capacitance created by this circuitry. This option is designated as "-10" when ordering the TH-8530, see ORDERING INFORMATION.

Unipolar voltage outputs, which provide internal offsets of the specified ±1 V input range, may be ordered. Option "P" produces 0 to +2 V and option "N" produces 0 to -2 V at the output (pin 15). A bipolar output range is available as option "B," see ORDERING INFORMATION.

TRIM ADJUSTMENTS

The offset and pedestal are trimmed at the factory to within the limits listed in TABLE 1. Further adjustments may be made using the trim adjustments as shown in FIGURE 2. Connect the output (pin 15) to an oscilloscope and ground the analog input (pin 22). Apply a 50 nsec negative ECL pulse at a 1 MHz rate to the gate input. Vary the pedestal adjustment potentiometer to

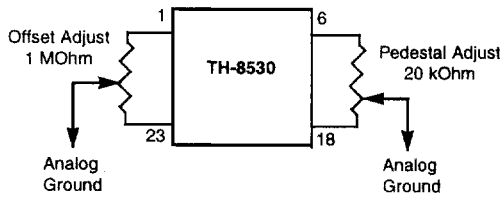


FIGURE 2. TRIM ADJUSTMENT CIRCUITS

minimize the pedestal and the offset potentiometer to trim the offset as shown in FIGURE 3.

INPUT/OUTPUT CHARACTERISTICS

As shown in FIGURE 4, the track interval is initiated when the gate input is brought LOW. The output slews as the hold capacitor is charged to a new value.

Acquisition Time is defined as the time required for the output to settle to within a given error band of its final value. Acquisition Time for any interval depends on the magnitude of the voltage change since the last interval. The minimum track time must be at least as long as the acquisition time for the largest possible input change.

The hold interval is initiated when the gate input is brought HIGH. As shown in FIGURE 4, there is a short delay, called Aperture Delay, before the series switch opens and isolates the hold capacitor from the analog input. The uncertainty in this delay, called Aperture Jitter, causes an error in the output when the input slews fast.

After the gate input goes HIGH, a transient appears on the output due to a charge transfer across the series switch. A settling time (sample to hold) interval elapses before the output reaches a given error band of its final value. The track/hold output has not achieved rated performance until after this settling time interval has elapsed.

The charge, transferred across the series switch to the hold capacitor when the gate input goes HIGH, causes a step error at

the output. This pedestal error is constant for every hold interval and does not vary with input voltage.

During the hold interval, the output voltage will increase or decrease, linearly, with time. This droop error results from charging the hold capacitor with bias current or series switch leakage current.

Feedthrough is another source of error during the hold interval. Even though the series switch is open, fast slewing input signals can cause the output to change by voltage division across the open switch capacitance. The resulting output error will be equal to the input voltage divided by the feedthrough attenuation.

GROUNDING

To minimize coupling a gate signal with an output signal, connect the input signal ground to pin 4 *only*. Do not connect any other grounds to pin 4. Analog input/output and supply voltage grounds can be connected to any of the analog ground pins. The analog grounds are connected together internally and tied to the case. To minimize impedances, it is best to connect these grounds together externally. The analog and digital grounds are separated internally to avoid crosstalk. Therefore, they must be tied together externally.

Attention must be paid to proper high frequency grounding techniques in order to maximize TH-8530 performance. It is highly desirable to use a large area ground plane under the track/hold. This will maintain a low impedance return path at all frequencies of interest. To avoid voltage differences between the ground pins, each of the ground pins on the track/hold package must be connected to ground as close to the package as possible.

POWER SUPPLY DECOUPLING

The TH-8530 provides internal ceramic decoupling capacitors on the power supply lines. In most applications, it is desirable to add external 1 µf tantalum capacitors. To avoid high frequency power supply line drops, these decoupling capacitors should be mounted as close as possible to the hybrid package .

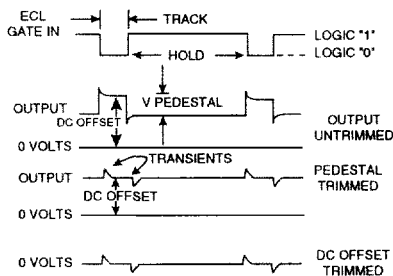


FIGURE 3. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

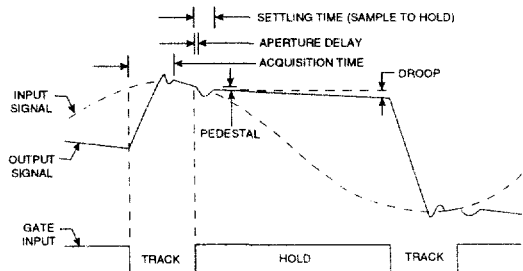
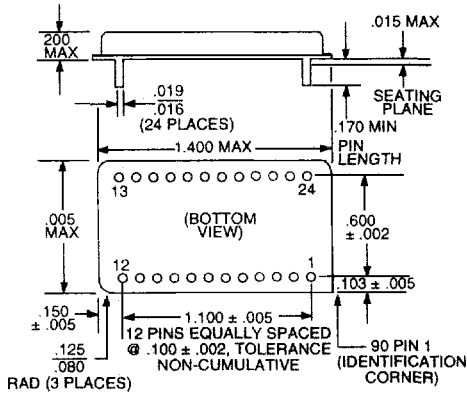


FIGURE 4. INPUT/OUTPUT CHARACTERISTICS





| PIN | FUNCTION | PIN | FUNCTION |
|-----|-----------------|-----|-----------------|
| 1 | Offset Adjust | 13 | Analog Ground |
| 2 | -5.2 VDC | 14 | +15 VDC |
| 3 | Gate Input | 15 | Output |
| 4 | Digital Ground | 16 | Analog Ground |
| 5 | NC | 17 | NC |
| 6 | Pedestal Adjust | 18 | Pedestal Adjust |
| 7 | Analog Ground | 19 | NC |
| 8 | NC | 20 | NC |
| 9 | Analog Ground | 21 | Analog Ground |
| 10 | NC (See NOTE) | 22 | Analog Input |
| 11 | -15 VDC | 23 | Offset Adjust |
| 12 | Analog Ground | 24 | Analog Ground |

Note: Pin 10 for external holding capacitor; special order only.

NOTES:

1. Dimensions shown are in inches
2. Lead identification numbers are for reference only
3. Lead spacing dimensions apply at seating plane
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C

FIGURE 5. 24-PIN DOUBLE DIP

ORDERING INFORMATION

TH-8530-1-B-10-833B

Reliability Grade:

- 883B = Fully compliant with MIL-PRF-38534.
- B = Screened to MIL-PRF-38534, but without QCI.
- Blank = Standard DDC procedures.

External Holding Capacitor:

- 10 = Pin 10 Connected to Holding Capacitor.
- Blank = No Connection.

Output Voltage Range (All with ±1 V input):

- B = -1 V to +1 V
- N = 0 to -2 V
- P = 0 to +2 V

Temperature Range:

- 1 = -55°C to +125°C
- 3 = 0°C to + 70°C