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ECL Products	

100125

Hex ECL–to–TTL Translator

FEATURES

- **Typical propagation delay: 2.2ns**
- **Typical ECL supply current ($-I_{EE}$): 65mA**
- **Typical TTL supply current (I_{TTL}): 75mA**

DESCRIPTION

The 100125 is a hex translator that converts ECL logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non–inverting, or differential receiver. An internal reference voltage generator provides V_{BB} for single–ended operation or for use in Schmitt trigger applications.

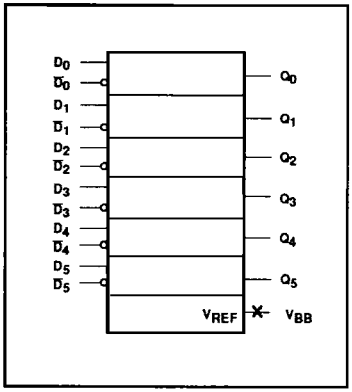
When used in the differential mode, common mode rejection makes this device tolerant of ground offsets and transients between the signal source and the translator. The 100125 outputs are designed to go to a low logic level whenever both inputs are left open or tied to V_{EE}. The V_{EE} and V_{TTL} power may be applied in any order.

All unused inputs can be left open due to integrated pull–down resistors.

PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_5$	True data Inputs (100K ECL compatible)
$\overline{D}_0 - \overline{D}_5$	Complementary data inputs (100K ECL compatible)
V_{BB}	Reference voltage output (100K ECL compatible)
$Q_0 - Q_5$	Data outputs (TTL compatible)

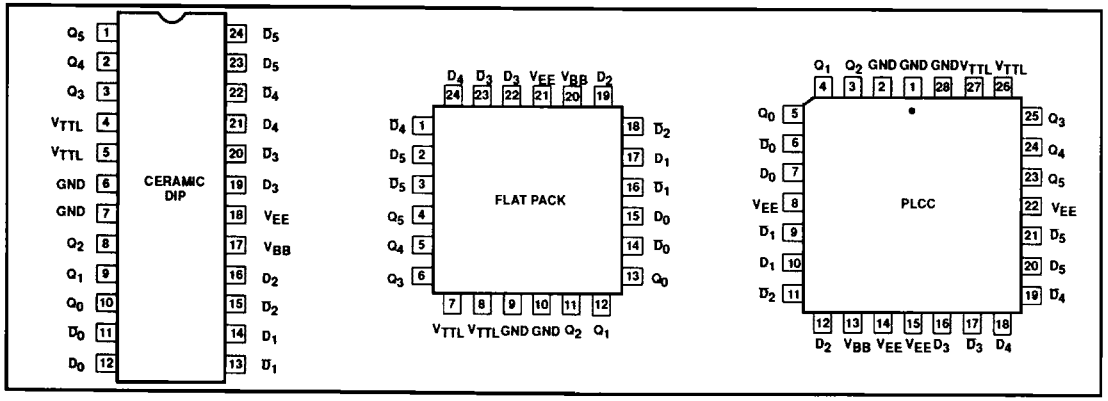
IEC/IEEE



ORDERING INFORMATION

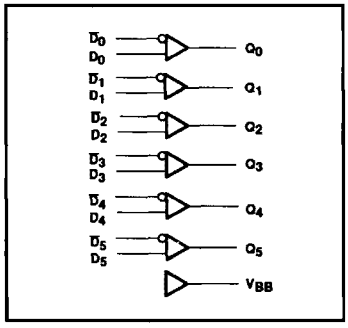
DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100125F
24–Pin Ceramic Flat Pack	100125Y
28–Pin PLCC	100125A

PIN CONFIGURATIONS



Translator | 100125

LOGIC DIAGRAM

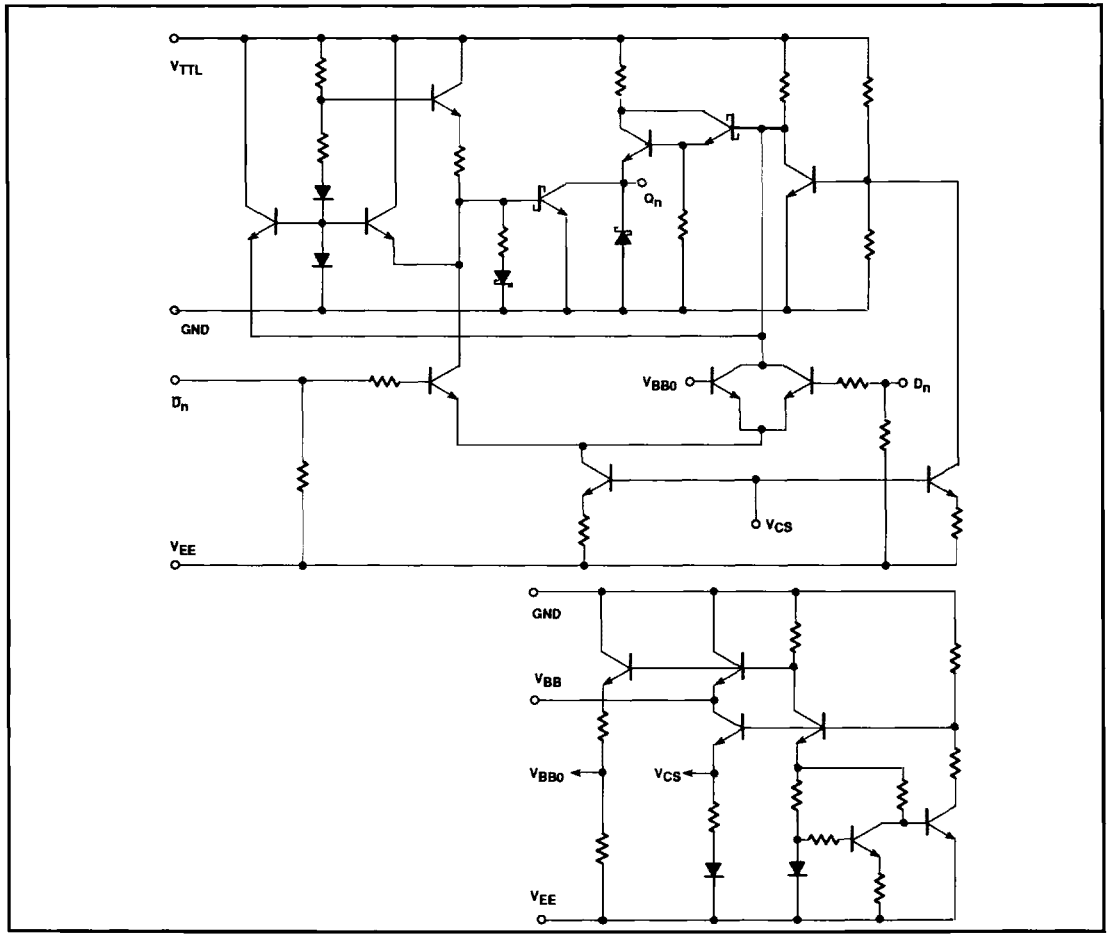


FUNCTION TABLE

INPUTS		OUTPUTS
D_n	$\overline{D}_n$	Q_0
L	H	L
H	L	H
L	L	U
H	H	U
open	open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	L	H
V_{BB}	H	H
V_{BB}	L	L

NOTES:
H = High voltage level
L = Low voltage level
U = Undefined level

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

GND = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	ECL Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
V_{TTL}	Output source current (continuous)	–0.5V to +7.0	V
V_{OUT}	Voltage applied to output in high state	–0.5V to V_{TTL}	V
I_O	Output source (continuous)	–40	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
GND	Circuit ground		0	0	0	V
V_{TTL}	TTL supply voltage		+4.5	+5.0	+5.5	V
V_{EE}	ECL supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	ECL supply voltage when operating with the 10K or the 10KH ECL family.		–5.7			V
V_{IH}[2]	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}[2]	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
V_{CM}[3]	Common mode voltage	V_{EE} = –4.2V	0		1.0	V
		V_{EE} = –4.5V				
		V_{EE} = –4.8V				
V_{DIFF}[4]	Differential input voltage	V_{EE} = –4.2V	150			V
		V_{EE} = –4.5V				
		V_{EE} = –4.8V				
$-I_{OH}$	High level output current				2.0	mA
I_{OL}	Low level output current				20	mA
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTES:
1. When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.
2. For input voltages outside the specified V_{IH} and V_{IL} ranges, the output voltage specifications will hold true. However, the AC performance will be according to specification only if two conditions are met: First, D_n or $\overline{D}_n$ must be above –2300mV at all times. Second, both D_n and $\overline{D}_n$ must be below –230mV.
3. V_{CM} is added or subtracted with respect to V_{BB}. For common–mode applications, the total voltage applied to D_n or $\overline{D}_n$ should be no less than V_{BB}–V_{CM}(max) and no greater than V_{BB} + V_{CM}(max).
4. V_{DIFF}(min) is the minimum voltage difference by which D_n must exceed $\overline{D}_n$ such that the output Q_n will assume a defined logic level(Low or High).

DC ELECTRICAL CHARACTERISTICS

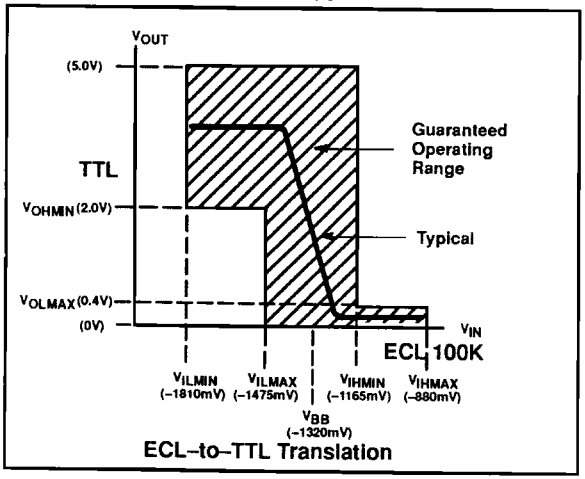
GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3]

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	All D_n = V_{IHMIN}, all $\overline{D}_n$ connected to V_{BB} pin. I_{OH} = –2.0 mA	2.5	3.4		V
V_{OL}	Low level output voltage	All D_n = V_{ILMAX}, all $\overline{D}_n$ connected to V_{BB} pin. I_{OL} = +20 mA		0.35	0.5	V
V_{OS1}	Indeterminate input protection test	All D_n = all $\overline{D}_n$ = V_{EE}. I_{OL} = +20 mA			0.5	V
V_{OS2}	Indeterminate input protection test	All D_n and all $\overline{D}_n$ open. I_{OL} = +20 mA			0.5	V
V_{BB}	Reference output voltage	V_{EE} = –4.5V; All D_n open, all $\overline{D}_n$ connected to V_{BB} pin.	–1380	–1320	–1260	mV
		V_{EE} = –4.8V to –4.2V; All D_n open, all $\overline{D}_n$ connected to V_{BB} pin.	–1396	–1320	–1244	mV
I_{IH}	High level input current	One D_n input under test at V_{IHMAX}, all other D_n inputs at V_{ILMIN}. All $\overline{D}_n$ inputs connected to V_{BB} pin.			350	µA
I_{IL}	Low level Input current	One $\overline{D}_n$ input under test at V_{ILMIN}, all other D_n inputs at V_{IHMAX}. All $\overline{D}_n$ inputs connected to V_{BB} pin.	0.5			µA
$-I_{EE}$	V_{EE} supply current	All D_n at V_{IHMAX}. All $\overline{D}_n$ at V_{BB}.	40	65	85	mA
$-I_{OS}$	Short circuit current[4]	All D_n connected to V_{BB} pin. All $\overline{D}_n$ inputs at V_{ILMIN}. One Q_n under test at ground, V_{TTL} = 5.5V.	–40		100	mA
I_{TTLH}	V_{TTL} supply current outputs High	All D_n connected to V_{BB} pin. All $\overline{D}_n$ inputs at V_{ILMIN}. V_{TTL} = 5.5V.		70	100	mA
I_{TTLL}	V_{TTL} supply current outputs Low	All D_n connected to V_{BB} pin. All $\overline{D}_n$ inputs at V_{IHMAX}. V_{TTL} = 5.5V.		80	115	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. Not more than one output should be shorted at a time. The other outputs should not be loaded. For testing I_{OS}, the use of a high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

TRANSFER CHARACTERISTICS



ECL–to–TTL Translation

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.80 0.80	3.50 3.50	0.90 0.90	3.70 3.70	1.00 1.00	4.00 4.00	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.50 0.50	2.60 2.60	0.50 0.50	2.60 2.60	0.50 0.50	2.60 2.60	ns ns

NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.72 0.72	3.85 3.85	0.81 0.81	4.07 4.07	0.90 0.90	4.40 4.40	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.45 0.45	2.86 2.86	0.45 0.45	2.86 2.86	0.45 0.45	2.86 2.86	ns ns

NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.80 0.80	3.30 3.30	0.90 0.90	3.50 3.50	1.00 1.00	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.50 0.50	2.50 2.50	0.50 0.50	2.50 2.50	0.50 0.50	2.50 2.50	ns ns

NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

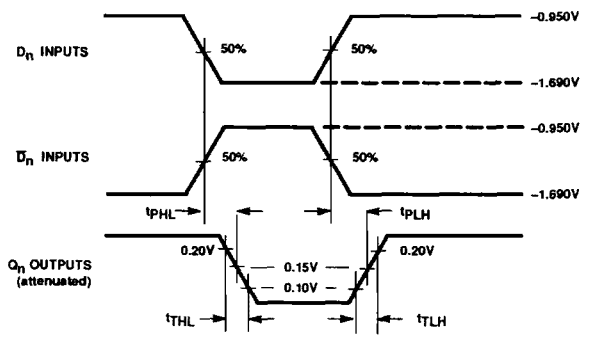
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC GND = ground, V_{TTL} = 4.5V to 5.5V, V_{EE} = –5.2V ± 5%

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n or $\overline{D}_n$ to Q_n	Waveform 1	0.72 0.72	3.63 3.63	0.81 0.81	3.85 3.85	0.90 0.90	4.18 4.18	ns ns
t_{TLH} t_{THL}	Transition time Q_n 1.0V to 2.0V, 2.0V to 1.0V		0.45 0.45	2.75 2.75	0.45 0.45	2.75 2.75	0.45 0.45	2.75 2.75	ns ns

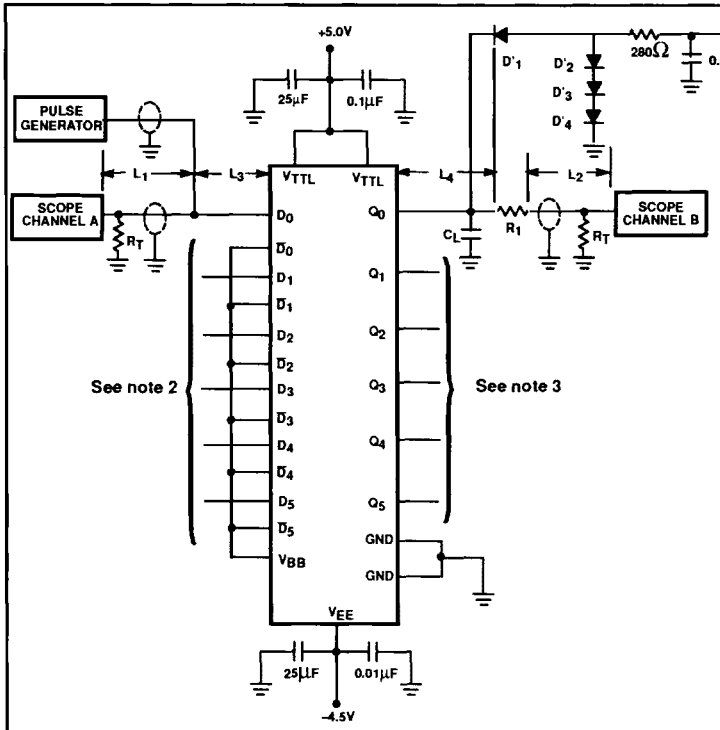
NOTES:
1. For AC test setup information, see AC Testing, Chapter 2, Section 3.
2. This AC data is for a Schottky load. When testing the 100125 with a FAST load, propagation delays may increase as much as 1.5ns.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times

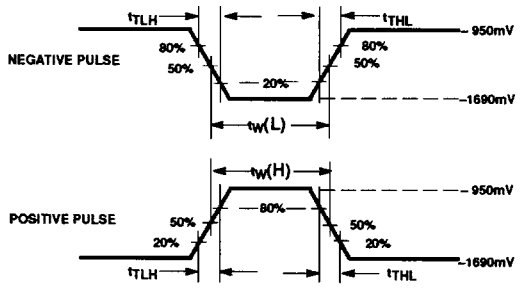
AC TEST CIRCUIT



NOTES:

1. The 0.01μF and 0.1μF decoupling capacitors should be NPO Ceramic or MLC type. All decoupling capacitors should be placed as close as physically possible to the Device Under Test (DUT), and lead lengths should be kept to less than 1/4 inch (6mm).
2. Those inputs not connected to the pulse generator should be connected to either a High or a Low state, consistent with the logic function required.
3. All unused outputs are loaded the same way as the output under test, substituting a 50Ω termination for the scope. The tolerance of all resistors should be ± 1% or better.
4. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the lead length from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and D_1, should not exceed 1/4 inch.
5. R_T = 50Ω termination internal to scope. R_1 = 450Ω.
6. Fixture and stray capacitance (not including scope cable capacitance) = C_L = 25pF.
7. Any unterminated stubs or unmatched connections anywhere along the transmission line between the pulse generator and the DUT or between the DUT and the scope should not exceed 1/4 inch (6mm) in length. (Refer to section on AC test procedure).

ECL INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
GND = 0V (system ground),
V_{EE} = –4.8V to –4.2V, V_{TTL} = +4.5V to +5.5V

Family	Amplitude	Rep Rate	$t_W(H)$, $t_W(L)$	t_{TLH}, t_{THL}
100K ECL	740mV_{p-p}	1MHz	500ns	0.7 ± 0.1ns