FDD spindle motor driver

BA6482AK

The BA6482AK is an FDD spindle motor driver that employs a 3-phase, full-wave, soft switching drive system. This high-performance IC contains a digital servo, an index amplifier, and a power save circuit.

●Applications

Floppy disk drives

●Features

1) 3-phase, full-wave, soft switching drive system.
2) Digital servo circuit.
3) Power save circuit.
4) Hall power supply switch.
5) Motor speed changeable.
6) Index amplifier.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	7	V
Power dissipation	Pd	400*	mW
Operating temperature	Topr	−25～+75	℃
Storage temperature	Tstg	−55～+125	℃
Output current	$I_{OMAX.}$	1000	mA

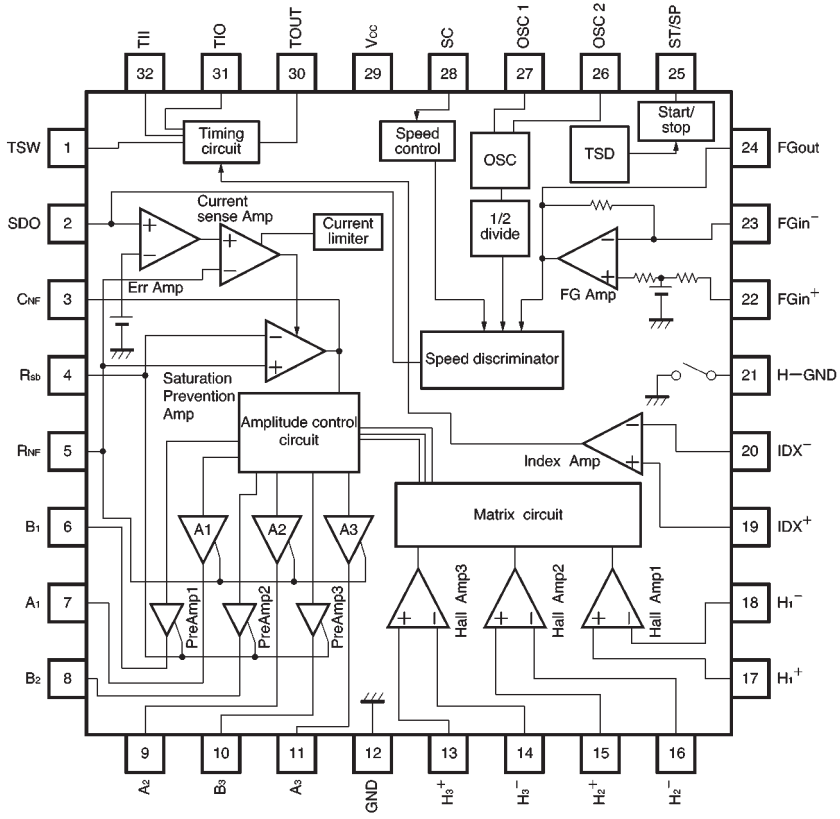
* Reduced by 4 mW for each increase in Ta of 1℃ over 25℃.

* Single unit

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	2.6	−	6.5	V

●Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	TSW	Reference timing pulse output
2	SDO	Speed discriminator output; error amplifier input
3	C_{NF}	Current sensing amplifier output (for phase compensation)
4	R_{sb}	Output base current sensing pin
5	R_{NF}	Driver power supply (current sensing pin)
6	B_1	Preamplifier output 1
7	A_1	Motor output 1
8	B_2	Preamplifier output 2
9	A_2	Motor output 2
10	B_3	Preamplifier output 3
11	A_3	Motor output 3
12	GND	GND
13	H_3^+	Hall input amplifier 3 input (+)
14	H_3^-	Hall input amplifier 3 input (−)
15	H_2^+	Hall input amplifier 2 input (+)
16	H_2^-	Hall input amplifier 2 input (−)
17	H_1^+	Hall input amplifier 1 input (+)
18	H_1^-	Hall input amplifier 1 input (−)
19	IDX^+	Index amplifier input (+)
20	IDX^-	Index amplifier input (−)
21	H-GND	Hall device bias switch (GND)
22	$FGin^+$	FG amplifier input (+)
23	$FGin^-$	FG amplifier input (−)
24	FGout	FG amplifier output
25	ST/SP	Start/stop
26	OSC2	Oscillator input
27	OSC1	Oscillator output
28	SC	Speed control
29	Vcc	Signal power supply
30	TOUT	Mono/multi timing output
31	TIO	Timing integrator output
32	TII	Timing integrator input

●Input/output circuits

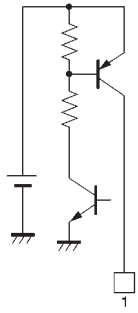


Fig.1

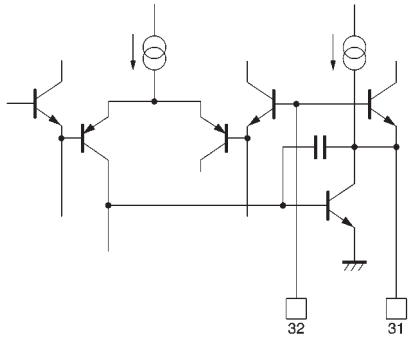


Fig.2

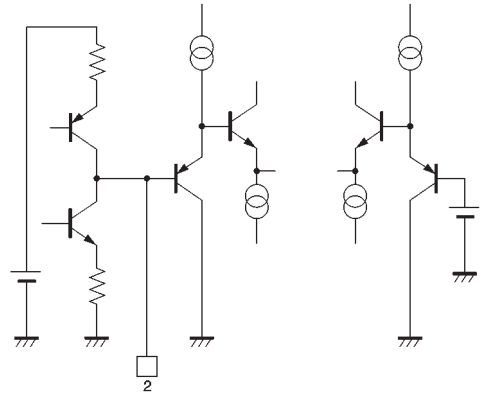


Fig.3

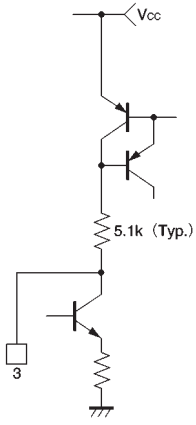


Fig.4

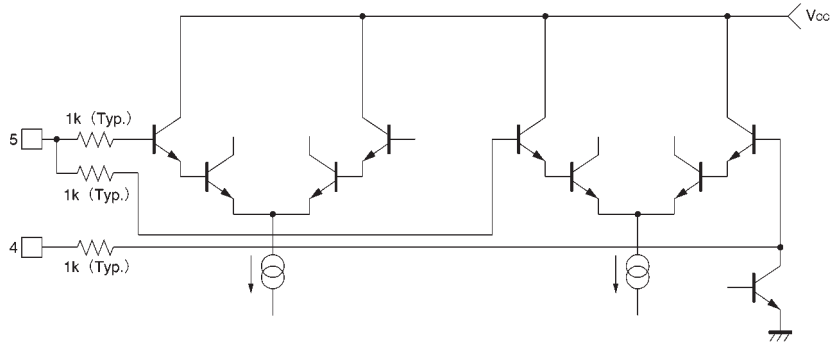


Fig.5

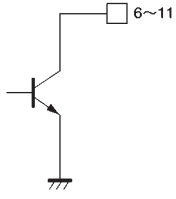


Fig.6

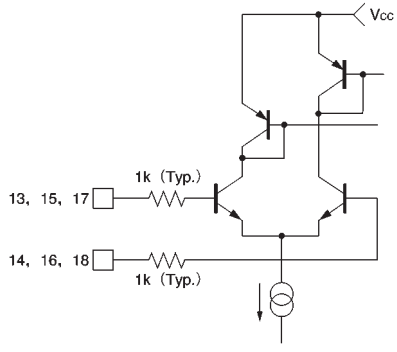


Fig.7

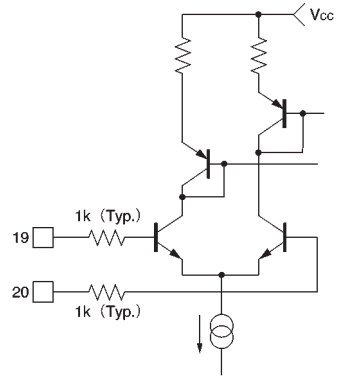


Fig.8

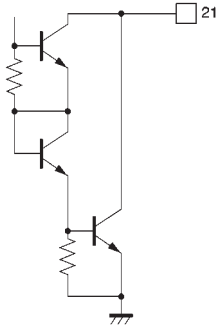


Fig.9

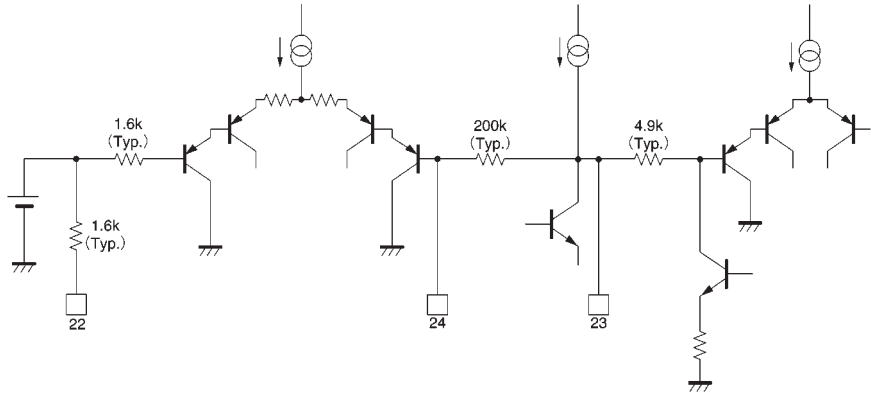


Fig.10

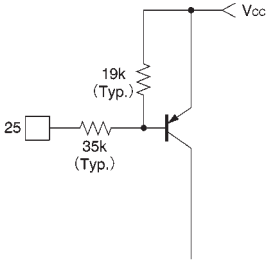


Fig.11

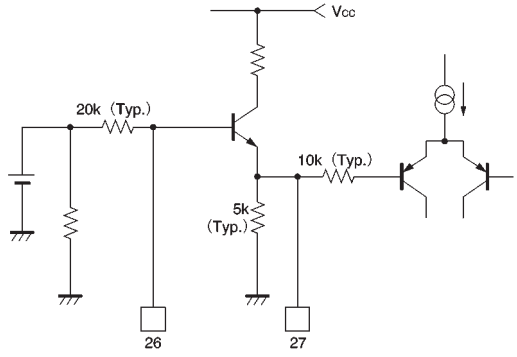


Fig.12

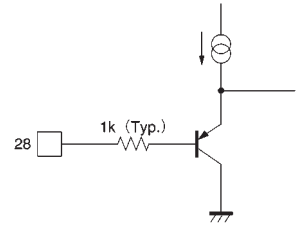


Fig.13

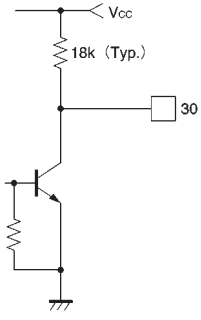


Fig.14

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply current 1	Icc1	—	18	26	mA	Operating state
Supply current 2	Icc2	—	—	3	μA	Standby state
Hall in-phase input voltage range	VHB	1.5	—	Vcc −0.5	V	
Hall amplifier input voltage sensitivity	VHin	40	—	—	V	Differential input
Output saturation voltage	Vsat	—	0.17	0.24	mV_{P-P}	Iout=350mA Low-side
Preamplifier maximum output current	Iopre	40	60	100	mA	
Current limiter voltage	Vcl	130	160	190	mV	R_{NF}=0.5Ω
Speed discriminator HIGH level output current	IDH	14	20	26	μA	
Speed discriminator LOW level output current	IDL	14	20	26	μA	
FG amplifier gain	GFG	39	42	45	dB	
Speed discriminator minimum input	VFGmi	2.0	—	—	mV_{P-P}	FG amplifier input conversion
Speed discriminator noise margin	VFGnm	—	—	0.5	mV_{P-P}	FG amplifier input conversion
Control input gain	GErr	−14	−11	−7.5	dB	R_{NF}=0.5Ω
Oscillator frequency	fOSC	—	1000	1100	kHZ	
Oscillator frequency precision*3	△fOSC	−0.2	—	0.2	%	f_{OSC}=1000kHz
Start/stop voltage, HIGH	VssH	Vcc −1.0	—	Vcc	V	Standby state
Start/stop voltage, LOW	VssL	0.0	—	Vcc −2.0	V	Operating state
Speed switching voltage, HIGH	VscH	2.0	—	Vcc	V	Synchronized at f_{FG}=360 Hz
Speed switching voltage, LOW	VscL	0.0	—	1.0	V	Synchronized at f_{FG}=300 Hz
Hall bias saturation voltage	VHGND	—	1.7	1.9	V	10 mA sink current
Timing in-phase input voltage range	VBT	1.5	—	Vcc −0.7	V	
Timing offset voltage	VosT	−5	0	5	mV	
Timing input hysteresis 1	VhyT1	10	20	30	mV	
Timing input hysteresis 2	VhyT2	−30	−20	−10	mV	
Delay timing 1	T_1	1.80	2.00	2.20	ms	300 rpm
Delay timing 2	T_2	1.50	1.67	1.83	ms	360 rpm
Delay timing ratio	T_1/T_2	1.15	1.20	1.25	—	
Timing output pull-up resistance	RT	12	18	24	kΩ	
Timing output LOW level voltage	VoLT	—	0.2	0.4	V	1.0 mA sink current

*3 This precision indicates the deviation observed within the same ceramic oscillator.

●Circuit operation

(1) Motor drive circuits

The motor driver employs a 3-phase, full-wave, soft switching current drive system, in which the rotor position is sensed by Hall devices. The motor drive current is sensed by a small resistor (R_{NF}). The total drive current is controlled and limited by sensing the voltage developed across this resistor. The motor drive circuit consists of Hall amplifiers, an amplitude control circuit, a driver, an error amplifier, a current feedback amplifier, and a saturation prevention amplifier (Fig. 15).

The waveforms of different steps along the signal path from the Hall devices to the motor driver output are shown in Fig. 16. The Hall amplifiers receive the Hall device voltage signals as differential inputs. Next, by deducting the voltage signal of Hall device 2 from the voltage signal of Hall device 1, current signal H1, which has a phase 30 degrees ahead of Hall device 1, is created. Current signals H2 and H3 are created likewise. The amplitude control circuit then amplifies the H1, H2, and H3 signals according to the current feedback amplifier signal. Then, drive current signals are produced at A1, A2, and A3 by applying a constant magnification factor. Because a soft switching system is employed, the drive current has low noise and a low total current ripple.

The total drive current is controlled by the error amplifier input voltage. The error amplifier has a voltage gain of about –11dB (a factor of 0.28). The current feedback amplifier regulates the total drive current, so that the error amplifier output voltage (V1) becomes equal to the V_{RNF} voltage, which has been voltage-converted from the total drive current through the R_{NF} pin. If V1 exceeds the current limiter voltage (Vcl), the constant voltage Vcl takes precedence, and a current limit is provided at the level of Vcl/R_{NF}.

The current feedback amplifier tends to oscillate because it receives all the feedback with a gain of 0dB. To prevent this oscillation, connect an external capacitor to the C_{NF} pin for phase compensation and for reducing the high frequency gain.

(2) Speed control circuit

The speed control circuit is a non-adjustable digital servo system that uses a frequency locked loop (FLL). The circuit consists of an 1/2 frequency divider, an FG amplifier, and a speed discriminator (Fig. 17).

An internal reference clock is generated from an external clock signal input or an oscillator (clock signal input.). The 1/2 frequency divider reduces the frequency of the OSC signal. The FG amplifier amplifies the minute voltage generated by the motor FG pattern and produces a rectangular-shaped speed signal. The FG amplifier gain (G_{FG} = 42dB, typical) is determined by the internal resistance ratio.

For noise filtering, a high-pass filter is given by C3 and a resistor of 1.6kΩ (typical), and a low-pass filter is given by C4 and a resistor of 200kΩ (typical). The cutoff frequencies of high-pass and low-pass filters (f_H and f_L, respectively) are given by:

$$f_H = \frac{1}{2\pi \times 1.6k\Omega \times C3} \quad f_L = \frac{1}{2\pi \times 200k\Omega \times C4}$$

The C3 and C4 capacitances should be set so as to satisfy the following relationship:

$f_H < f_{FG} < f_L$

where f_{FG} is the FG frequency. Note that the FG amplifier inputs have a hysteresis.

The speed discriminator divides the reference clock and compares it with the reference frequency, and then outputs an error pulse according to the frequency difference. The motor rotational speed N is given by:

$$N = 60 \cdot \frac{f_{osc}}{n} \cdot \frac{1}{z} \quad (1)$$

fosc is the reference clock frequency,
n is (speed discriminator count) × 2,
z is the FG tooth number.

The discriminator count depends on the speed control pin voltage.

Speed control pin	Count
H	1388
L	1666

The integrator flattens out the error pulse of the speed discriminator and creates a control signal for the motor drive circuit (Fig. 18).

(3) Index amplifier

The index amplifier receives the Hall device signals as differential inputs and amplifies the signals. The hall inputs have a hysteresis. The delay time can be set arbitrarily in the delay circuit with the external constants.

(4) Other circuits

• Start/stop circuit

The start/stop circuit puts the IC to the operational state when the control pin is LOW, and to the standby state (circuit current is nearly zero) when the control pin is HIGH. The Hall device bias switch, which is linked to the start/stop circuit, is turned off during the standby state, so that the Hall device current is shut down.

• Thermal shutdown circuit

This circuit shuts down the IC currents when the chip junction temperature is increased to about 170°C (typical). The thermal shutdown circuit is deactivated when the temperature drops to about 140°C (typical).

●Circuit operation

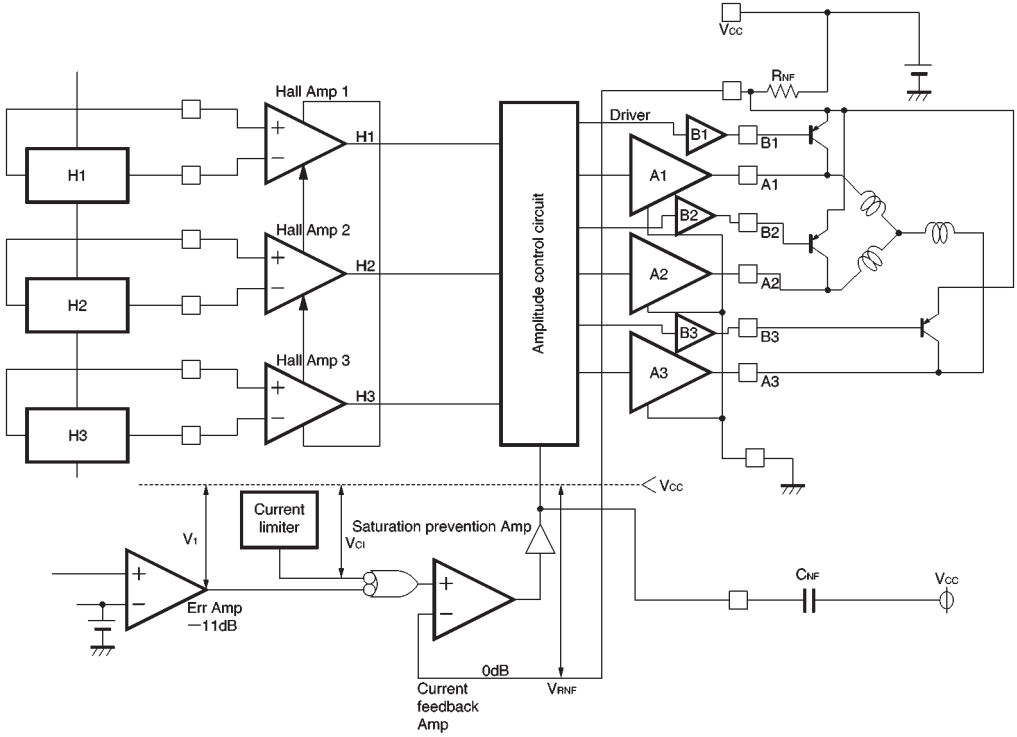


Fig.15 Motor drive circuit

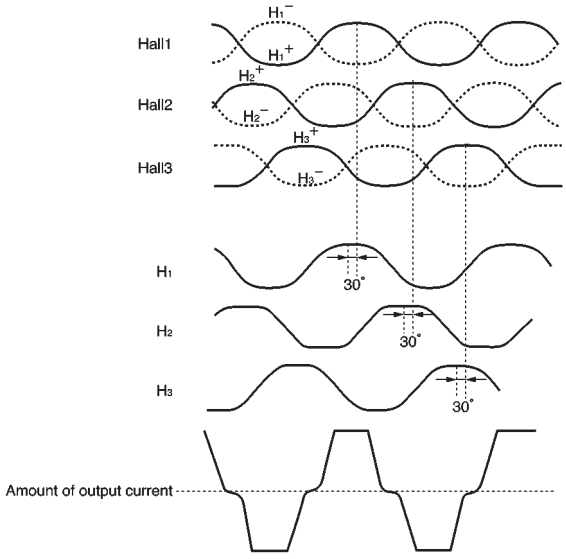


Fig.16 I / O waveforms

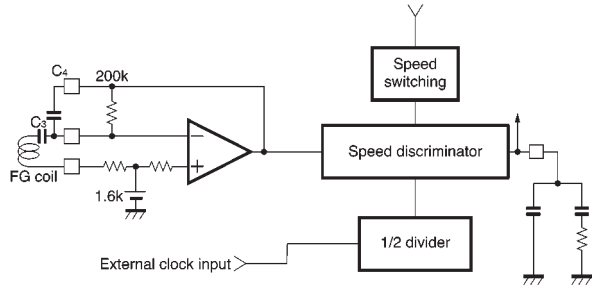


Fig.17 Speed control circuit

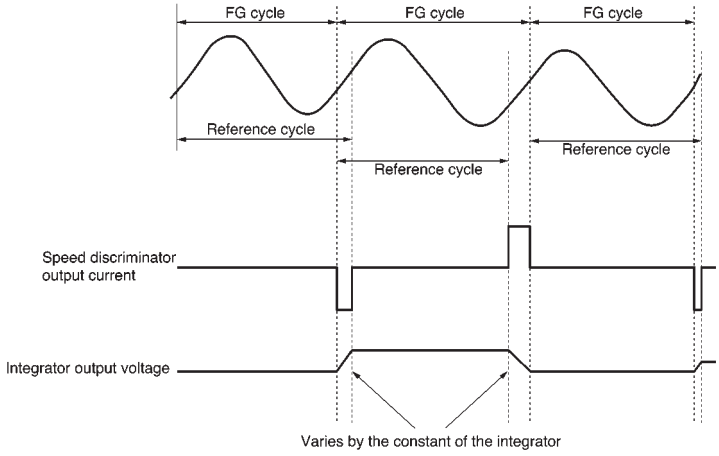


Fig.18 Control signal waveforms

●Application example

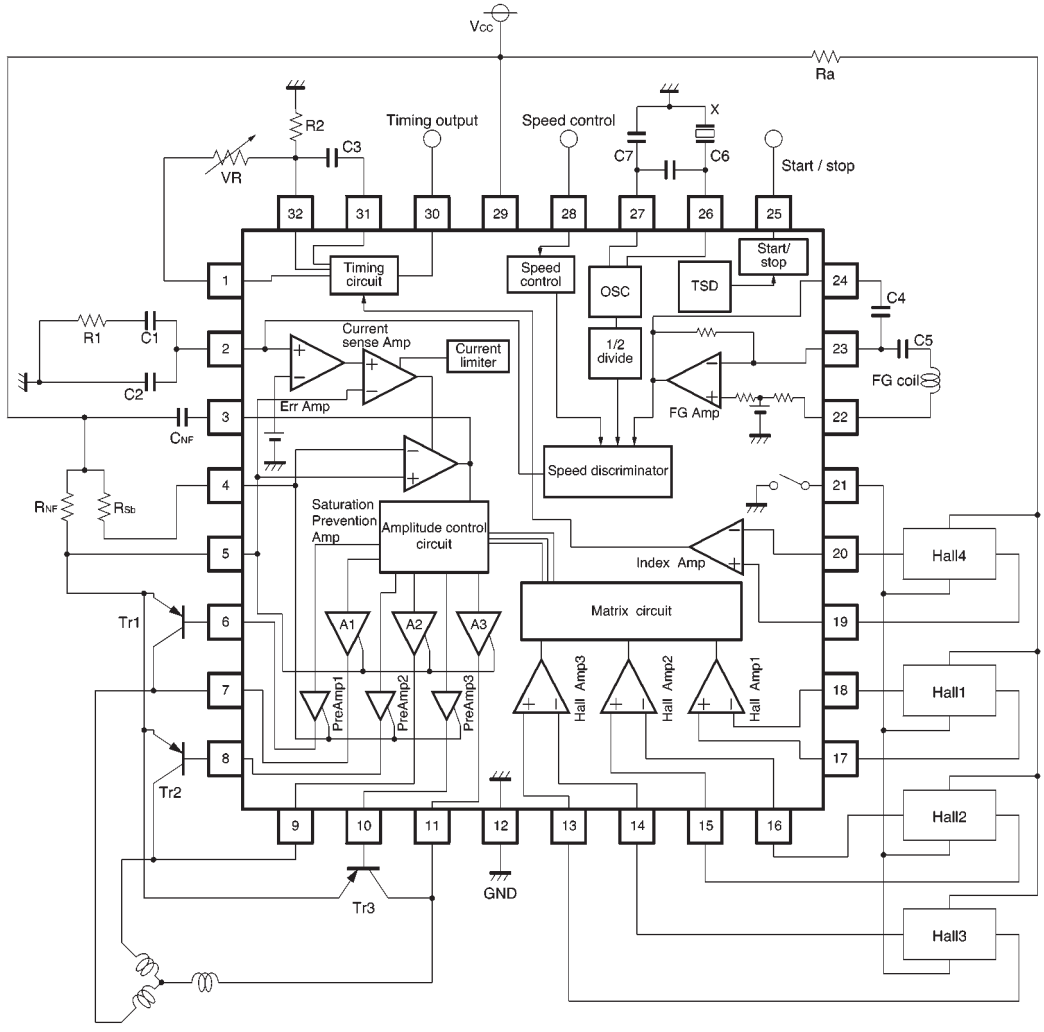


Fig.19

●Operation notes

(1) Thermal shutdown circuit

This circuit shuts down all the IC currents when the chip junction temperature is increased to about 170°C (typical). The circuit is deactivated when the temperature drops to about 140°C (typical).

(2) Hall devices connection

Hall devices can be connected in either series or parallel. When connecting in series, care must be taken not to allow the Hall output to exceed the Hall common-mode input range.

(3) Hall input level

Switching noise may occur if the Hall input voltage (pins 13～18) is too high. Differential inputs of about 100mV (peak to peak) are recommended.

(4) Ceramic oscillator external constants

The appropriate external constants vary with ceramic oscillator types. Consult with the ceramic oscillator manufacturer when determining the constants.

(5) Oscillator external input

An external clock can be directly input to the IC from OSC2 (pin 26) without a coupling capacitor. Leave OSC1 (pin 27) open in this case. The OSC2 voltage should be more than the V_{CC} voltage and less than the ground voltage.

(6) Relationship between the Hall input signal and the motor output signal

The 3-phase Hall input signal is amplified by the amplifier, and further amplified and combined in the matrix circuit. The signal is then converted to current in the amplitude control circuit and sent to the output driver to provide the motor drive current. The phase of the motor output signal is 30 degrees (typical) ahead of the phase of the Hall input signal.

(7) Although the quality of this IC is rigorously controlled, the IC may be destroyed when the supply voltage or the operating temperature exceeds its absolute maximum rating. Because short mode or open mode cannot be specified when the IC is destroyed, be sure to take physical safety measures, such as fusing, if any of the absolute maximum ratings might be exceeded.

●Electrical characteristic curves

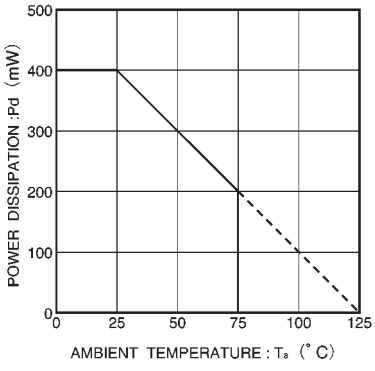


Fig.20 Power dissipation curve

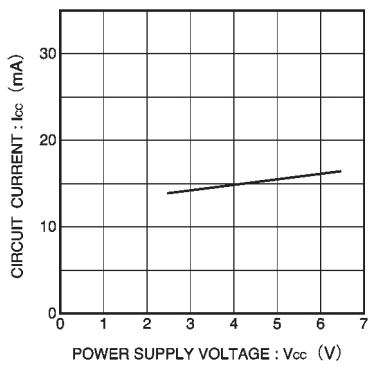


Fig.21 Circuit current vs. power supply voltage

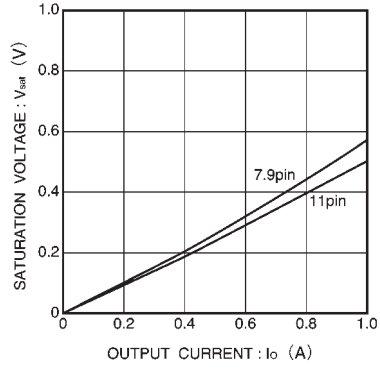


Fig.22 Output saturation voltage vs. output current

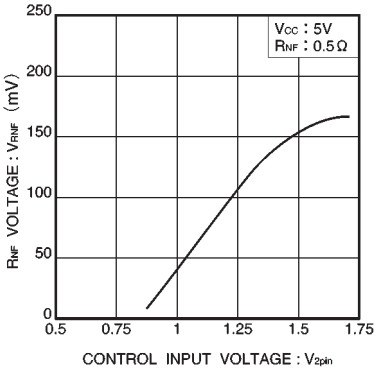


Fig.23 R_{NF} voltage vs. control input voltage

●External dimensions (Units: mm)