BU8325S
BU8325K

Pulse and tone dialer

The BU8325S and BU8325K are large scale integrated circuits for telephone sets. The LSI has both a pulse dialer and tone dialer, and a 32-digit redial buffer. It also has an internal serial input interface that allows control of the LSI using an external CPU.

Features

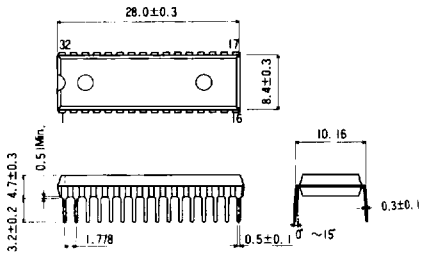
- since the chip includes both a pulse and tone dialer, it is possible to dial pulse and tone
- internal 4 × 4 encoder (4 × 4 matrix, 4-bit parallel output) together with serial interface allow external control from a CPU
- in the event of a power failure when CPU control may be lost, dial signals can still be sent from a keypad because line current is used to power the LSI
- built in 32-digit redialing memory in pulse mode. In tone mode, a digit in the memory is used to store the mode, so the maximum number of digits is 31
- power supply voltage (V_{DD}) is independent of the DTMF output level
- LSI complies with standard specifications in Japan, U.S. A., Canada, U.K., Korea, Taiwan, and Australia

Applications

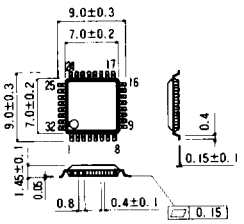
- telephone and cordless telephone sets

Dimensions (Units : mm)

BU8325S (SDIP32)



BU8325K (QFP32)



Absolute maximum ratings (T_a = 25°C)

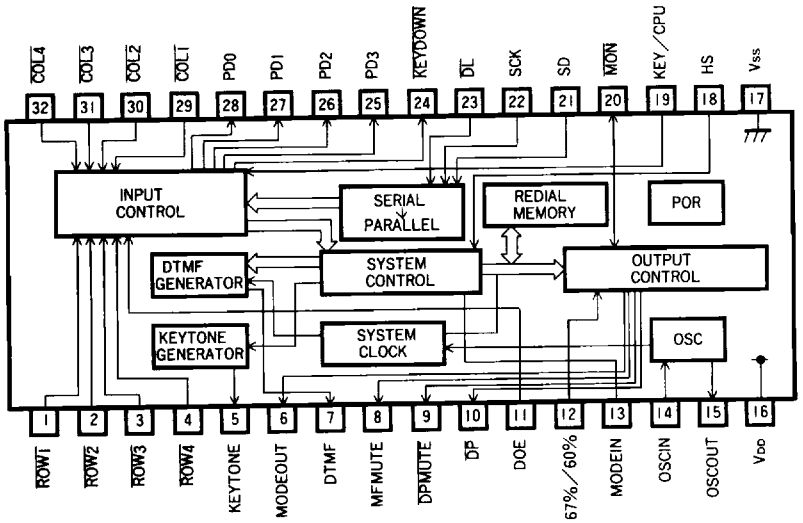
Parameter		Symbol	Limits	Unit	Conditions
Power supply voltage		V_{DD}	7.0	V	
Input voltage		V_{IN}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V	Applies to $\overline{ROW1} \sim \overline{ROW4}$, $\overline{COL1} \sim \overline{COL4}$, HS, MODEIN, OSCIN, 67%/60%, DOE, KEY/CPU, SD, SCK, and $\overline{DL}$ pins
Output voltage	1	Vout1	$V_{SS}-0.3 \sim V_{DD}+0.3$	V	Applies to OSCOUT, KEYTONE, and DTMF pins
	2	Vout2	$V_{SS}-0.3 \sim 7.0$	V	Applies to MODEOUT, $\overline{MFMUTE}$, $\overline{DPMUTE}$, $\overline{DP}$, $\overline{MON}$, $\overline{KEYDOWN}$, and PDO ~ PD3 pins
Power dissipation	BU8325S	P_d	900	mW	Reduce power by 9 mW/°C for each degree above 25°C.
	BU8325K		400		Reduce power by 4 mW/°C for each degree above 25°C.
Operating temperature		T_{opr}	−10 ~ +60	°C	
Storage temperature		T_{stg}	−55 ~ +125	°C	

Recommended operating conditions (T_a = 25°C)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Power supply voltage	V_{DD}	2.0	3.0	5.5	V	
Oscillation frequency	f_{OSC}		3.579545		MHz	Recommended parts (Mfg. part numbers listed below are 3-pin surface-mount devices with internal capacitors): Murata CSTC3.58MGU300GA Fujitsu FAR-C4CA-03580-K02 Kyocera KBR-3.58MWS-BU5
Key input time	t_{KD}	40			ms	Minimum time to process a key input (down) operation is 40 ms.
Key release time	t_{KU}	5			ms	Minimum time to process a key release (up) operation is 5 ms.
MODEIN pull-up resistance	R_{MIU}	0		10	kΩ	
MODEIN pull-down resistance	R_{MID}	0		10	kΩ	

Block diagram

BU8325S (SDIP32)



BU8325K (QFP32)

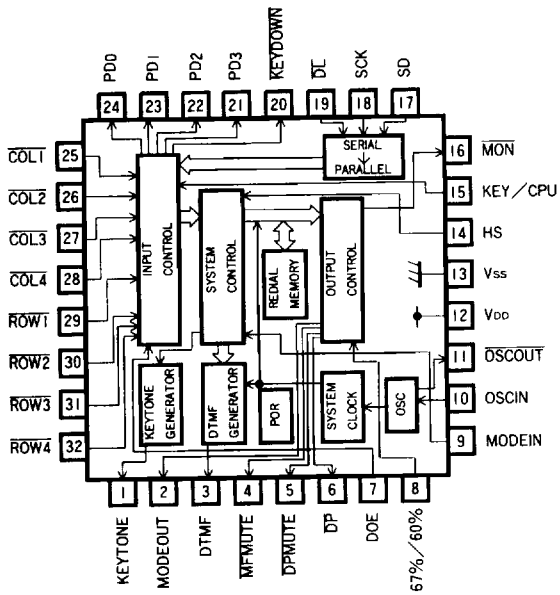


Table 1 Pin description

Pin no SDIP32	Pin no QFP32	Symbol	Description
1 ~ 4 29 ~ 32	29 ~ 32 25 ~ 28	Key input: $\overline{ROW1}$ ~ $\overline{ROW4}$ and $\overline{COL1}$ ~ $\overline{COL4}$	These pins can either be connected to a 3×4 (2 of 7) or a 4×4 keypad. A valid key entry sequence can be either: Connecting a $\overline{ROW}$ input to a $\overline{COL}$ input Taking a $\overline{ROW}$ input and a $\overline{COL}$ input LOW simultaneously In pulse mode, if more than one key is pressed at the same time, the entry is ignored. In tone mode, you can generate a single tone by pressing two or more keys in the same row or the same column. If multiple keys not in the same row or the same column are pressed, the entry is ignored.
18	14	HS (Hook switch input)	When this pin is HIGH, the IC perceives the phone as on hook; when the pin is LOW, the phone is off hook. The IC is set to the off-hook state during a dial signal transmission and to the on-hook state during memory hold. In the on-hook state, only redial buffer memory erase is enabled. The oscillator circuit does not operate during redial buffer memory erase. Current does flow in the pull-up resistors (SCK, $\overline{DL}$). There is current flow in the shift register, the only current in the on-hook state
12	8	67%/60% (Dial pulse break ratio switching)	Switches the dial pulse break. When this pin is HIGH, the IC uses the 67% ratio; when the pin is LOW, the IC uses the 60% ratio.
6	2	MODEOUT (Mode status output)	This pin is forced to the high impedance state when the output mode is set for pulse, and to LOW when the output mode is set for tone generation. This pin also goes to the high impedance state when the IC is in the on-hook state. The state of the MODEIN pin can also be output at MODEOUT by going off-hook and pressing the P_A key. (In this case, no pause is generated.) MODEOUT goes LOW if MODEIN is LOW, and HIGH if MODEIN is HIGH or is in the high impedance state (Z).
13	9	MODEIN (Mode select)	This pin has three states. LOW is used to select tone mode. Z (high impedance) is used to select the 10 pps pulse mode and HIGH is used to select the 20 pps pulse mode. When the T key is pressed, tone mode is selected regardless of the state of this pin. If the HIGH and LOW levels are applied to this pin through a resistor, the resistance should be 10 kΩ or less.
14 15	10 11	OSCIN, OSCOUT (Internal oscillator input and output)	Connect a piezoelectric or ceramic resonator between OSCIN and OSCOUT. For ceramic resonators, please refer to notes in the table "Recommended operating conditions" on page 134.

Table 1 Pin description

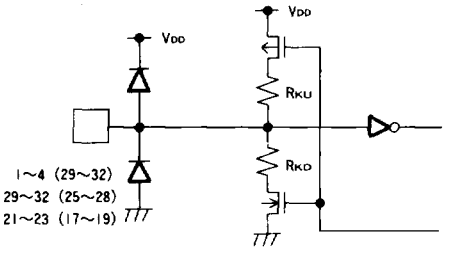
Pin no SDIP32	Pin no QFP32	Symbol	Description
5	1	KEYTONE (Key-press confirmation tone output)	This has a CMOS output. When the IC is in the off-hook state, this pin outputs a key-press confirmation tone (square wave) for all valid key presses in pulse mode and for valid P_A, R, and H key presses in tone mode. The output frequency (f_{KT}) and pulse duration (t_{KT}) are 1193 Hz and 34 ms respectively. The pin is LOW when no tone is output.
11	7	DOE PD enable	Data output on PD0 ~ PD3 is valid only when this pin is HIGH and $\overline{\text{KEYDOWN}}$ is LOW. When DOE is LOW, pins PD0 ~ PD3 are in the high impedance (Z) state.
7	3	DTMF	In tone mode, this pin outputs the DTMF signal for the key that was pressed. It is a CMOS output that is in the high impedance (Z) state when no DTMF tone is being transmitted. If the KEY/CPU pin is HIGH, holding a key down sends out a continuous DTMF signal. If the KEY/CPU pin is LOW, holding the $\overline{\text{DL}}$ pin LOW causes a continuous DTMF signal to be sent. A dc bias (a dc level between the minimum and maximum peaks of the DTMF signal) is output on the DTMF pin during the tone pre-pause time (t_{PPM}), the tone mute overlap time (t_{MOM}), and the tone inter-digital pause time (t_{IDPM}) between consecutive key inputs. This bias keeps popping sounds from being generated by the amplifier and capacitor.
8	4	$\overline{\text{MFMUTE}}$	This pin is LOW when a DTMF signal is being output or an on-hook sequence is in progress. It goes to the high impedance state (Z) during pulse mode, or if no DTMF signal is being output, or the unit is on-hook.
9	5	$\overline{\text{DPMUTE}}$	This pin is LOW when a dial pulse signal is being output or an on-hook sequence is in progress. It goes to the high impedance state (Z) in tone mode, or if no dial pulse signal is being output, or the unit is on hook.
10	6	$\overline{\text{DP}}$	In pulse mode, this pin outputs dial pulses (contact make and break sequences) corresponding to the pressed keys (Z = make; LOW = break). This is an N-channel, open drain (tri-state) output that goes to the high impedance state when not sending dial pulses.
19	15	KEY/CPU	This pin determines whether the input from the keypad or the CPU (serial data input) is used. The CPU input is used when this pin is LOW, the keypad input is used when this pin is HIGH.
21	17	SD Serial data input	When the KEY/CPU pin is LOW, serial data can be entered on this pin. This data is entered through the internal resistance of the IC. When the KEY/CPU pin is HIGH, the SD pin is pulled LOW by the IC.
22	18	SCK Serial clock input	When the KEY/CPU pin is LOW, a serial clock can be connected to this pin. Data is clocked in on the rising edge of the clock pulse. When KEY/CPU pin is HIGH, this pin is pulled LOW by the IC. When $\overline{\text{DL}}$ is LOW, serial data shifting by SCK within the IC is inhibited.

Table 1 Pin description

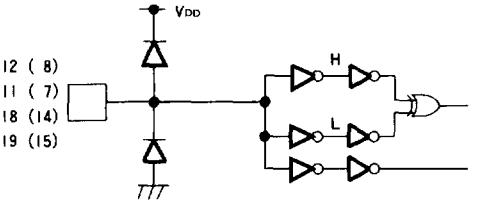
Pin no SDIP32	Pin no QFP32	Symbol	Description
23	19	$\overline{DL}$ (Data latch input)	When the KEY/CPU pin is LOW, data latch input is enabled on this pin. Serial data bits (from the SD input) that have been clocked into the IC by SCK are latched by taking this pin LOW for the duration of the latch time (t_{DLH}). This pin should be held LOW whenever data is being latched (sent to the dialer). When the KEY/CPU pin is HIGH, this pin is pulled LOW by the IC.
20	16	$\overline{MON}$	This pin is LOW while the dial signal (including pauses) is being transmitted. It is in the high impedance state (Z) if no dial signal is being sent, or if the HS pin is HIGH (on-hook). $\overline{MON}$ goes LOW at the end of the transmit start time, t_{tso} (which follows the falling edge of $\overline{DL}$). It goes HIGH at the end of the dial signal transmission, at the end of the mute overlap time 1 (t_{TMO1}), at the end of mute overlap time 2 (t_{TMO2}), and at the tone mute overlap time (t_{MOM}).
24	20	$\overline{KEYDOWN}$	When HS is LOW (off hook), this pin goes LOW when a single key is pressed, regardless of the state of the KEY/CPU pin. If HS is HIGH or no single key is being pressed, it is in the "Z" state.
28 ~ 25	24 ~ 21	PDO ~ PD3	When the HS pin is LOW (off hook), these four pins output 4-bit (converted) parallel data corresponding to the keys that are pressed, regardless of the state of the KEY/CPU pin. Even non-valid key entries are sent (for instance, if more than one key is pressed simultaneously). $\overline{KEYDOWN}$, however, remains in the Z state if multiple keys are pressed. Therefore, data should only be taken off these pins when $\overline{KEYDOWN}$ is LOW. The Z state is defined as 1, and LOW is 0. The pins go to the Z state when no data is being output, or HS is HIGH.

Figure 1 Input and output equivalent circuits

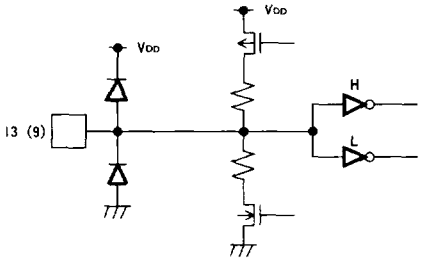
$\overline{ROW}$, $\overline{COL}$, SD, SCK, $\overline{DL}$



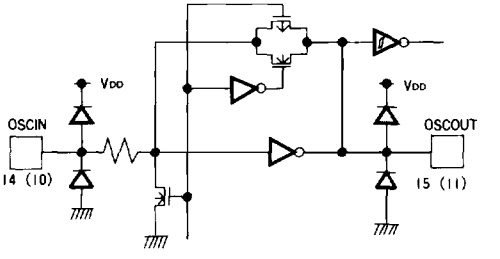
67%/60%, DOE, HS, KEY/CPU



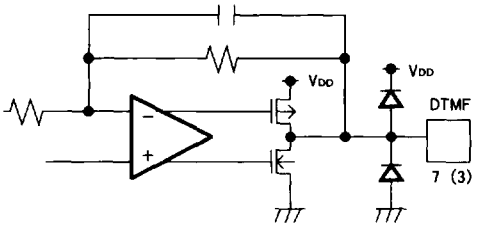
MODEIN



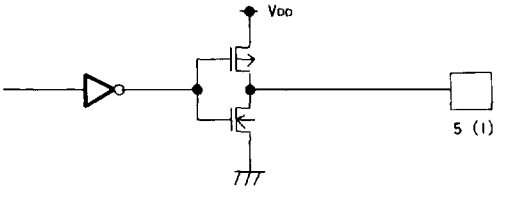
OSCIN, OSCOUT



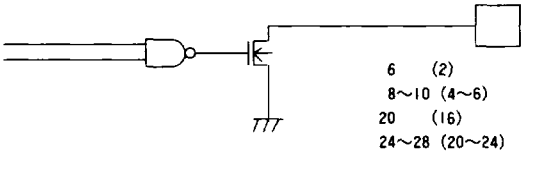
DTMF



KEYTONE



MODEOUT, $\overline{MFMUTE}$, $\overline{DPMUTE}$, $\overline{DP}$, $\overline{MON}$, $\overline{KEYDOWN}$, PD0 ~ PD3



In the diagrams, pin numbers in parentheses are for BU8325K, other pin numbers are for BU8325S

Input and output pin specifications

Table 2 Logic inputs

Pin name	HIGH	Z	LOW	Input type
HS	On hook	Should not be used	Off hook	CMOS (Schmidt trigger input)
67%/60%	Pulse break ratio = 67%	Should not be used	Pulse break ratio = 60%	CMOS
MODEIN	Pulse mode = 20 pps	Pulse mode = 10 pps	Tone mode	CMOS
DOE	PD0 ~ PD3 output data enable	Should not be used	PD0 ~ PD3 output data enable (Z level)	CMOS
KEY/CPU	Keypad input	Should not be used	CPU input	CMOS (Schmidt trigger input)

Table 3 Serial data inputs

Pin name	Pin function	Input type		
			KEY/CPU = LOW	KEY/CPU = HIGH
SD	Serial data input	CMOS	Pull-up	Pull-down
SCK	Serial clock input	CMOS (Schmidt trigger input)	Pull-up	Pull-down
$\overline{DL}$	Data latch input	CMOS	Pull-up	Pull-down

Table 4 Output pin circuit types

Output	Output type	Output	Output type
MODEOUT	NMOS open drain	$\overline{DP}$	NMOS open drain
KEYTONE	CMOS	$\overline{MON}$	NMOS open drain
DTMF	CMOS	$\overline{KEYDOWN}$	NMOS open drain
$\overline{MFMUTE}$	NMOS open drain	PDO ~ PD3	NMOS open drain
$\overline{DPMUTE}$	NMOS open drain		

$\overline{MON}$, $\overline{KEYDOWN}$, PDO ~ PD3 output signals are normally output regardless of the state of the KEY/CPU pin. The DOE pin must be HIGH to output PDO ~ PD3. When the HS pin goes HIGH (off hook) the IC enters standby mode, with all of the above outputs in the high impedance (Z) state.

DC electrical characteristics (unless otherwise noted, T_a = 25 °C, V_{DD} = 3.0 V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Supply current, pulse mode	I_{DDP}		0.45	0.60	mA	Output not loaded; pulse mode
Supply current, tone mode	I_{DDT}		0.60	1.00	mA	Output not loaded; tone mode
Memory retention current	I_{MR}		0.01	2.0	µA	
Memory retention voltage	V_{MR}	1.0			V	
Input voltage 1 HIGH	V_{I1H}	0.8 V_{DD}		V_{DD}	V	V_{DD} = 2.0 ~ 5.5 V Applies to $\overline{ROW1}$ ~ $\overline{ROW4}$, $\overline{COL1}$ ~ $\overline{COL4}$, HS, OSCIN, SD, and $\overline{DL}$ pins
Input voltage 1 LOW	V_{I1L}	V_{ss}		0.2 V_{DD}	V	
Input voltage 2 HIGH	V_{I2H}	0.9 V_{DD}		V_{DD}	V	V_{DD} = 2.0 ~ 5.5 V Applies to MODEIN, 67%/60%, DOE, KEY/CPU, and SCK pins
Input voltage 2 LOW	V_{I2L}	V_{SS}		0.1 V_{DD}	V	
Input current HIGH	I_{IH}			1.0	µA	V_{DD} = 5.5 V Applies to HS, 67%/60%, DOE, and KEY/CPU pins
Input current LOW	I_{IL}			−1.0	µA	
Input pull-up resistance	R_{IU}		300		kΩ	Applies to $\overline{ROW1}$ ~ $\overline{ROW4}$, $\overline{COL1}$ ~ $\overline{COL4}$, SD, SCK, and $\overline{DL}$ pins
Input pull-down resistance	R_{ID}		30		kΩ	
Keytone sink current	I_{KTL}	250			µA	V_{DD} = 2.0 V, V_O = 0.2 V
Keytone source current	I_{KTH}	−250			µA	V_{DD} = 2.0 V, V_O = 1.8 V
Output sink current	I_{OS}	250			µA	V_{DD} = 2.0 V, V_O = 0.2 V Applies to MODEOUT $\overline{MFMUTE}$, $\overline{DPMUTE}$, $\overline{DP}$, $\overline{MON}$, $\overline{KEYDOWN}$, and PDO ~ PD3 pins
Output leakage current	I_{OLKG}			±1.0	µA	V_{DD} = 5.5 V Applies to MODEOUT, $\overline{MFMUTE}$, $\overline{DPMUTE}$, $\overline{DP}$, $\overline{MON}$, $\overline{KEYDOWN}$, DTMF, and PDO ~ PD3 pins

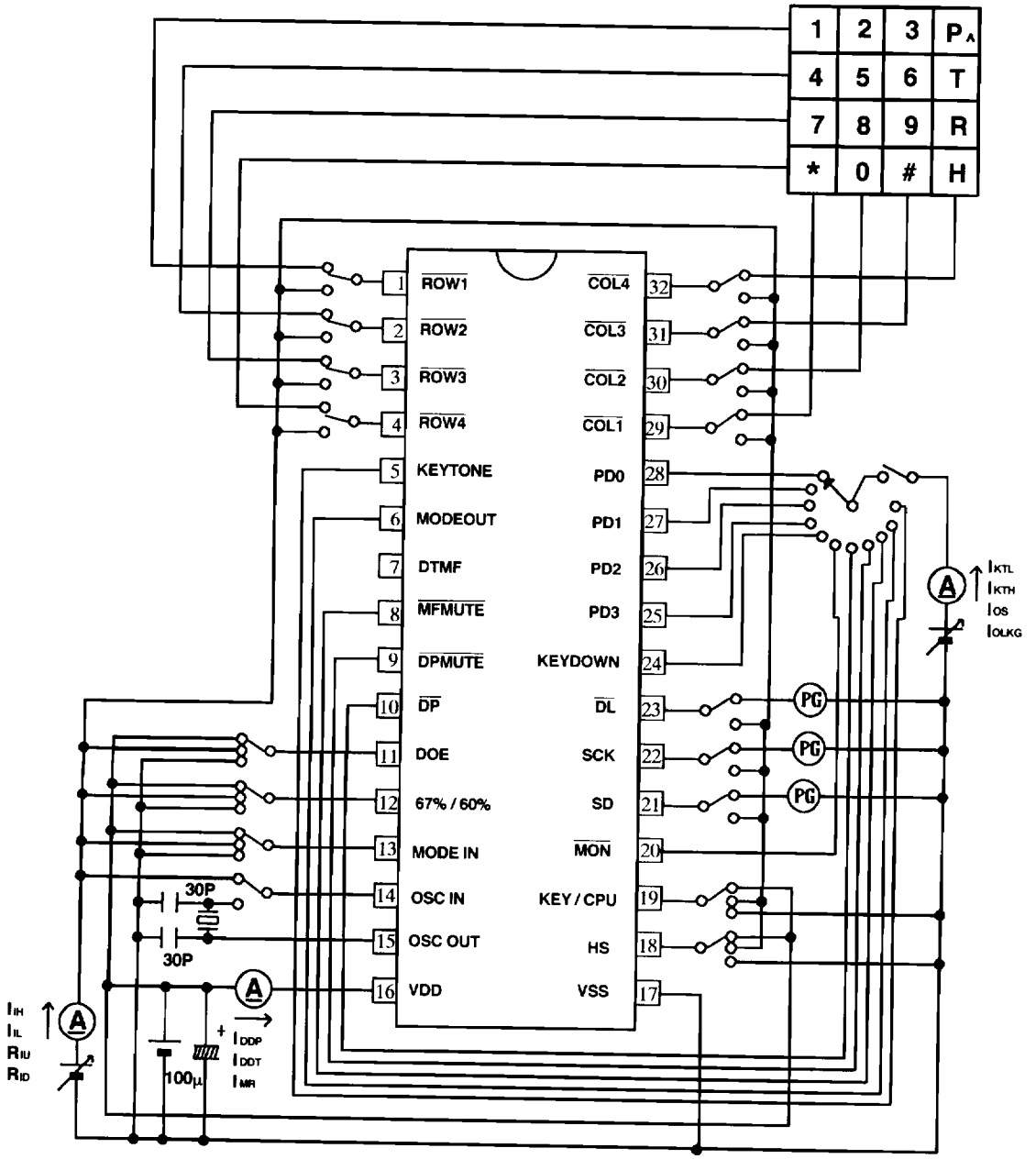
AC electrical characteristics 1 (unless otherwise noted, T_a = 25 °C, V_{DD} = 3.0 V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Oscillation start time	t_{OS}		0.1	2.0	ms	$t_{OS} = t_1 - t_2$, where t_1 is the elapsed time between the application of a LOW on the $\overline{COL1}$ pin, and the appearance of a LOW level at the $\overline{COL2}$ pin. t_2 is the elapsed time between the triggering of the internal division counter by the OSCOUT pin waveform, and the appearance of a LOW level at the $\overline{COL2}$ pin.
Key debounce time	t_{DB}		30		ms	
Output pulse rate 1	PR1		9.9		pps	MODEIN = Z (Open)
Output pulse rate 2	PR2		19.9		pps	MODEIN = HIGH
Pulse break ratio 1	BR1		66.7		%	67%/60% = HIGH
Pulse break ratio 2	BR2		60		%	67%/60% = LOW
Inter-digital pause 1 HIGH	t_{IDP1H}		838		ms	MODEIN = Z (10 pps) 67%/.60% = HIGH
Inter-digital pause 1 LOW	t_{IDP1L}		845		ms	MODEIN = Z (10 pps) 67%/.60% = LOW
Inter-digital pause 2 HIGH	t_{IDP2H}		469		ms	MODEIN = Z (20 pps) 67%/.60% = HIGH
Inter-digital pause 2 LOW	t_{IDP2L}		473		ms	MODEIN = Z (20 pps) 67%/.60% = LOW
Tone output time	t_{MF}		101		ms	Dial tone is output for as long as the key is held down, or when $\overline{DL}$ is being input. Minimum hold time for both tone output and an inter-digital pause is 101 ms. When redialing, tone output and interdigit pause are 101 ms.
Tone inter-digital pause	t_{IDPM}		101		ms	
Tone output cycle variation	$\lvert \Delta f \rvert$			0.15	%	
Tone output voltage, ROW	V_{OR}	125	150	180	mV_{pk-pk}	
Tone output voltage, COLUMN	V_{OC}	166	200	240	mV_{pk-pk}	
High band pre-emphasis	P_{EHB}	1.8	2.5	3.3	dB	
Tone output distortion	DIS		5.0	10.0	%	400 Hz ~ 30 kHz, BPF

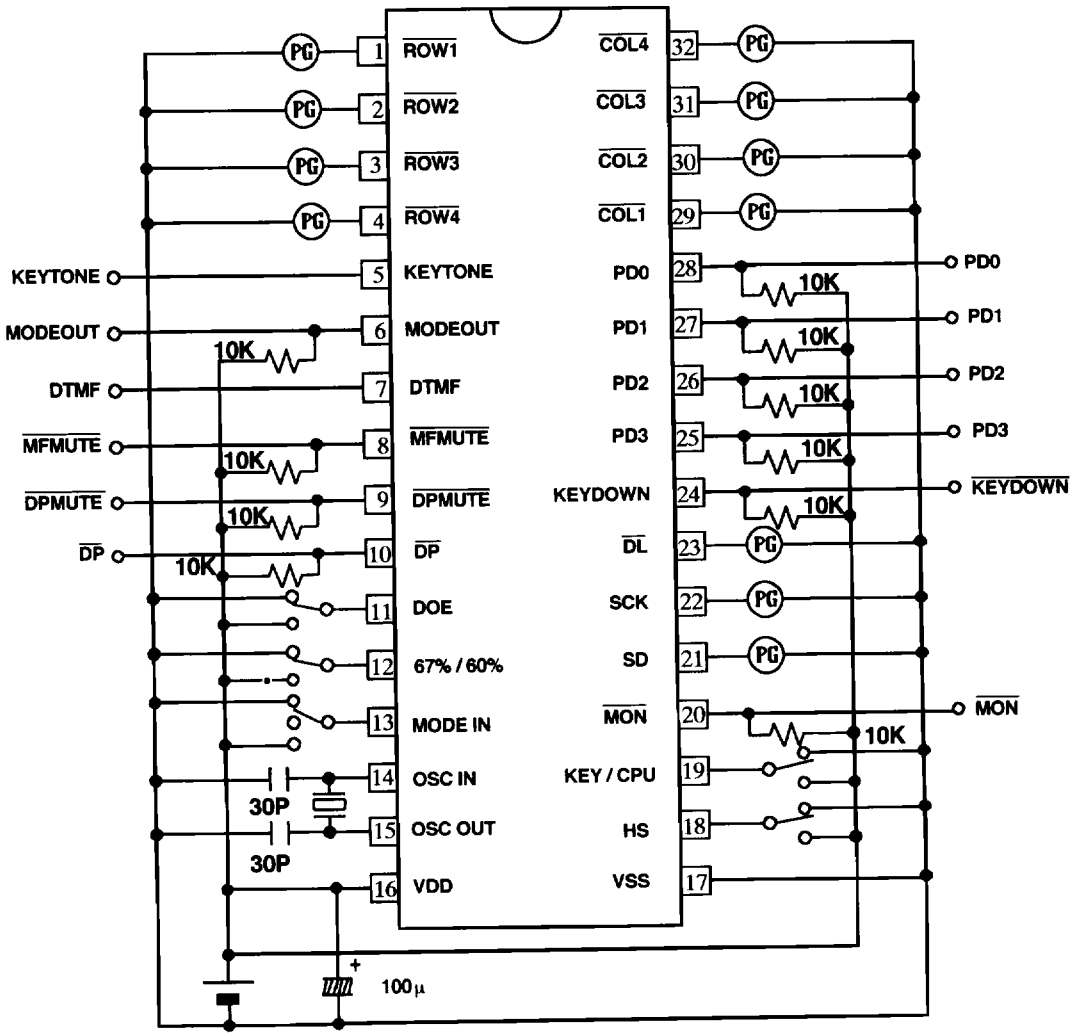
AC electrical characteristics 2 (unless otherwise noted, T_a = 25 °C, V_{DD} = 3.0 V)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Pause time	t_{PA}		3.6		s	
Hooking time	t_{HK}		708		ms	
Hooking pause time 1	t_{HKPA}		1.0		s	
On-hook time	t_{OH}	1			ms	When going on hook, the HS pin must be held HIGH for at least 1 ms.
Keytone frequency	f_{KT}		1193		Hz	
Keytone output time	t_{KT}		34		ms	
Pre-pause time, 1H	t_{PP1H}		334		ms	MODEIN = Z (10 pps) 67%/60% = HIGH
Pre-pause time, 1L	t_{PP1L}		340		ms	MODEIN = Z (10 pps) 67%/60% = LOW
Pre-pause time, 2H	t_{PP2H}		168		ms	MODEIN = HIGH (20 pps) 67%/60% = HIGH
Pre-pause time, 2L	t_{PP2L}		171		ms	MODEIN = HIGH (20 pps) 67%/60% = LOW
Tone-pre-pause time	t_{PPM}		7		ms	MODEIN = LOW (Tone)
Mute overlap time 1	t_{MO1}		810		ms	MODEIN = Z (10 pps)
Mute overlap time 2	t_{MO2}		459		ms	MODEIN = HIGH (20 pps)
Tone/mute overlap time	t_{MOM}		101		ms	
SD setup time	t_{SDS}	100			ns	KEY/CPU = LOW These values apply for a CMOS interface. Note that these values become very large when an NMOS open drain interface is used. (See "Precautions for use" following.)
SD hold time	t_{SDH}	100			ns	
Serial clock cycle period	t_{CS}	500			ns	
$\overline{DL}$ setup time	t_{DLS}	500			ns	KEY/CPU = LOW
$\overline{DL}$ hold time	t_{DLH}	15			ms	KEY/CPU = LOW When using $\overline{DL}$, to latch data into the IC, $\overline{DL}$ must be held LOW for at least 15 ms.
Transmit start time	t_{SO}	20		24	ms	Not including oscillator start time

Test circuit—DC electrical characteristics



Test circuit—AC electrical characteristics



Operation

The following section describes the operation of the integrated circuit and its inputs.

Table 5 Keypad key functions

Key	Function
0 ~ 9	Dial signals are sent when one of these keys is pressed.
✳ or #	In tone mode, when these keys are pressed, DTMF signals are transmitted. In pulse mode, the # key is not valid. The ✳ key switches the unit from pulse mode to tone mode.
P_A	When this key is pressed, a 3.6-s pause is generated. Also serves as a "break pause" key when redialing.
T	Used to switch from pulse to tone mode. Automatically inserts a 3.6-s pause. Also serves as a "break pause" key when redialing.
R	Used in redial and dial inhibit operation. Also serves as a "break pause" key when redialing.
H	Pressed to simulate an on-hook operation.

Figure 2 Keypad arrangements

	$\overline{COL1}$	$\overline{COL2}$	$\overline{COL3}$
$\overline{ROW1}$	1	2	3
$\overline{ROW2}$	4	5	6
$\overline{ROW3}$	7	8	9
$\overline{ROW4}$	✳	0	#

3 × 4 (2 of 7) keypad

	$\overline{COL1}$	$\overline{COL2}$	$\overline{COL3}$	$\overline{COL4}$
$\overline{ROW1}$	1	2	3	P_A
$\overline{ROW2}$	4	5	6	T
$\overline{ROW3}$	7	8	9	R
$\overline{ROW4}$	✳	0	#	H

4 × 4 keypad

Table 6 DTMF frequencies

Standard frequencies (Hz)		BU8325S or BU8325K (excluding drift of resonator)	
		Frequency (Hz)	Frequency variation (%)
Low	697	696.41	–0.08
	770	769.79	–0.03
	852	852.27	+0.03
	941	941.99	+0.10
High	1209	1209.31	+0.03
	1336	1335.65	–0.03
	1477	1479.15	+0.15

Table 7

Parallel data output Serial data input				Corresponding key data or function	
D3	D2	D1	D0	Off hook (HS = LOW)	On hook (HS = HIGH)
0	0	0	0	H	
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	9	
1	0	1	0	0	
1	0	1	1	*	
1	1	0	0	#	
1	1	0	1	T	
1	1	1	0	P_A	
1	1	1	1	R	Redial buffer memory erase

Key operation

In the following description, the IC behavior is described when certain key operations are carried out. In all cases, the (↑) indicates that an off-hook signal is generated. A (↓) symbol indicates that an on-hook signal is generated. Digit keys are represented by the symbol D_n, where n indicates the sequence number of the digit, not the actual digit pressed. All special keys such as the P_A key are shown as, for instance, P_A.

Normal dialing (↑) $D_1...D_n$ When the IC is in the off-hook state, the dial data from the key input is written into the redial memory and the proper dial signals (tone or pulse, depending on the operating mode) are transmitted. There is no upper limit on the number of digits that can be dialed. Key inputs can be entered during dial output. The redial buffer is cleared if the R key is pressed twice at any time after the last dial signal is transmitted, but before the IC is returned to the on-hook state.

Access pause (↑) D_1P_A, D_2 ... D_n When the P_A key is pressed with the IC in an off-hook state, a 3.6 pause is inserted into the transmission signal. Pause times can be stacked by simply re-pressing the P_A key. During a pause, dialing inputs are allowed as they are during dial signal transmission. If a pause is included in a redial, the pause can be removed during transmission by pressing the P_A, T, or R key. This operation will stop a single or a stacked pause.

Redial (↑) R Redial is only accepted if the redial key is pressed immediately after going off hook. Pressing R after going off hook causes the last number dialed to be redialed. Key inputs are not accepted when a redial signal is being output. After the redial digits have been transmitted, any number of valid key inputs are accepted and transmitted.

The redial memory holds up to 32 digits. Redial is inhibited if more than 32 digits (pulse mode) or 31 digits (tone mode) are dialed. In tone mode, one digit of dial memory is used to store the current mode. Hence only 31 digits are available for redial in tone mode.

The following keys can form part of the redial string:

- Pulse mode: digits 0 through 9, P_A and T
- Tone mode: digits 0 through 9, P_A, ✳, and #

The redial buffer is cleared if the R key is pressed twice at any time after the last dial signal is transmitted, but before the IC is returned to the on-hook state.

Mode switching (Mixed mode dialing) (↑) D_1... D_iT or ✳, D_{i+1}...Dn (MODEIN = HIGH or Z). The IC can only be switched once from pulse mode to tone mode when in an off hook state. Setting the MODEIN pin to HIGH or Z (pulse mode) and pressing the T (or ✳) key writes the data required to switch to tone mode into memory. When the IC is in pulse mode, and a T or ✳ key is pressed while the dial signal is being sent, a 3.6-s pause is inserted after all digits up to that key have been transmitted and all subsequent dial signals are transmitted as tones. In this case the ✳ signal is sent out as a DTMF signal. If a T or ✳ key is entered after the dial signal has been transmitted (after $\overline{\text{DPMUTE}}$ goes from the LOW to the Z state) no pause is inserted.

Since the data for switching to tone mode is stored in the redial memory, mixed mode can also be used when redialing. When the IC redials, it always starts the redial in the mode that it was in when the numbers were initially dialed, no matter what the state of the MODEIN pin.

Hooking (↑) H. This sequence executes an on-hook sequence. A hook pause is automatically entered after the end of an on-hook sequence. If a dial signal is being transmitted when the H is pressed, the dial sequence is immediately interrupted and the on-hook sequence starts. Hook time is 708 ms.

When the H key is pressed, the following operations are performed in the IC:

- Input mode is reset, and the circuit goes to the pulse mode wait state (waiting for key inputs). If the MODEIN pin is LOW, the mode is changed to Tone.
- The write pointer is reset and the redial buffer is enabled.

Note: The hooking input is not written into memory. The operator can press any other keys after the H key is pressed. When the hooking operation is in progress, the only key input that is not accepted is the H key.

Table 8 Operating example: 4 × 4 keypad

Operation	Key sequence	Dial output	Redial memory contents
Normal dialing 1 MODEIN = HIGH	(↑) 1, 2, 3, 4	Pulse 1, 2, 3, 4 at 20 pps	1, 2, 3, 4
Normal dialing 2 MODEIN = Z	(↑) 1, 2, 3, 4	Pulse 1, 2, 3, 4 at 10 pps	1, 2, 3, 4
Normal dialing 3 MODEIN = LOW	(↑) 1, 2, 3, 4	DTMF 1, 2, 3, 4	T, 1, 2, 3, 4
Access pause	(↑) 0, P_A, 1, 2, 3	0, (pause 3.6 s), 1, 2, 3	0, P_A, 1, 2, 3
Break in progress pause	(↑) 0, P_A, 1, 2, 3 (↓) or (↑)R●P_A	0, (pause 3.6 s), 1, 2, 3 0, (pause ≤ 3.6 s), 1, 2, 3 (Press P_A for break in progress)	0, P_A, 1, 2, 3 0, P_A, 1, 2, 3
Redial 1	(↑) 1, 2, 3, 4 (↓) (↑)R	1, 2, 3, 4 1, 2, 3, 4	1, 2, 3, 4 1, 2, 3, 4
Redial 2	1, 2, 3.....32, 33 (↑) 1, 2, 3 ... 2, 3, (↓) (↑)R	1, 2, 3, ... 2, 3 No output	Memory cleared Memory cleared
Inhibit redial 1	(↑) 1, 2, 3, 4 ○ R, R (↓) (↑)R	1, 2, 3, 4 No output	Memory cleared Memory cleared
Inhibit redial 2	(↑) 1, 2, 3, 4 (↓) (↑)R○ R, R (↓) (↑)R	1, 2, 3, 4 1, 2, 3, 4 No output	1, 2, 3, 4 Memory cleared Memory cleared
Switch modes using T key MODEIN = HIGH or Z	(↑) 1, 2, T, 3, 4 (↓) (↑)R	1, 2, (pause 3.6 s), 3, 4 Pulse DTMF 1, 2, (pause 3.6 s), 3, 4 Pulse DTMF	1, 2, T, 3, 4 1, 2, T, 3, 4
Switch modes using ✳ key MODEIN = HIGH or Z	(↑) 1, 2, ✳, #, ✳(↓)	1, 2, (pause 3.6 s),#, ✳ Pulse DTMF	1, 2, T, #, ✳
On-hook	(↑)H	Hook sequence	

● Follow-on key pressed during pause
○ Follow-on key pressed after previous input processed

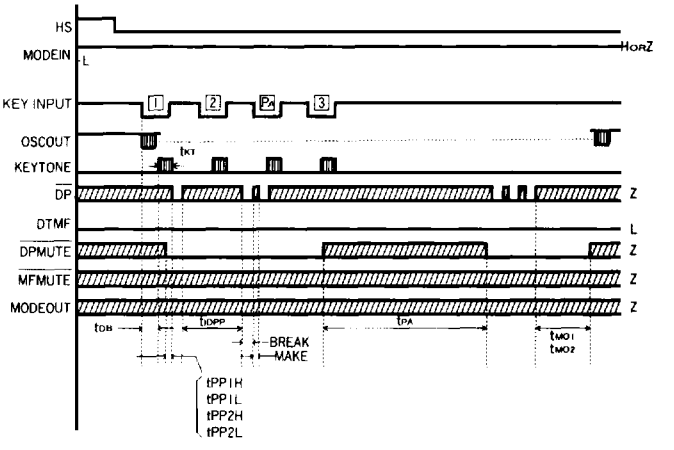


Figure 3 Pulse dial timing (KEY/CPU pin HIGH)

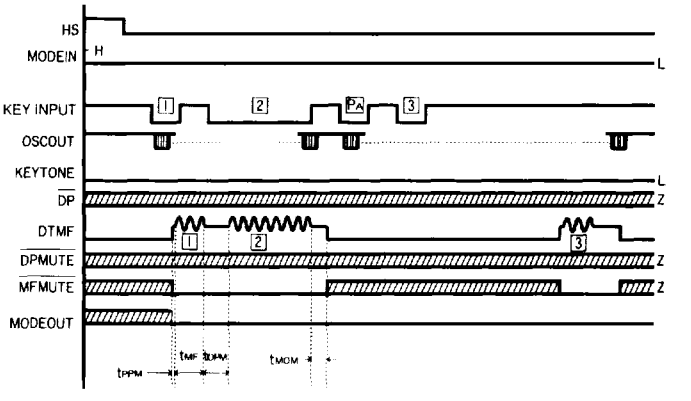


Figure 4 Tone dial timing (KEY/CPU pin HIGH)

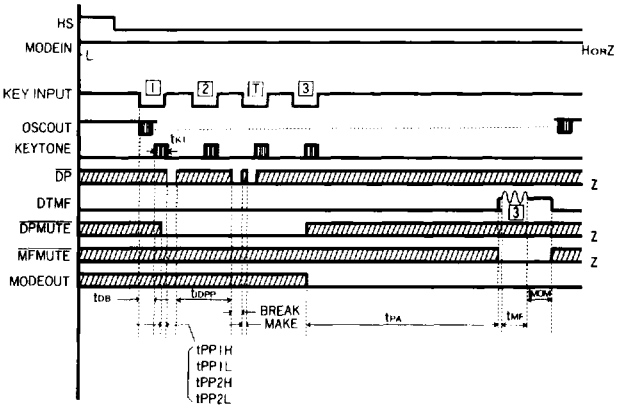


Figure 5 Pulse and tone mixed dial timing (KEY/CPU pin HIGH)

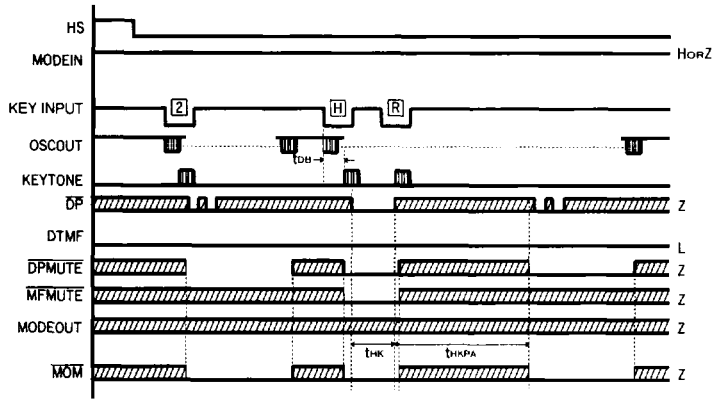


Figure 6 Hooking and redial timing (KEY/CPU pin HIGH)

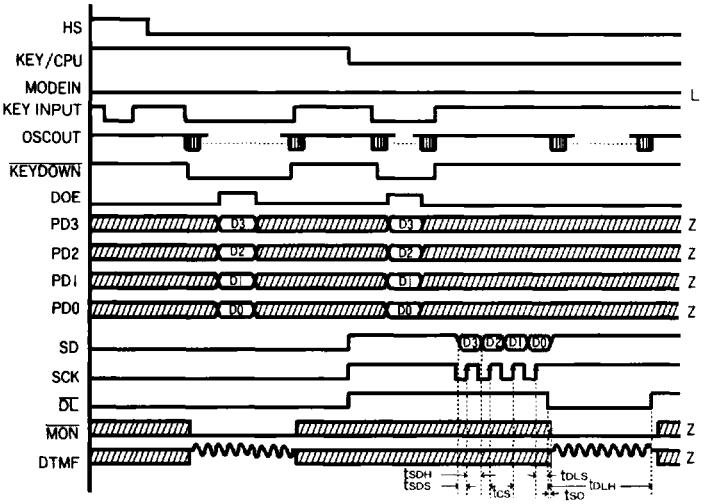


Figure 7 CPU interface timing

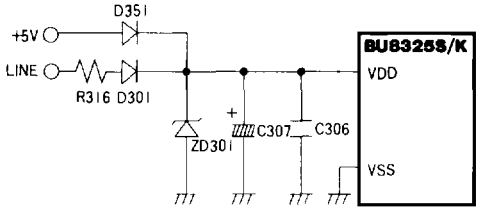
Application

Note: The BU8390AS/AK application board can be used as an application board for the BU8325S and BU8325K ICs. When this board is used for the BU8325S/K, the LH/SH switch performs the DOE function.

Selecting external circuit components

The following section specifies the external components that are required to ensure that the IC functions as intended.

Figure 8 Supply voltage external circuit

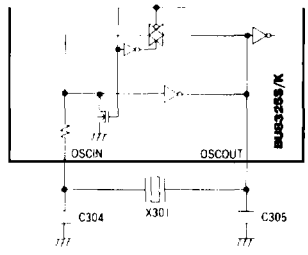


C306, C307: V_{DD} bypass capacitors
ZD301: Prevents the supply voltage from rising above 5.5 V. (Use a 5.1-volt zener.)

D301, D351: Reverse current blocking diodes. Connect the +5 V terminal of this circuit to the CPU 5-volt supply (Spec. 1SS133).

R316: This resistor applies supply voltage from the telephone circuit to the dialer. It also alters the ac impedance of the telephone. The LINE terminal of this circuit should be connected to the VL pin of the speech network IC. When selecting the value of R316, consider not only the voltage that needs to be applied to the dialer, but also the affect of the resistor on the ac impedance of the telephone.

Figure 9 Oscillator circuit



X301: Use a 3.579545 MHz piezoelectric or ceramic resonator. For recommended ceramic resonators, see the table "Recommended operating conditions" on page 134.

C304, C305: These are loading capacitors required if a ceramic resonator is used. Use 33-pF CH-type capacitors. If a 3-pin resonator with built-in capacitors is used, C304 and C305 are not required.

CPU interface

Keypad input mode When the KEY/CPU pin is HIGH, the IC is in the keypad input mode. Data entered from a keypad connected to the BU8325S/K is converted into 4-bit key codes by a 4 × 4 key encoder, and the codes are transferred to the dial circuit. The key codes perform operations as defined by the dialer, and are also output to the CPU as parallel data when the DOE pin is HIGH.

CPU input mode When the KEY/CPU pin is LOW, the IC is in the CPU input mode. Data entered at a keypad connected to the BU8325S/K is converted into 4-bit key codes by a 4 × 4 key encoder, and output to the CPU as parallel data. In this mode, the dial circuit is operated by serial data from the CPU. This allows data entered from the keypad to be processed against special function data as defined by the CPU (for instance, time stamps or secret code registration). The data sent to the dial circuit can also be defined as desired, and sent under CPU program control. Having a KEY/CPU pin to switch the CPU in and out of the dial signal path makes it easy to implement a variety of useful telephone functions, such as the capability to dial out during a power failure.

Figure 10 CPU interface

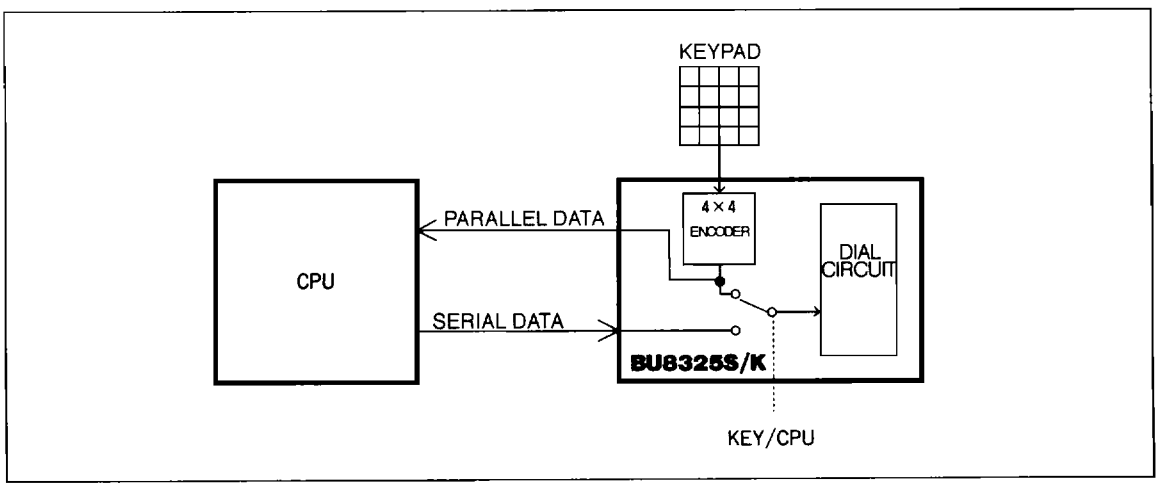
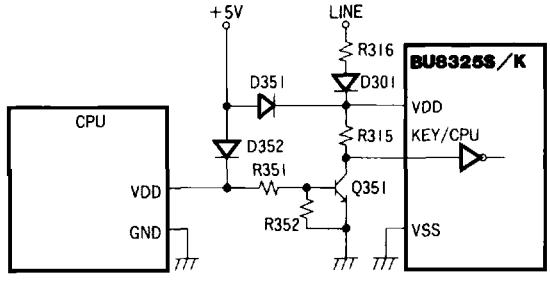


Figure 11 KEY/CPU pin external circuit



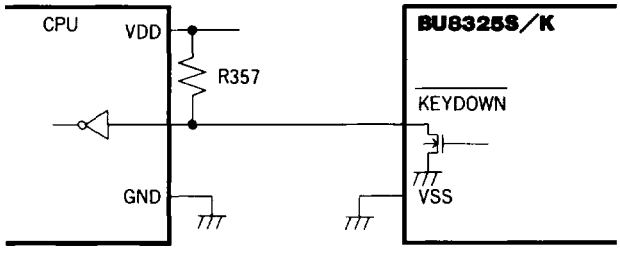
KEY/CPU pin input logic levels
Normal operation (5-V supplied): Q351 on; KEY/CPU pin LOW.
Power failure (no 5-V supply): Q351 off; KEY/CPU pin HIGH

The circuit is configured so that when a power failure occurs, and the CPU is out of operation, the circuit will switch the IC from CPU-input to keypad-input mode.

D352: Diode to apply power from the +5-V supply to the CPU. The diode keeps the V_{DD} voltage applied to the CPU about the same as that applied to the BU8325S/K. (Specification 1SS133)

R315: KEY/CPU pin pull-up resistor
R351, R352: Base resistors for Q351. The voltage at which Q351 will detect a drop in the 5-V supply is determined by the ratio of these resistors.

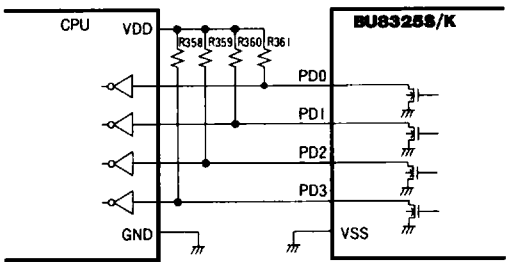
Figure 12 $\overline{\text{KEYDOWN}}$ pin external circuit



When the HS pin is LOW (off-hook), the $\overline{\text{KEYDOWN}}$ pin outputs a LOW when any valid key input is entered at a keypad connected to the BU8325S/K. This is true regardless of the state of the KEY/CPU pin. The $\overline{\text{KEYDOWN}}$ pin is usually connected to an interrupt input port on the CPU.

The $\overline{\text{KEYDOWN}}$ pin is an N-channel open drain output. It should be pulled up through a resistor (R357) to the CPU supply voltage V_{DD} (+5 V) at the CPU input pin.
Use a resistor of at least 20 kΩ. (If you use a CPU with internal pull-up resistors, verify that they are 20 kΩ or greater.)

Figure 13 PD0 ~ PD3 pins

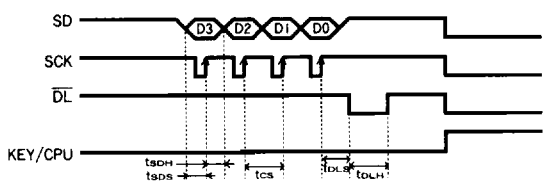


When the HS pin is LOW (off hook), these four pins output 4-bit parallel data (serial-to-parallel converted data) corresponding to the keyboard keys that are pressed, regardless of the KEY/CPU pin state. Non-valid key data generated by pressing more than one key is also output. Since $\overline{\text{KEYDOWN}}$ stays in the Z state when multiple keys are pressed, data must be taken from these pins only when $\overline{\text{KEYDOWN}}$ is LOW.

The Z state is defined as "1" data and the LOW state is "0" data. PD0 ~ PD3 go to the Z state when no data is being output, or HS is HIGH (on hook), or DOE is LOW (disabled). This use of the high impedance state avoids the waste of power in the pull-up resistors. The PD0 ~ PD3 pins are usually connected to a 4-bit parallel input at the CPU.

PD0 ~ PD3 are N-channel open drain outputs. Pull these outputs up through the resistors R358 - R361 from the CPU V_{DD} (+5 V) at the CPU input. The resistors should be at least 20 kΩ. (If you use a CPU with internal pull-up resistors, verify that they are 20 kΩ or greater.)

Figure 14 SD, SCK, and $\overline{\text{DL}}$ pins



When KEY/CPU pin is LOW (CPU) the SD, SCK, and $\overline{\text{DL}}$ pins are used to bring in serial data from the CPU. (All three pins are CMOS inputs that are pulled up to V_{DD} and pulled-down to V_{SS} through internal resistors.)

When the KEY/CPU pin is LOW the inputs are enabled, and when the KEY/CPU pin is HIGH, the inputs are disabled.

The pins are normally connected to a serial data output port on the CPU end, but if the CPU does not have enough serial output ports, a general purpose port can be used.

The SCK input circuit uses a Schmidt trigger to prevent erratic operation due to noise on the clock.

The CPU outputs you use should be able to sink at least 500 µA at a V_{DD} of 5.0 V.

Serial data input specifications are listed in Table 9. The longer NMOS times and cycle periods (as compared to CMOS) result from time delays in NMOS open drain interfaces due to the RC time constants of internal pull-up resistors and floating capacitors. This should be taken into account during circuit design.

Note: The circuit in Figure 15 is recommended if there is a need to further reduce the NMOS open drain interface specifications

Table 9 Data input specifications

Parameter	Symbol	CMOS	NMOS
SD setup time	t_{SDS}	100 ns max	2 µs max
SD hold time	t_{SDH}	100 ns max	10 µs max
Serial clock cycle period	t_{CS}	500 ns min	20 µs min
DL setup time	t_{DLS}	500 ns min	500 ns min
DL hold time	t_{DLH}	15 ms min	15 ms min

Figure 15 Application example: Circuit to improve data input speed in an NMOS I/F

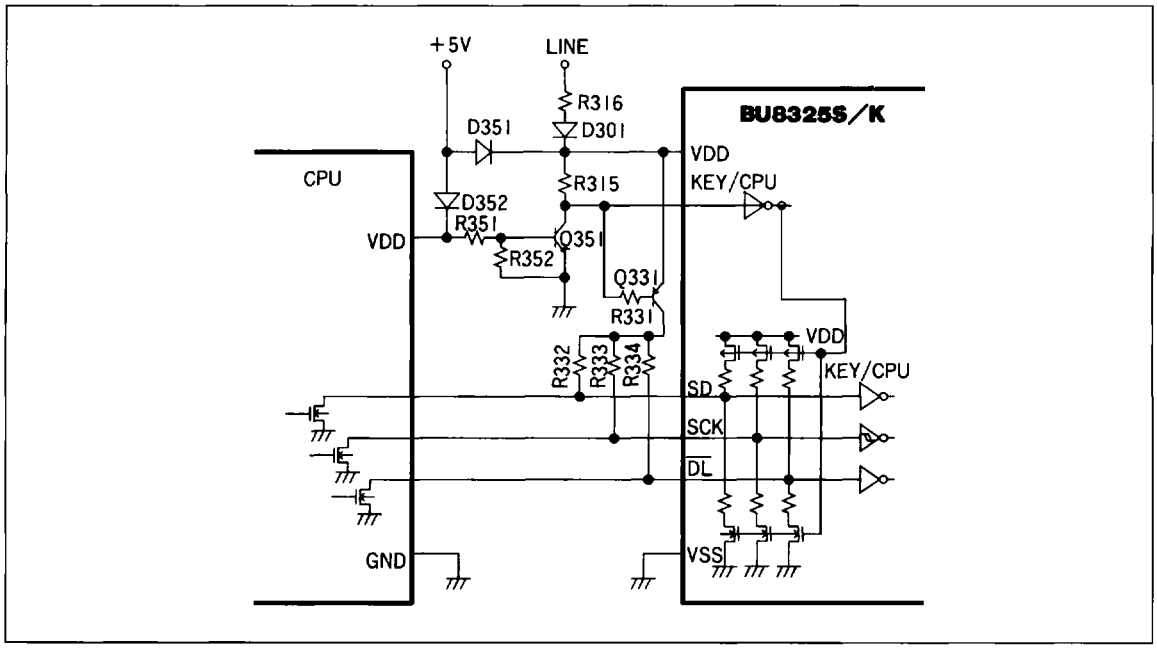


Figure 16 Serial data input timing

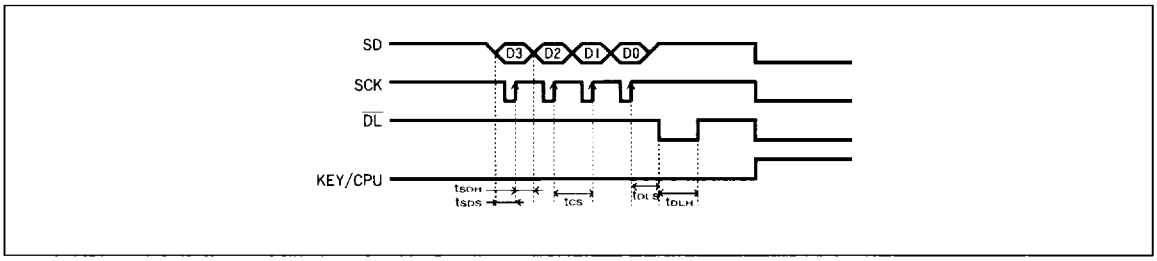


Figure 17 Parallel data output timing (KEYDOWN, PD0 ~ PD3, key input, DOE pin HIGH)

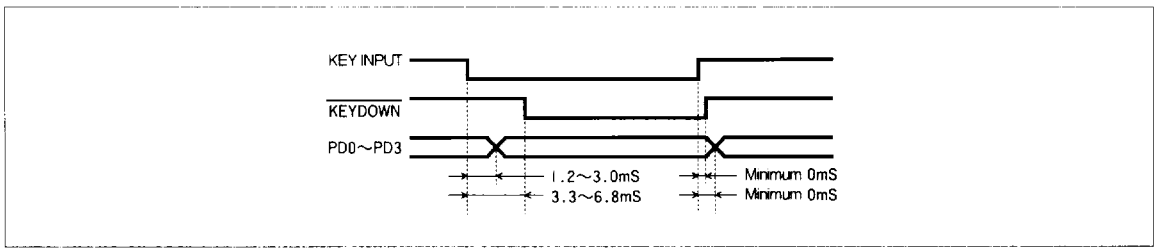
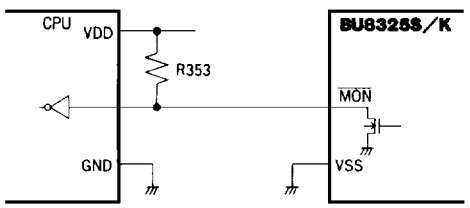


Figure 18 $\overline{\text{MON}}$ pin connections



The $\overline{\text{MON}}$ pin is LOW while the dial signal (including pauses) is transmitted. It is in the high impedance (Z) state if no dial signal is being sent, or if the HS pin is HIGH (on-hook).
At the CPU, this pin is usually connected to a general purpose input port.

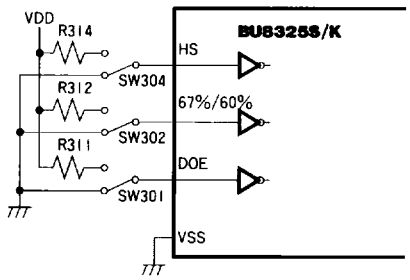
The $\overline{\text{MON}}$ pin is an N-channel open drain output. Pull up the $\overline{\text{MON}}$ pin through resistor R353 from the CPU V_{DD} (+5 V) at the CPU input. The resistor should be at least 20 kΩ. (If you use a CPU with an internal pull-up resistor, verify that it is 20 kΩ or greater.)

Note: CPU program considerations: Parallel data output on the PD0 ~ PD3 pins of the BU8325S/K is valid while $\overline{\text{KEYDOWN}}$ is LOW and the DOE pin is HIGH. $\overline{\text{KEYDOWN}}$ is disabled if more than one key is pressed. Since no key debounce period is set, the CPU program must preclude the reading-in of erroneous data due to key chattering.

When transferring data from the CPU to the BU8325S/K, no more than 32 digits can be transferred at one time. If you have more than 32 digits to transfer, send the first 32 digits; then monitor the $\overline{\text{MON}}$ pin until the high impedance (Z) state returns before sending the next 32 digits.

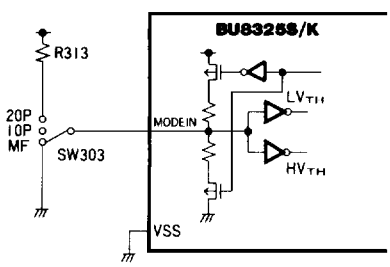
The redial buffer is a 32-digit ring buffer. If more than 32 digits come in at high speed, the digits that have not left the buffer can be overwritten, resulting in the wrong dial data being sent out.

Figure 19 HS, 67%/60%, and DOE pins



R311, R312, and R314:
When shorting-type switches are used for SW301, SW302, and SW304, V_{DD} is momentarily shorted to ground as the switch slides from one position to the other. R311, R312, and R314 are used to prevent a drop in supply voltage when this occurs. Use 100 kΩ (approximately) resistors.

Figure 20 MODEIN pin connections

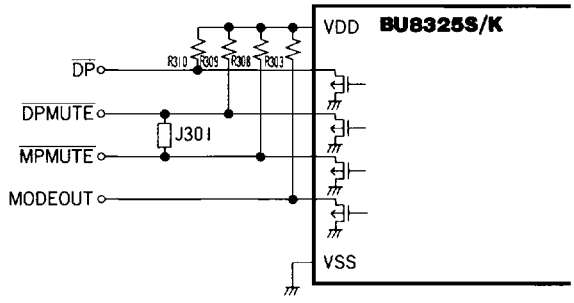


The MODEIN pin is the mode select pin. A LOW level on this pin selects tone mode, an open pin (Z state) selects the 10 pps pulse mode, and a HIGH level selects the 20 pps pulse mode.

When the T key is pressed, tone mode is always selected, regardless of the state of this pin. The MODEIN state is set in the IC when the first digit is read-in after going off-hook. When this first digit is read in, internal resistors (to sense the Z state) are connected between V_{SS} and V_{DD} by transistor switches as shown in the illustration.

R313: When a shorting-type switch is used for SW303, V_{DD} is momentarily shorted to ground as the switch slides between positions. R304 is used to prevent a momentary drop in supply voltage when this occurs. (Consider using an IC-internal resistor for this. Use about a 10 kΩ resistor.)

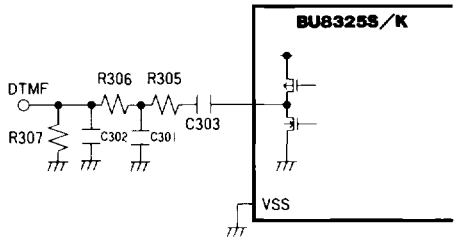
Figure 21 $\overline{\text{DP}}$, $\overline{\text{DPMUTE}}$, $\overline{\text{MFMUTE}}$, and $\overline{\text{MODEOUT}}$ pin connections



R303, R308, R309, and R310: Pull-up resistors for the NMOS open drain outputs. These resistors are only required for waveform monitoring; they are not required for normal use. Use 100 kΩ (approximately) resistors.
J301: This is an optional jumper that can be used to connect the outputs of $\overline{\text{DPMUTE}}$ and $\overline{\text{MFMUTE}}$. If J301 is inserted in the circuit as shown, both pins will go LOW during dial pulse or DTMF signal transmission.

$\overline{\text{DP}}$ In pulse mode, this pin outputs dial pulses (contact make and break sequences) corresponding to the pressed keys (Z = make; LOW = break). This pin goes to the high impedance state when not sending dial pulses.
$\overline{\text{DPMUTE}}$ This pin goes LOW when a dial pulse is being output or an on-hook sequence is in progress. It goes to the high impedance state in tone mode, when no dial pulse is output, and when the unit is on-hook.
$\overline{\text{MFMUTE}}$ This pin goes LOW when DTMF signals are output or when an on-hook sequence is in progress. It goes to the high impedance state in pulse mode or when no DTMF signal is being output, or when the unit is on-hook.
$\overline{\text{MODEOUT}}$ This pin outputs the dial signal output mode status. It goes to the high impedance state in pulse mode, and to the LOW state when in tone mode. It also goes to the high impedance state when the unit is the on-hook state.

Figure 22 DTMF pin connections



In tone mode, this pin outputs a DTMF signal that corresponds to the keyed data. It goes to the low impedance (Z) state when no DTMF tone is being transmitted.

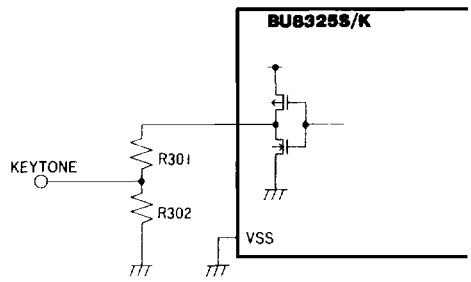
C301, C302: These capacitors form, along with R305 and R306, a low-pass filter that removes the high frequency components of the DTMF output. (Use a 15-nF capacitor for C301, and a 33 nF capacitor for C302.)

R305, R306: Use a 5.1-kΩ resistor for R305 and R306

C303: Blocks the dc component of the DTMF output. (Use a 100-nF capacitor.)

R307: The DTMF output is developed across this voltage divider resistor.

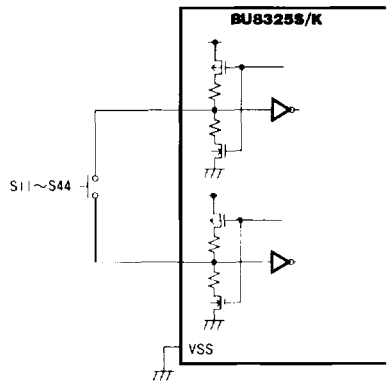
Figure 23 KEYTONE pin connections



This pin outputs key-press confirmation tones. This pin outputs a key tone (square wave) for all valid data inputs in pulse mode, and for valid P_A, R, or H data inputs in tone mode. The output frequency (f_{KT}) is 1193 Hz and the pulse width (t_{KT}) is 34 ms. The pin is LOW when no tone is output.

R301, R302: These two resistors form an attenuator that reduces the keytone output level. R301 should be at least 8 kΩ.

Figure 24ROW1 ~ ROW4, COL1 ~ COL4 pin connections



These pins can be connected to a 4 × 4 keypad. A valid key entry sequence can be either:

Connecting a $\overline{\text{ROW}}$ input to a $\overline{\text{COL}}$ input
Taking a $\overline{\text{ROW}}$ input and a $\overline{\text{COL}}$ input LOW simultaneously

In pulse mode, if more than one key is pressed at the same time, the entry is ignored.
In tone mode, you can generate a single tone by pressing two or more keys in the same row or the same column. If multiple keys not in the same row or the same column are pressed, the entry is ignored.

S11 - S44: Keypad switches. Use switches with contact resistance of 2 kΩ or less.

Table 10 Parts list

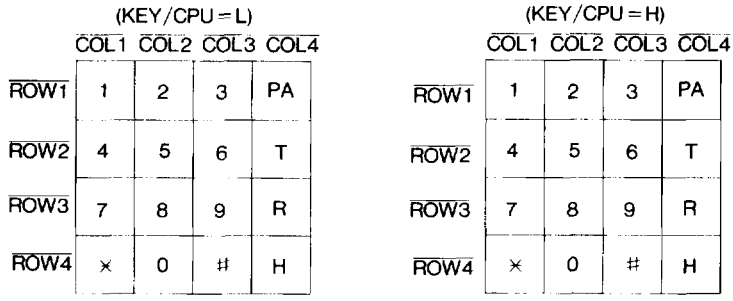
Part no.	Component	Specification	Part no.	Component	Specification
C301	Film capacitor	15 nF	R311	Carbon resistor	100 kΩ, 1/8 W
C302	Film capacitor	33 nF	R312	Carbon resistor	100 kΩ, 1/8 W
C303	Film capacitor	100 nF	R313	Carbon resistor	10 kΩ, 1/8 W
C305	Ceramic capacitor	33 pF type	R314	Carbon resistor	100 kΩ, 1/8 W
C306	Film capacitor	10 nF	R315	Carbon resistor	100 kΩ, 1/8 W
C307	Electrolytic capacitor	100 µF, 6.3 V	R316	Carbon resistor	3.3 kΩ, 1/8 W
R301	Carbon resistor	1 kΩ, 1/8 W	SW301	Toggle switch	2-posn. switch
R302	Carbon resistor	220 kΩ, 1/8 W	SW302	Toggle switch	2-posn. switch
R303	Carbon resistor	100 kΩ, 1/8 W	SW303	Slide switch	3-posn. switch
R305	Carbon resistor	5.1 kΩ, 1/8 W	SW304	Toggle switch	2-posn. switch
R306	Carbon resistor	5.1 kΩ, 1/8 W	D301	Diode	1SS133
R307	Carbon resistor	5.1 kΩ, 1/8 W	ZD301	Zener diode	5.1 V
R308	Carbon resistor	100 kΩ, 1/8 W	X01	Oscillator	3.579545 MHz piezo or ceramic resonator
R309	Carbon resistor	100 kΩ, 1/8 W	S11 ~ S44	Push-button switch	Single contact
R310	Carbon resistor	100 kΩ, 1/8 W			

Software ROM

The two software ROMs described below are available for use with an AB-8325CPU to check BU8325S/ K operation.

8325AA03

Figure 25 8325AA03 keypad functions



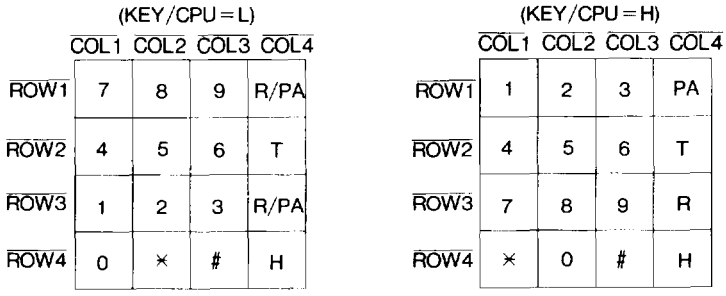
Since parallel data output from the BU8309AS/AK is output from the CPU without modification as serial data, the apparent operation is the same as that shown above for KEY/CPU = H.

Table 11 Data conversion table

BU8325S/K parallel data output					BU83325S/K serial data input				
Pressed key	**D3**	**D2**	**D1**	**D0**	**Data**	**D3**	**D2**	**D1**	**D0**
ROW4, COL4	0	0	0	0	H	0	0	0	0
ROW1, COL1	0	0	0	1	1	0	0	0	1
ROW1, COL2	0	0	1	0	2	0	0	1	0
ROW1, COL3	0	0	1	1	3	0	0	1	1
ROW2, COL1	0	1	0	0	4	0	1	0	0
ROW2, COL2	0	1	0	1	5	0	1	0	1
ROW2, COL3	0	1	1	0	6	0	1	1	0
ROW3, COL1	0	1	1	1	7	0	1	1	1
ROW3, COL2	1	0	0	0	8	1	0	0	0
ROW3, COL3	1	0	0	1	9	1	0	0	1
ROW4, COL2	1	0	1	0	0	1	0	1	0
ROW4, COL1	1	0	1	1	*	1	0	1	1
ROW4, COL3	1	1	0	0	#	1	1	0	0
ROW2, COL4	1	1	0	1	T	1	1	0	1
ROW1, COL4	1	1	1	0	P_A	1	1	1	0
ROW3, COL4	1	1	1	1	R	1	1	1	1

8325AB02

Figure 26 8325AB02 keypad functions



Parallel data output from the BU8325S/K is first converted by the CPU and then output as serial data. The R/P_A key is the AB-8309CPU INIT button. The R/P_A key serves as the AB8309 CPU INIT key. (Originally it was intended to input the state of the HS pin to the CPU, but since there was no port to send it to, the INIT button was substituted.) When the R/P_A button is pressed, the program is set up to output first the R and then the P_A. Both are output as serial data.

Table 12 Data conversion table

BU8325S/K Parallel data output					BU8325S/K Serial data input				
Pressed key	**D3**	**D2**	**D1**	**D0**	**Data**	**D3**	**D2**	**D1**	**D0**
$\overline{ROW4}$, $\overline{COL4}$	0	0	0	0	H	0	0	0	0
$\overline{ROW1}$, $\overline{COL1}$	0	0	0	1	7	0	1	1	1
$\overline{ROW1}$, $\overline{COL2}$	0	0	1	0	8	1	0	0	0
$\overline{ROW1}$, $\overline{COL3}$	0	0	1	1	9	1	0	0	1
$\overline{ROW2}$, $\overline{COL1}$	0	1	0	0	4	0	1	0	0
$\overline{ROW2}$, $\overline{COL2}$	0	1	0	1	5	0	1	0	1
$\overline{ROW2}$, $\overline{COL3}$	0	1	1	0	6	0	1	1	0
$\overline{ROW3}$, $\overline{COL1}$	0	1	1	1	1	0	0	0	1
$\overline{ROW3}$, $\overline{COL2}$	1	0	0	0	2	0	0	1	0
$\overline{ROW3}$, $\overline{COL3}$	1	0	0	1	3	0	0	1	1
$\overline{ROW4}$, $\overline{COL2}$	1	0	1	0	*	1	0	1	1
$\overline{ROW4}$, $\overline{COL1}$	1	0	1	1	0	1	0	0	0
$\overline{ROW4}$, $\overline{COL3}$	1	1	0	0	#	1	1	0	0
$\overline{ROW2}$, $\overline{COL4}$	1	1	0	1	T	1	1	0	1
$\overline{ROW1}$, $\overline{COL4}$	1	1	1	0	R	1	1	1	1
$\overline{ROW3}$, $\overline{COL4}$	1	1	1	1	P_A	1	1	1	0

Figure 27 CPU board (APB-8309CPU) circuit diagram

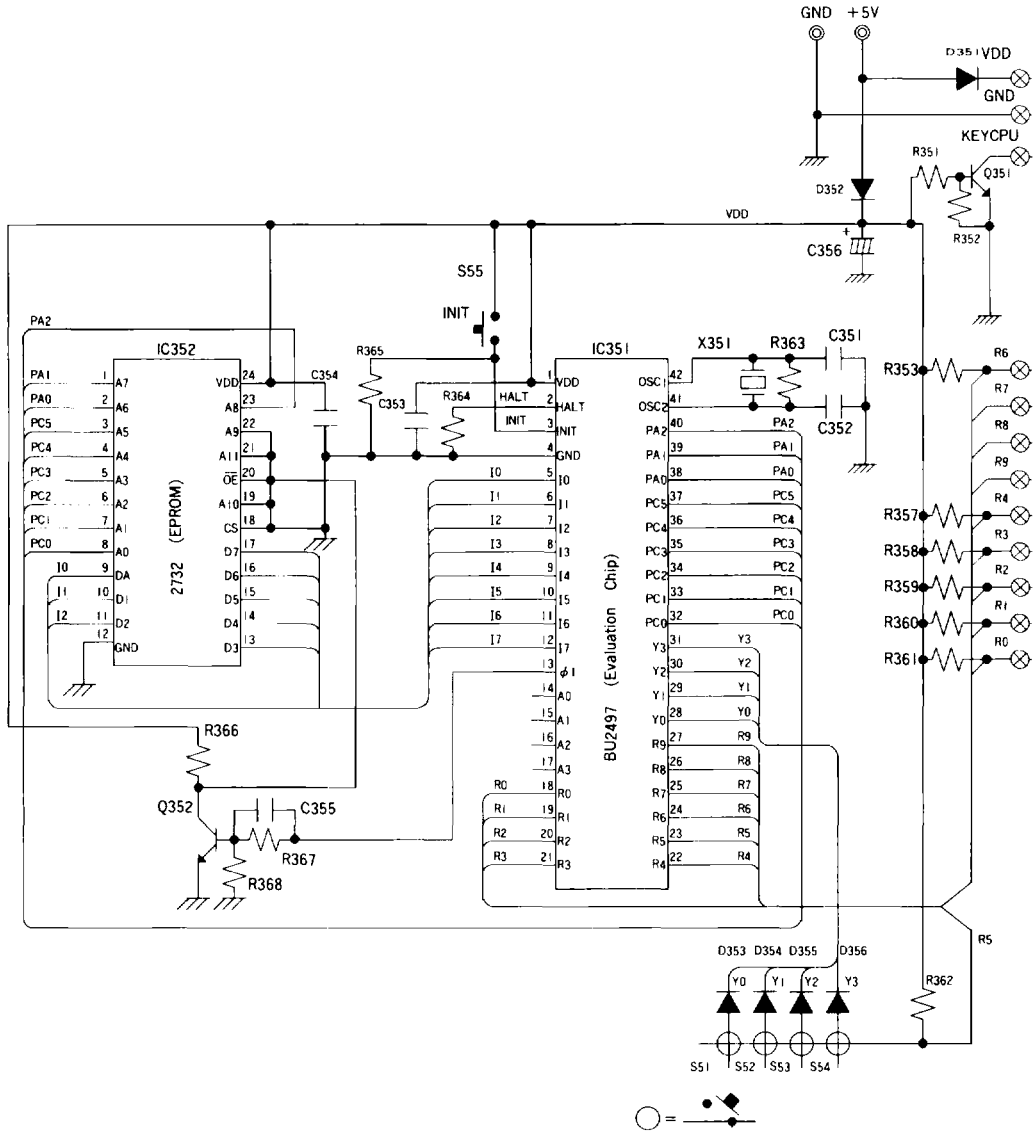
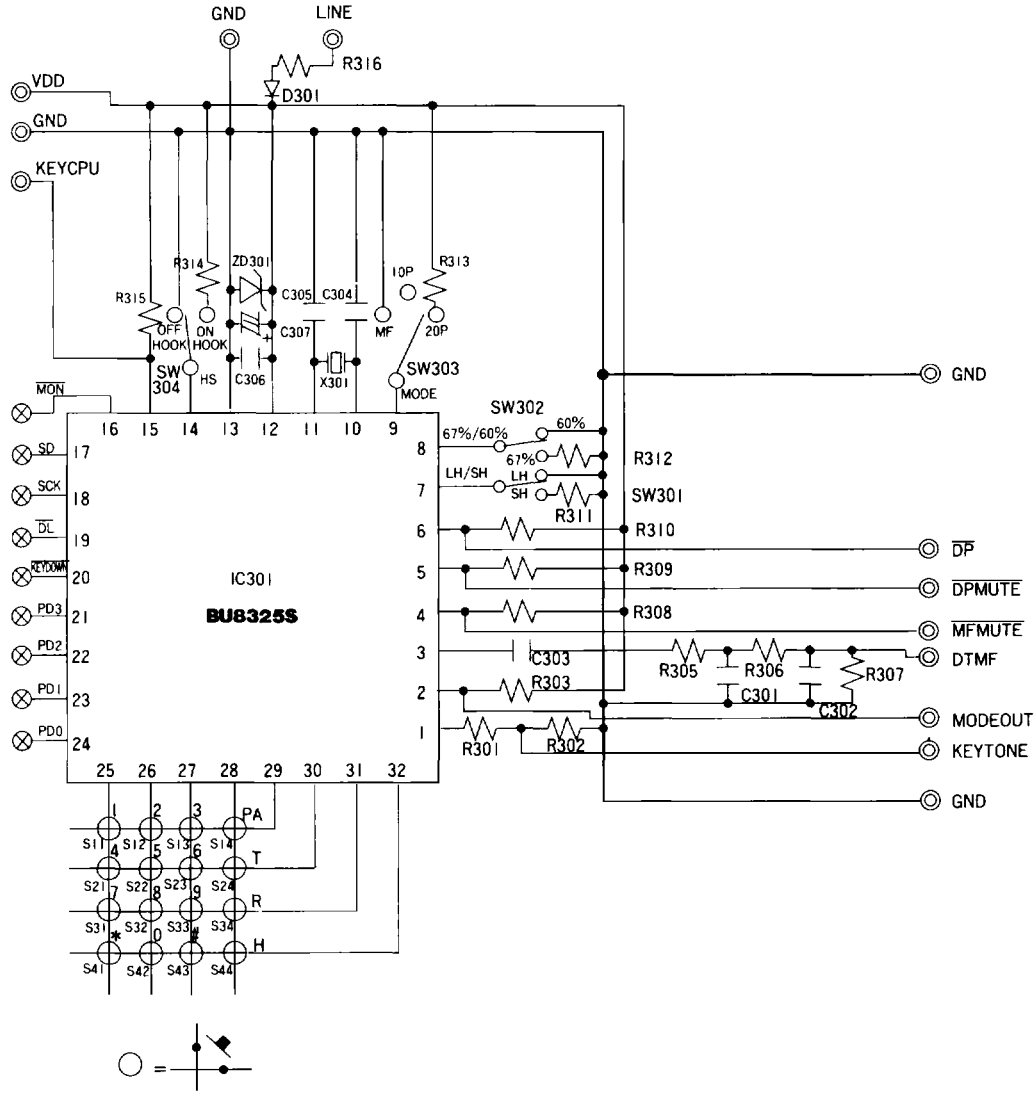


Figure 28 Dialer board (APB-8309DIA) circuit diagram



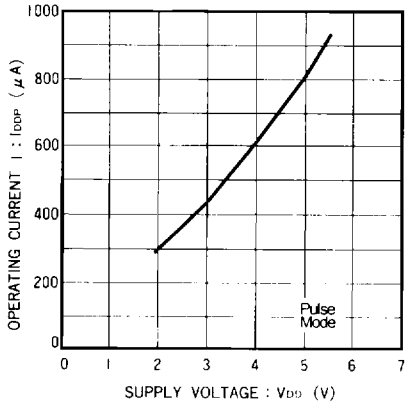


Figure 29

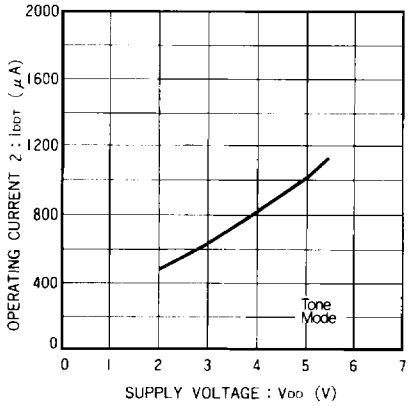


Figure 30

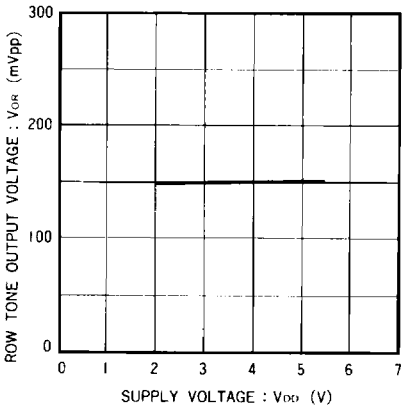


Figure 31

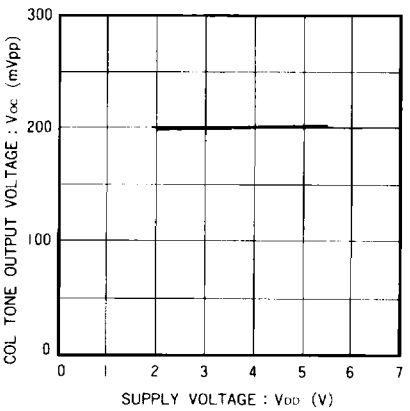


Figure 32

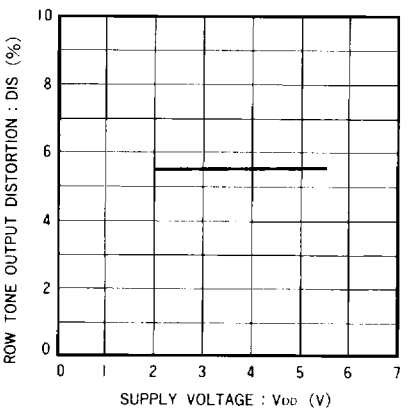


Figure 33

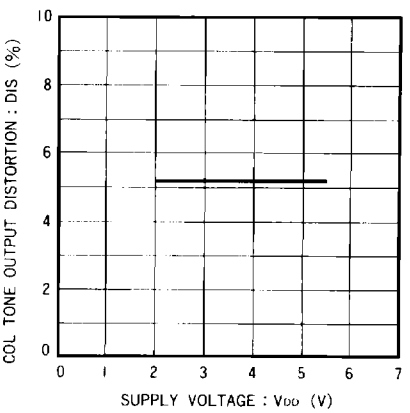


Figure 34