

# TOSHIBA MOS MEMORY PRODUCTS

THM81002S/L-85, 10, 12

## DESCRIPTION

The THM81002S/L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511002J on the printed circuit board.

The THM81002S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

## FEATURES

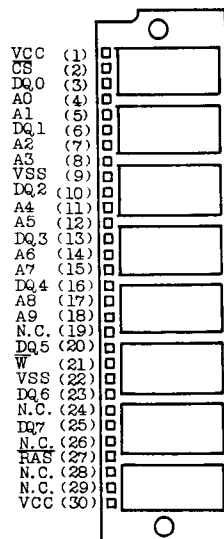
- 1,048,576 words by 8 bits organization
- Fast access time

	THM81002S/L-85	THM81002S/L-10	THM81002S/L-12
$t_{RAC}$ $\overline{RAS}$ Access Time	85ns	100ns	120ns
$t_{AA}$ Column Address Access Time	45ns	50ns	60ns
$t_{CAC}$ $\overline{CS}$ Access Time	25ns	25ns	30ns
$t_{RC}$ Cycle Time	165ns	190ns	220ns
$t_{SC}$ Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V±10%
- Low power
  - 3,080mW MAX. Operating (THM81002S/L-85)
  - 2,640mW MAX. Operating (THM81002S/L-10)
  - 2,200mW MAX. Operating (THM81002S/L-12)
  - 44mW MAX. Standby
- $\overline{CS}$  before  $\overline{RAS}$  refresh,  $\overline{RAS}$  only refresh, Hidden refresh, and Static Column Mode capability.
- All Inputs and Outputs TTL Compatible
- 512 refresh cycles/8ms

## PIN CONNECTION

(TOP VIEW)

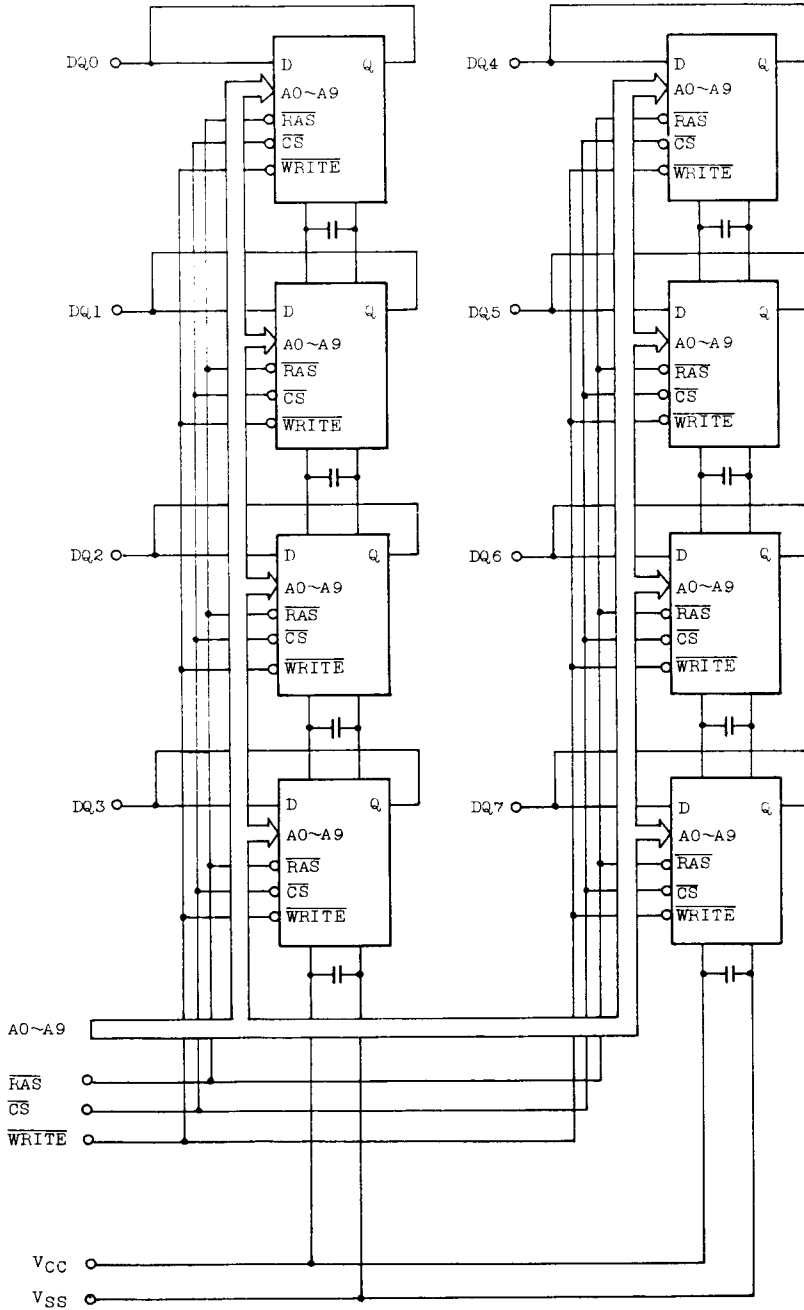


## PIN NAMES

A0 ~ A9	Address Inputs
DQ0 ~ DQ7	Data Input/Outputs
$\overline{CS}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
VCC	Power (+5V)
VSS	Ground
N.C.	No Connection

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## BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	$V_{IN}$	-1.0 ~ 7.0	V	1
Output Voltage	$V_{OUT}$	-1.0 ~ 7.0	V	1
Power Supply Voltage	$V_{CC}$	-1.0 ~ 7.0	V	1
Operating Temperature	$T_{OPR}$	0 ~ 70	°C	1
Storage Temperature	$T_{STG}$	-55 ~ 125	°C	1
Soldering Temperature • Time	$T_{SOLDER}$	260 • 10	°C • sec	1
Power Dissipation	$P_D$	4.8	W	1
Short Circuit Output Current	$I_{OUT}$	50	mA	1

## RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	2
$V_{IH}$	Input High Voltage	2.4	-	6.5	V	2
$V_{IL}$	Input Low Voltage	-1.0	-	0.8	V	2

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{RAS}$ , $\overline{CS}$ , Address Cycling: $t_{RC}=t_{RC}$ MIN.)	THM81002S/L-85	-	560	mA	3, 4
		THM81002S/L-10	-	480		
		THM81002S/L-12	-	400		
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CS}=V_{IH}$ )	-	16	mA		
I <sub>CC3</sub>	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ( $\overline{RAS}$ Cycling, $\overline{CS}=V_{IH}$ : $t_{RC}=t_{RC}$ MIN.)	THM81002S/L-85	-	560	mA	3
		THM81002S/L-10	-	480		
		THM81002S/L-12	-	400		
I <sub>CC4</sub>	FAST PAGE MODE CURRENT Average Power Supply Current, Static Column Mode ( $\overline{RAS}=\overline{CS}=V_{IH}$ , Address Cycling: $t_{SC}=t_{SC}$ MIN.)	THM81002S/L-85	-	400	mA	3, 4
		THM81002S/L-10	-	320		
		THM81002S/L-12	-	240		
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{RAS}=\overline{CS}=V_{CC}-0.2V$ )	-	8	mA		
I <sub>CC6</sub>	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ( $\overline{RAS}$ , $\overline{CS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	THM81002S/L-85	-	560	mA	3
		THM81002S/L-10	-	480		
		THM81002S/L-12	-	400		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ( $0V \leq V_{IN} \leq 6.5V$ , All Other Pins not under Test=0V)	-80	80	μA		
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT ( $D_{OUT}$ is disabled, $0V \leq V_{OUT} \leq 5.5V$ )	-20	20	μA		
V <sub>OH</sub>	OUTPUT LEVEL Output "H" Level Voltage ( $I_{OUT}=-5mA$ )	2.4	-	V		
V <sub>OL</sub>	OUTPUT LEVEL Output "L" Level Voltage ( $I_{OUT}=4.2mA$ )	-	0.4	V		

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## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $V_{CC}=5V\pm 10\%$ ,  $T_a=0\sim 70^\circ C$ ) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81002S/L-85		THM81002S/L-10		THM81002S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
$t_{SC}$	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
$t_{RAC}$	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
$t_{CAC}$	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
$t_{AA}$	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
$t_{CLZ}$	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
$t_{OFF}$	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
$t_{AOH}$	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
$t_{OW}$	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
$t_{WOH}$	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
$t_{RP}$	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
$t_{RASC}$	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
$t_{RSH}$	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
$t_{CSH}$	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
$t_{CS}$	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
$t_{CSC}$	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
$t_{CRP}$	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
$t_{CP}$	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
$t_{ASR}$	Row Address Set-Up Time	0	-	0	-	0	-	ns	
$t_{RAH}$	Row Address Hold Time	15	-	15	-	15	-	ns	
$t_{ASC}$	Column Address Set-Up Time	0	-	0	-	0	-	ns	
$t_{CAH}$	Column Address Hold Time	20	-	20	-	25	-	ns	
$t_{AWR}$	Write Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

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## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81002S/L-85		THM81002S/L-10		THM81002S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{AR}$	Column Address Hold Time referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
$t_{AH}$	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
$t_{CWL}$	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{RCS}$	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
$t_{RCH}$	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
$t_{RRH}$	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
$t_{WH}$	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
$t_{WCR}$	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{WP}$	Write Command Pulse Width	20	-	20	-	25	-	ns	
$t_{WI}$	Write Command Inactive Time	10	-	10	-	15	-	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
$t_{DS}$	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
$t_{DH}$	Data-In Hold Time	20	-	20	-	25	-	ns	11
$t_{DHR}$	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
$t_{REF}$	Refresh Period	-	8	-	8	-	8	ms	
$t_{WS}$	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
$t_{CSR}$	$\overline{CS}$ Set-Up Time ( $\overline{CS}$ before $\overline{RAS}$ )	10	-	10	-	10	-	ns	
$t_{CHR}$	$\overline{CS}$ Hold Time ( $\overline{CS}$ before $\overline{RAS}$ )	30	-	30	-	30	-	ns	
$t_{RPC}$	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
$t_{CPT}$	$\overline{CS}$ Precharge Time ( $\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
$t_{CPN}$	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	

### CAPACITANCE ( $V_{CC}=5V\pm 10\%$ , $f=1MHz$ , $T_a=0\sim 70^\circ C$ )

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$C_{I1}$	Input Capacitance ( $A_0 \sim A_9, \overline{W}, \overline{CS}, \overline{RAS}$ )	-	60	pF
$C_{DQ}$	I/O Capacitance ( $DQ_0 \sim DQ_7$ )	-	15	pF

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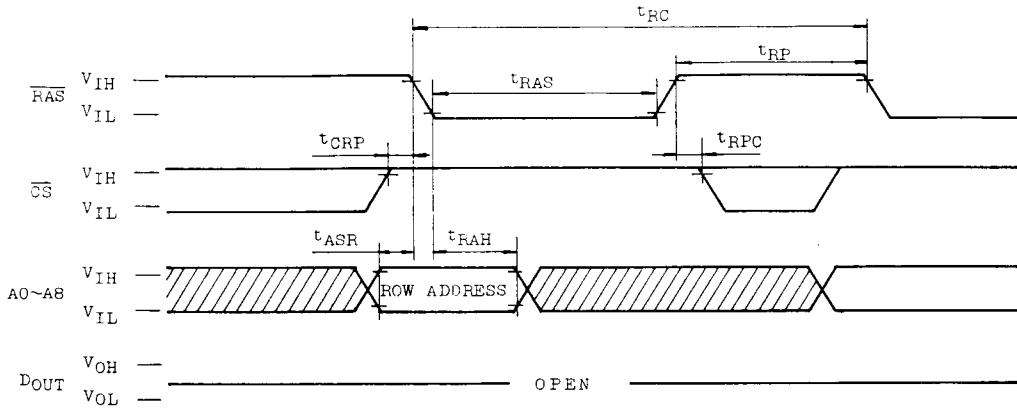
### NOTES:


1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ ,  $I_{CC6}$  depend on cycle rate.
4.  $I_{CC1}$ ,  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200 $\mu$ s is required after power-up followed by any 8  $\overline{RAS}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CS}$  before  $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
6. AC measurements assume  $t_T=5$ ns.
7.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
11. These parameters are referenced to  $\overline{CS}$  leading edge.
12.  $t_{WS}$ ,  $t_{WH}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WS} \geq t_{WS}(\text{min.})$  and  $t_{WH} \geq t_{WH}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles.
13. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
14. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled exclusively by  $t_{AA}$ .
15.  $t_{AH}$  is the condition to latch column address when  $\overline{RAS}$  has risen up.



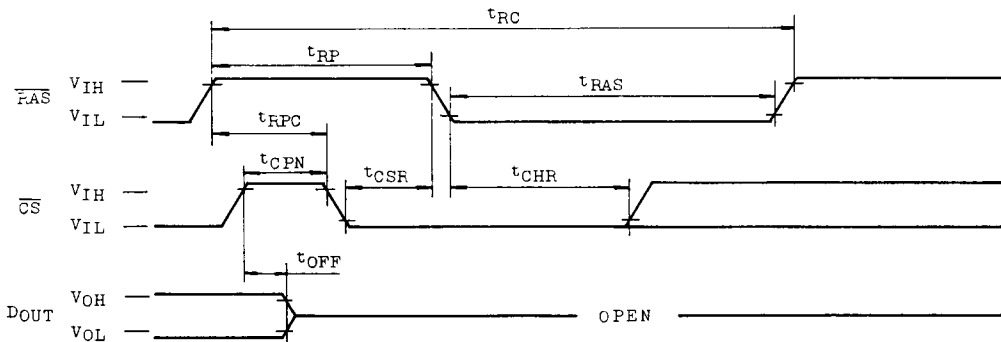


RAS ONLY REFRESH CYCLE



NOTE:  $\overline{\text{WRITE}} = \text{"H"}$  or  $\text{"L"}$ ,  $\text{A9} = \text{"H"}$  or  $\text{"L"}$   :  $\text{"H"}$  or  $\text{"L"}$

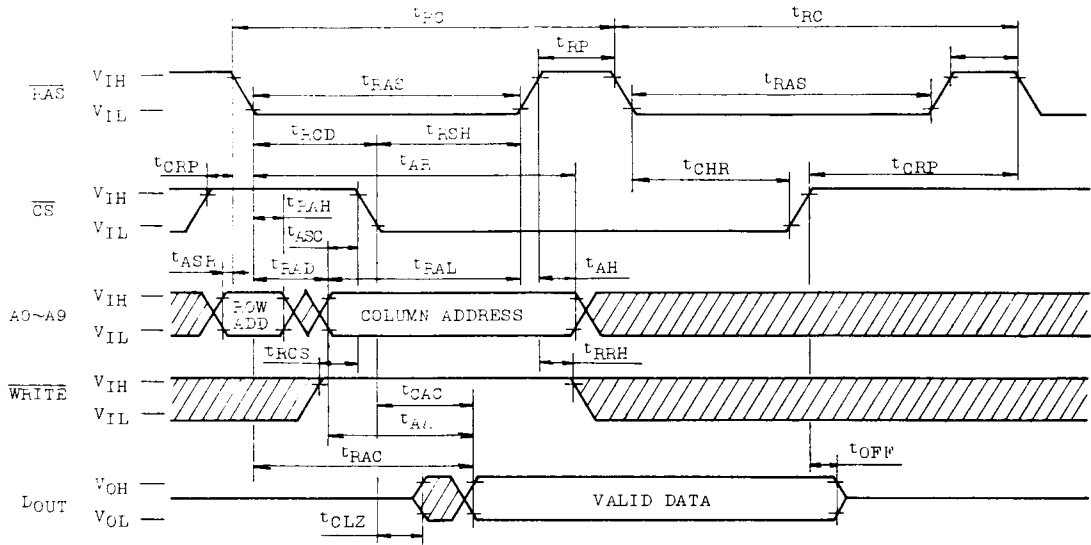
$\overline{\text{CS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH CYCLE



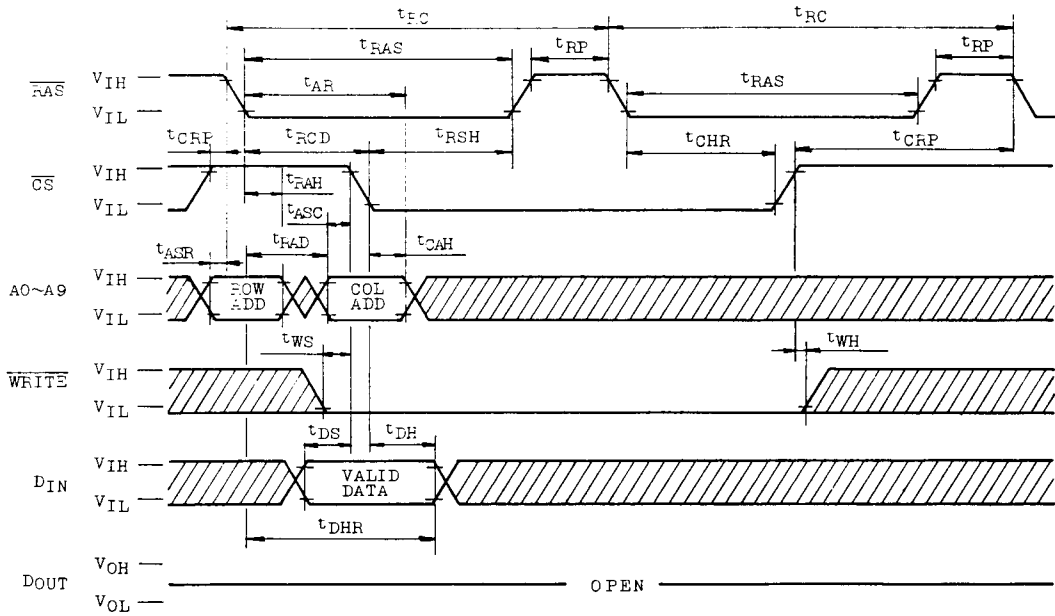
NOTE:  $\overline{\text{WRITE}} = \text{"H"}$  or  $\text{"L"}$ ,  $\text{A0} \sim \text{A9} = \text{"H"}$  or  $\text{"L"}$

# THM81002S/L-85, 10, 12

## HIDDEN REFRESH CYCLE (READ)



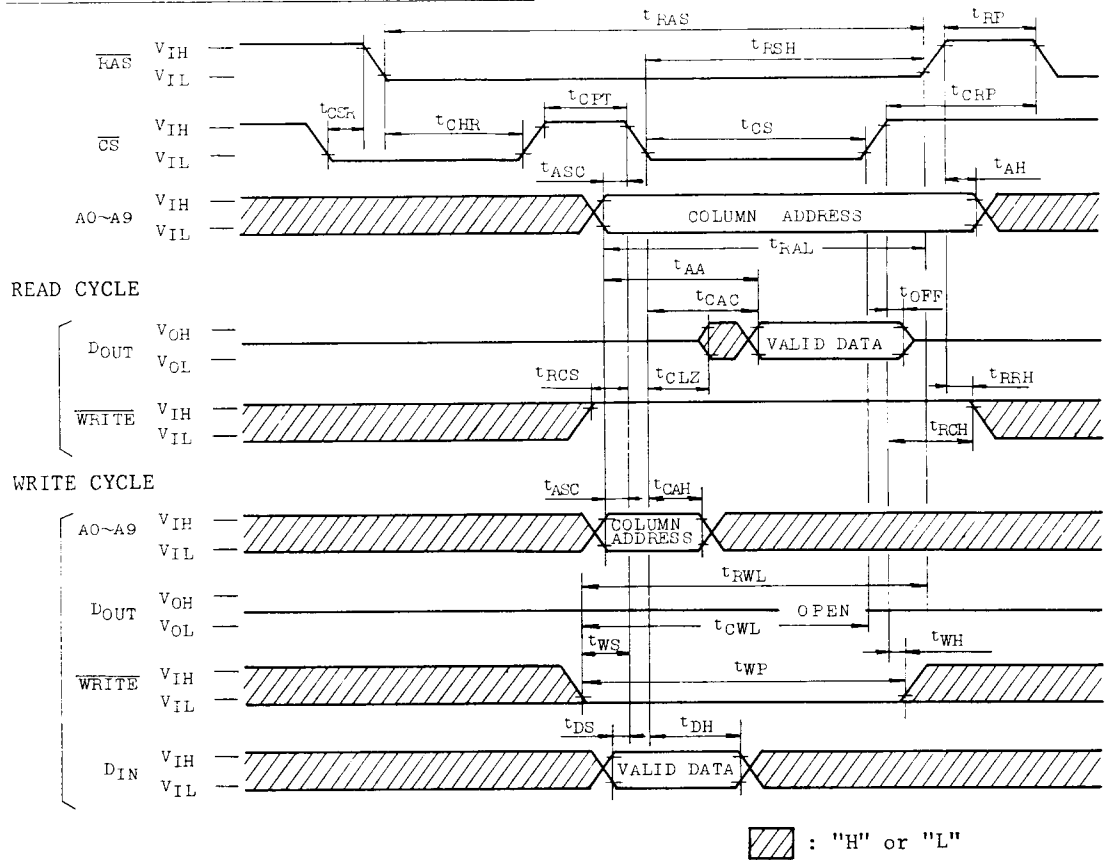
## HIDDEN REFRESH CYCLE (WRITE)



▨ : "H" or "L"

# THM81002S/L-85, 10, 12

CS BEFORE RAS REFRESH COUNTER TEST CYCLE

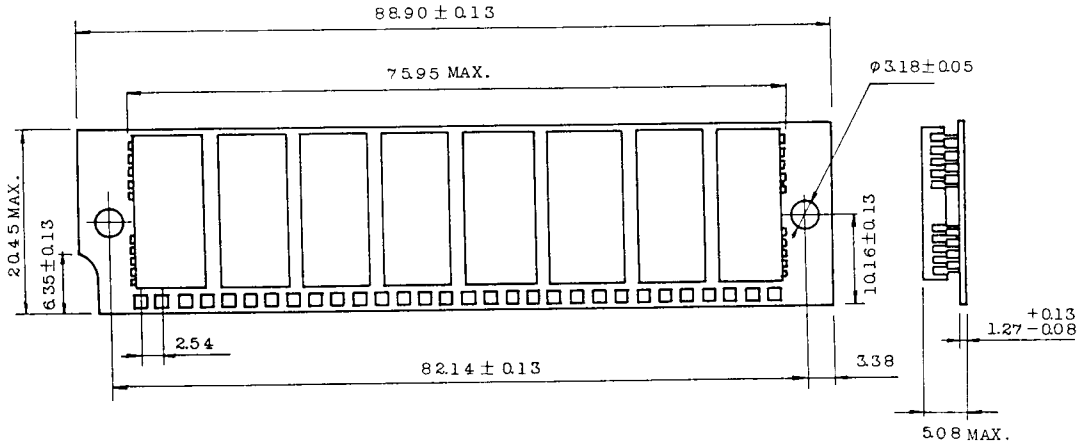


# THM81002S/L-85, 10, 12

## OUTLINE DRAWINGS

• THM81002S

Unit in mm



• THM81002L

