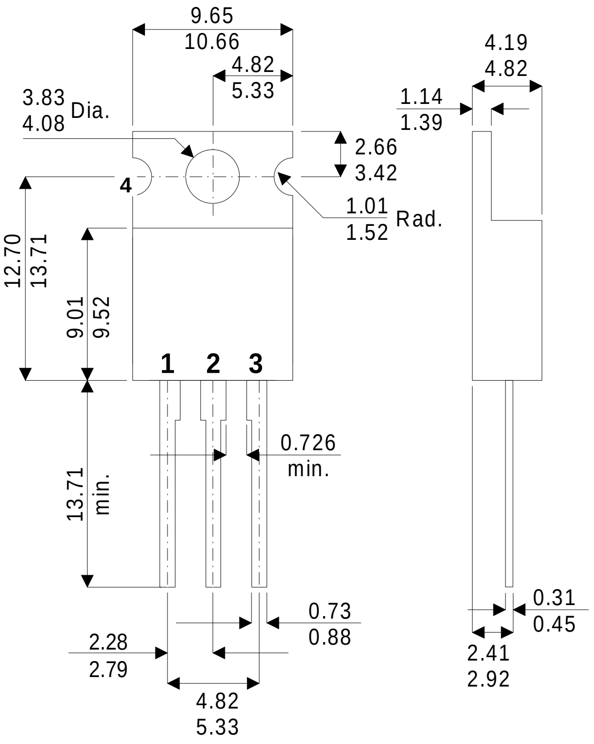
SEME
LAB

TetraFET

D1284UK

METAL GATE RF SILICON FET

MECHANICAL DATA
Dimensions in mm (inches)



TO–220 PLASTIC PACKAGE

PIN 1 – GATE	PIN 2 – DRAIN
PIN 3 – SOURCE	PIN 4 – DRAIN

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 4W – 12V – 200MHz SINGLE ENDED

FEATURES

- **SIMPLIFIED AMPLIFIER DESIGN**
- **SUITABLE FOR BROAD BAND APPLICATIONS**
- **LOW C_{rss}**
- **SIMPLE BIAS CIRCUITS**
- **LOW NOISE**
- **HIGH GAIN – 10dB MINIMUM**
- **SURFACE MOUNT**

APPLICATIONS

- LOW COST DC to 200 MHz

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise stated)

P_D	Power Dissipation	62.5W
BV_{DSS}	Drain – Source Breakdown Voltage	40V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	10A
T_{STG}	Storage Temperature	–65 to 125°C
T_J	Maximum Operating Junction Temperature	150°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ $I_D = 10mA$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 12.5V$ $V_{GS} = 0$			1	mA
I_{GSS}	Gate Leakage Current	$V_{GS} = 20V$ $V_{DS} = 0$			1	µA
$V_{GS(th)}$	Gate Threshold Voltage*	$I_D = 10mA$ $V_{DS} = V_{GS}$	1		7	V
g_{fs}	Forward Transconductance*	$V_{DS} = 10V$ $I_D = 1A$	0.8			S
G_{PS}	Common Source Power Gain	$V_{DS} = 12.5V$ $I_{DQ} = 0.2$ $P_O = 4W$ f = 200MHz	10			dB
η	Drain Efficiency		40			%
VSWR	Load Mismatch Tolerance		20:1			—
C_{iss}	Input Capacitance	$V_{DS} = 0V$ $V_{GS} = –5V$ f = 1MHz			60	pF
C_{oss}	Output Capacitance	$V_{DS} = 12.5V$ $V_{GS} = 0$ f = 1MHz			40	
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 12.5V$ $V_{GS} = 0$ f = 1MHz			4	

* Pulse Test: Pulse Duration = 300 µs , Duty Cycle ≤ 2%

THERMAL DATA

$R_{THj–case}$	Thermal Resistance Junction – Case	Max. 6°C / W