Speech Synthesizer (Voice ROM)

FEATURES

- Can synthesize human voices and most animal sounds.
- Direct current output combined with a single transistor can drive a speaker.
- Up to 20 seconds speech duration that can be separated into 64 sections for µp mode, 8 sections for SA (Standalone) mode.
- Duration of the 64 (8) sections can be different and determined by customer's voice content of each section, the total maximum duration is about 20 seconds.
- Mute is available for each section up to 48 seconds.
- Expandable, can extend the speech duration by 15 x n seconds with n pieces of MSS2001.
- Single power supply can operate at 2.4V through 6.0V.
- Automatic power down function: (selected by bonding option). Starts operating upon receiving a speech synthesis command, and powers down upon conclusion (unvoiced).

DESCRIPTION

The MSS2001 is a CMOS single-chip speech synthesizing ROM that can synthesize up to 20 seconds of voice using the PCM Quantified Coding method.
The chip contains most of the necessary circuit such as the Oscillator, ROM, D/A converter, sequence control logic and interface circuit for key switches and microcomputers. Application to widely used voice systems with minimum external parts is possible. Up to 64 sections of speech are available for µp mode, up to 8 sections are available for SA mode. Several chips can be combined to reach longer voice duration (longer than 20 seconds). Customer speech data is edited and programmed into ROM with a single mask during the device fabrication.

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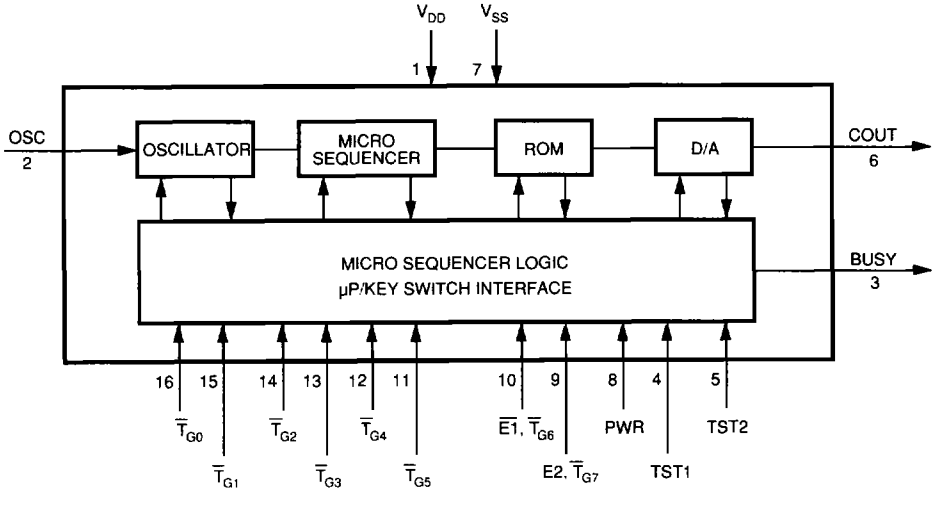
BLOCK DIAGRAM



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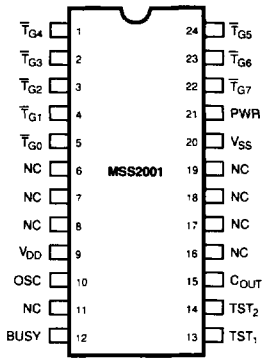
PID033

MSS2001

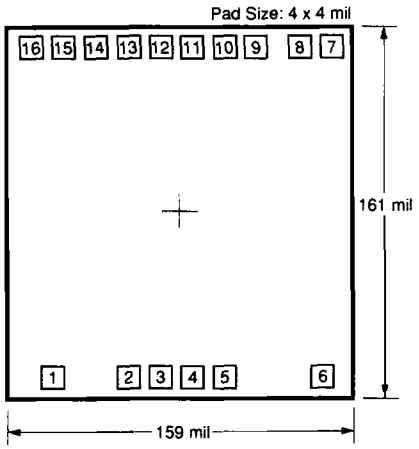
PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	V_{DD}	Positive power supply
2	OSC	Oscillator Input
3	BUSY	Busy signal output; active high
4	TST1	Test mode production test only
5	TST2	Test mode, production test only
6	C_{OUT}	Speech signal current outputs
7	V_{SS}	Negative power supply
8	P_{WR}	Active high for non-power down
9	E2, $\overline{T}_{G7}$	Enable 2; active high, Trigger 7; active low
10	$\overline{E1}$, $\overline{T}_{G6}$	Enable 1/Trigger 6; active low
11	$\overline{T}_{G5}$	Trigger/Address 5; active low
12	$\overline{T}_{G4}$	Trigger/Address 4; active low
13	$\overline{T}_{G3}$	Trigger/Address 3; active low
14	$\overline{T}_{G2}$	Trigger/Address 2; active low
15	$\overline{T}_{G1}$	Trigger/Address 1; active low
16	$\overline{T}_{G0}$	Trigger/Address 0; active low

PIN CONFIGURATION



BONDING DIAGRAM



PIN NO.	DESIGNATION	X	Y
1.	V_{DD}	−1778.3	−1701.6
2.	OSC	−455.3	−1764.5
3.	BUSY	−171.8	−1785.6
4.	TST_1	125.0	−1764.5
5.	TST_2	416.8	−1764.5
6.	COUT	1612.2	1762.9
7.	V_{SS}	1737.0	1762.9
8.	PWR	1442.2	1765.5
9.	$\overline{T}_{G7}$, E2	944.9	1765.5
10.	$\overline{T}_{G6}$, $\overline{E1}$	551.4	1765.6
11.	$\overline{T}_{G5}$	253.7	1764.7
12.	$\overline{T}_{G4}$	−188.2	764.6
13.	$\overline{T}_{G3}$	−486.0	765.5
14.	$\overline{T}_{G2}$	−927.9	1764.6
15.	$\overline{T}_{G1}$	−1225.7	1765.5
16.	$\overline{T}_{G0}$	−1627.2	1765.5

*Note: Substrate is V_{DD} Unit: µM

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	UNITS
V_{DD} - V_{SS}	−0.5 ~+0.7	V
V_{IN} ($\overline{T}_{G0}$ ~ $\overline{T}_{G7}$, P_{WR})	V_{SS}−0.3 < V_{IN} < V_{DD}+0.3	V
V_{OUT} (BUSY)	V_{SS} < V_{OUT} < V_{DD}	V
T(Operating)	−10 ~ +60	°C
T(Storage)	−55 ~ +125	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER NAME	PARAMETER		TEST CONDITIONS	MSS2001 MIN.	TYP.	MAX.	UNITS
V_{DD}	Operating Voltage			2.4	4.5	5	V
I_{SB}	Supply Current	Stand by	V_{DD} = 4.5, I/O Open	-	-	0.6	μA
I_{OP}		Operating		-	-	120	
V_{IH}	Input Voltage ($\overline{T}_{G0}$ ~ $\overline{T}_{G7}$, E1, E2, P_{WR})		V_{DD} = 4.5V	4	4.5	5	V
V_{IL}				−0.3	0	0.3	
I_{IL}	Input Current ($\overline{T}_{G0}$ ~ $\overline{T}_{G7}$)		V_{DD} = 4.5V	-	-	5	μA
I_{IH}				-	0	-	
I_{CO}	Output Current (C_{OUT})		V_{DD} = 4.5V	-	−1	-	mA
I_{IH}	Input Current for PWR		V_{DD} = 4.5V	-	-	10	μA
I_{IL}				-	0	-	
I_{OH}	Output Current (BUSY)		V_{DD} = 4.5V, $V_{O/P}$ = 4V	-	−1	-	mA
I_{OL}			V_{DD} = 4.5V, $V_{O/P}$ = 0.5V	-	1	-	
ΔF/F	Frequency Stability		F_{OSC}(4.5V)−F_{OSC}(4V) / F_{OSC}(4.5V)	-	-	5	%
ΔF/F	Frequency Variation		V_{DD} = 4.5V, R_{OSC} = 1.2MΩ	-	-	15	%

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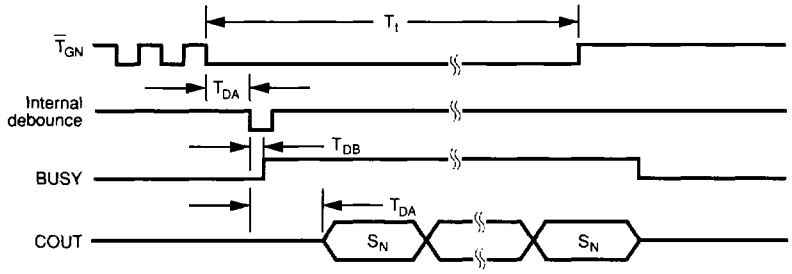
AC ELECTRICAL CHARACTERISTICS

STANDALONE MODE			
TIMING		**MIN.**	**MAX.**
T_T	Trigger pulse width	15ms	
T_{TD}	Trigger to Debounce delay time		10ms
T_{DB}	Debounce to BUSY delay time		200µs
T_{DA}	Debounce to Audio delay time		250µs
MICROPROCESSOR MODE			
TIMING		**MIN.**	**MAX.**
T_W	Write Enable pulse width	30ns	
T_H	Trigger address hold time	80ns	
T_{WB}	Write Enable to BUSY delay time		200µs
T_{WA}	Write Enable to Audio delay time		250µs

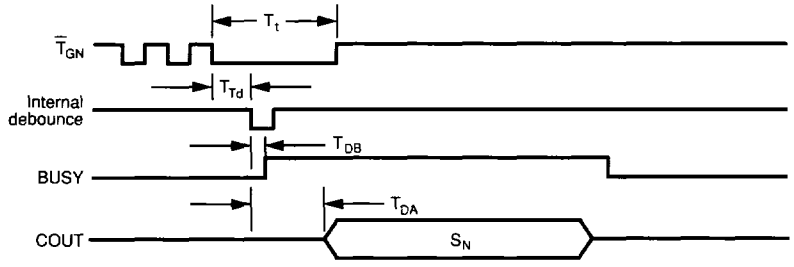
TIMING WAVEFORMS

I. Standalone-Level Mode

1. Level Trigger



2. Edge Trigger

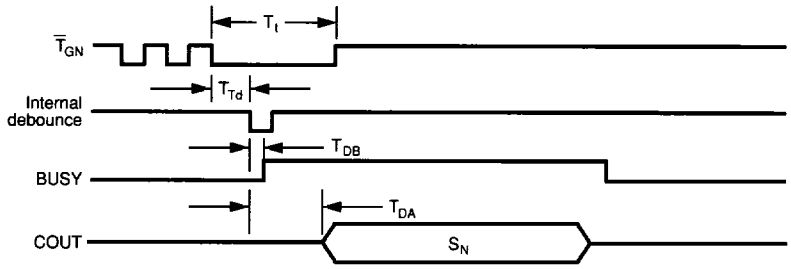


Notes:
1. $\overline{T}_{G0} \sim \overline{T}_{G7}$ are low active.
2. $\overline{T}_{G0} \sim \overline{T}_{G7}$ are internal pull high.

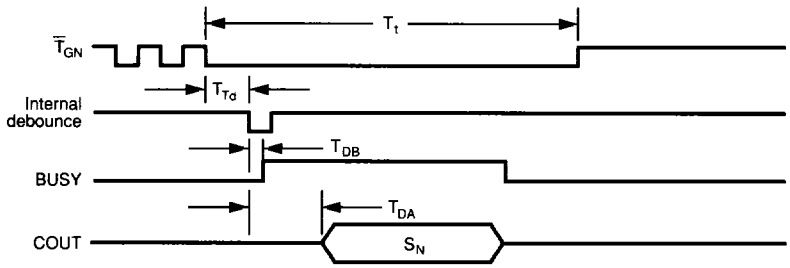
TIMING WAVEFORMS

II. Standalone-Edge Mode

1. Edge Trigger

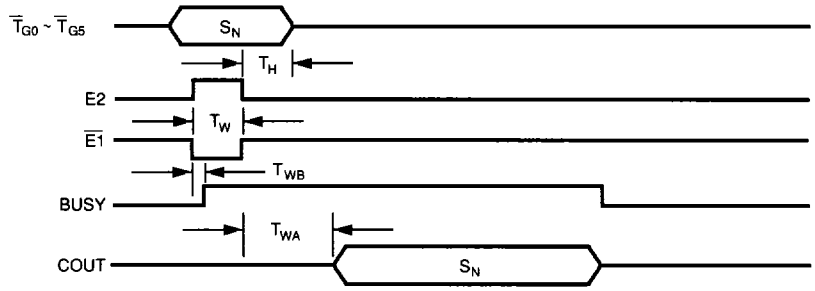


2. Level trigger



Note:
$\overline{T}_{G0}$ ~ $\overline{T}_{G7}$ are internal pull high.

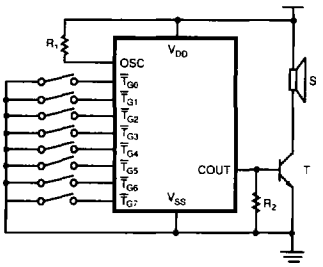
III. CPU Mode



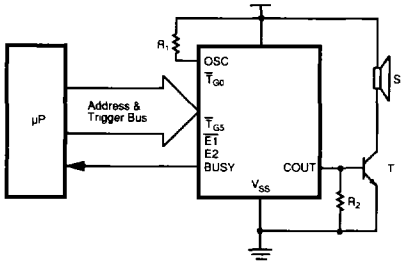
Notes:
1. $\overline{T}_{G0}$ ~ $\overline{T}_{G5}$ are used as address bus.
2. $\overline{E1}$, E2, are used as trigger input.
3. $\overline{T}_{G0}$ ~ $\overline{T}_{G5}$, $\overline{E1}$, E2, are internally pulled high.
4. Every retrigger action will reload address and play the speech from the beginning.
5. In CPU mode to avoid unwanted noise caused by abrupt change between different sections of voice messages, it is recommended to program PWR pin to high (V_{DD}) during voice processing.

APPLICATION CIRCUITS

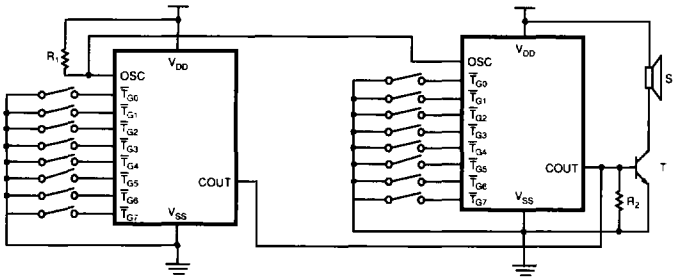
1. **Typical application**
   a. Standalone



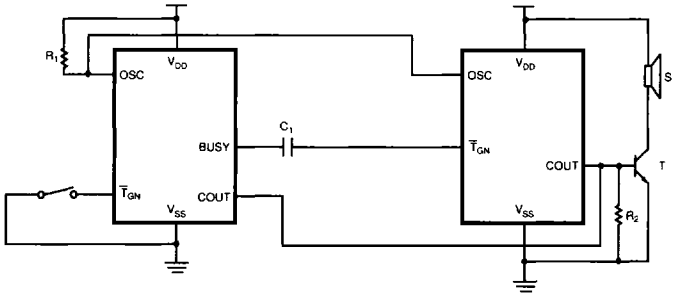
b. CPU Mode



2. **Parallel application**
   (Could extend up to desired number of voice sections in parallel arrangement)



3. **Cascade application**
   (Could extend to desired voice length in serial arrangement)



Notes:
a. R1 (resistor) = 1.2MΩ, R2 = 470Ω, T (transistor) = ß > 150, S (speaker) = 1/4W, 8Ω, C1 = 0.1μf; all typical.
b. Both cascade and parallel application can apply to CPU mode.