PBL 385 70
Universal Speech Circuit

Description.

PBL 38570 is a monolithic integrated speech transmission circuit for use in electronic telephones. It is designed to accomodate either a low impedance dynamic or an electret microphone. A separate input for DTMF dialling tones that is controlled by a mute signal, and a signal summing point at the transmitter input, are available.

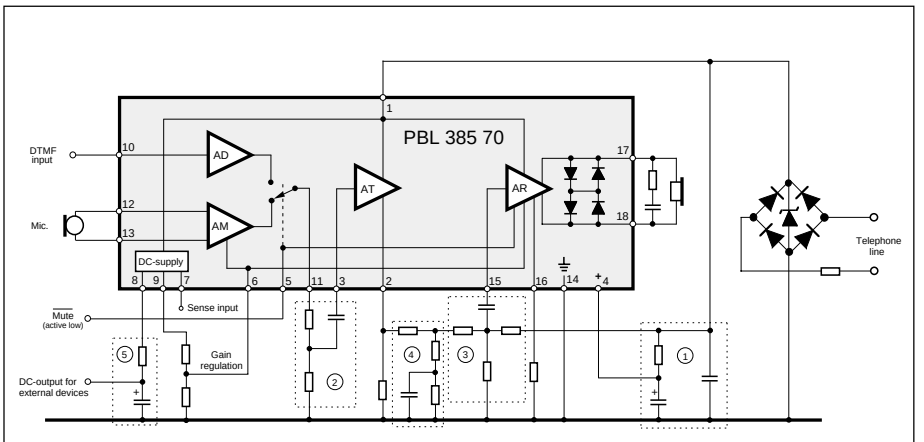
An internally preset line length compensation can be adjusted with external resistors to fit into different current feed systems as for ex. 48 V, 2 x 200 ohms, 48 V, 2 x 400 ohms and 48 V, 2 x 800 ohms. The line length compensation can be shut off in either high or low gain mode. Application dependent parameters such as line balance, side tone level, transmitter and receiver gains and frequency responces are set independently by external components which means an easy adaption to various market needs.

The setting of the parameters if carried out in certain order will counteract the interaction between the settings.

A number of different DC - supplies are provided to feed microphones and diallers.

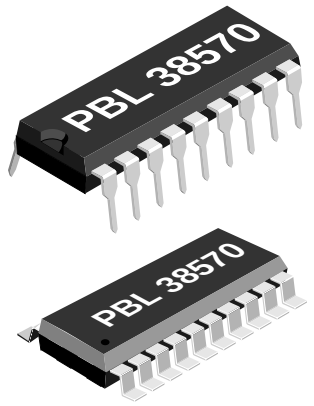
Key features.

- Minimum number of external components, 7 capacitors and 11 resistors.
- Easy adaption to various market needs.
- Mute control input for operation with DTMF - generator.
- A separate input for DTMF tones controlled by mute.
- Transmitter and receiver gain regulation for automatic loop loss compensation.
- Extended current and voltage range 5 - 130 mA, down to 2 V.
- Differential microphone input for good balance to ground.
- Balanced receiver output stage.
- Stabilized DC - supplies for low current CMOS diallers and electret microphones.
- 18 - pin DIP and 20 - pin SO packages.
- Short start up time.
- Excellent RFI performance.



1. Line impedance and radio interference suppression.
2. Transmit gain and frequency response network.
3. Receive gain and frequency response network.
4. Side tone balance network.
5. DC-supply components.

Figure 1. Functional diagram. DIP package.



20-pin plastic SO
18-pin plastic DIP

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Line voltage, t_p = 2 s	V_L	0	18	V
Line current, continuous DIP	I_L	0	130	mA
Line current, continuous SO package	I_L	0	100	mA
Operating temperature range	T_{Amb}	-40	+70	°C
Storage temperature range	T_{Stg}	-55	+125	°C

No input should be set on higher level than pin 4 (+C).

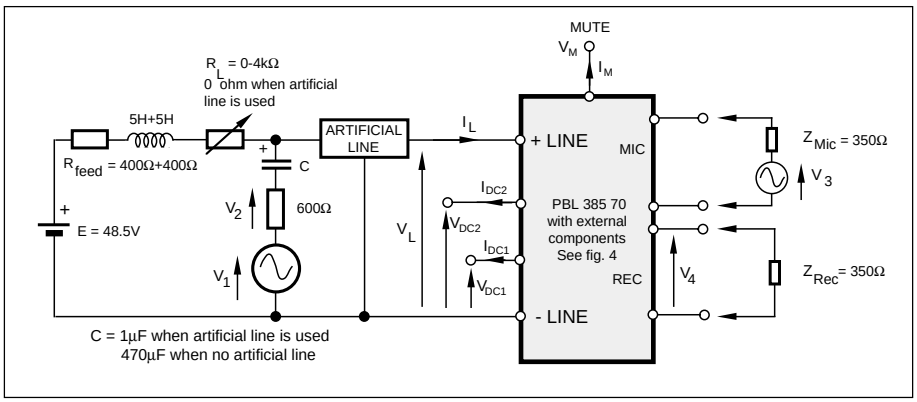


Figure 2. Test set up without rectifier bridge.

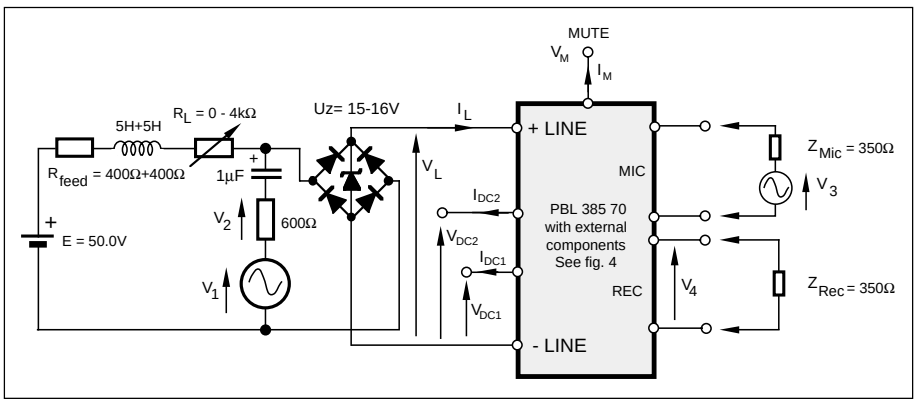


Figure 3. Test set up with rectifier bridge.

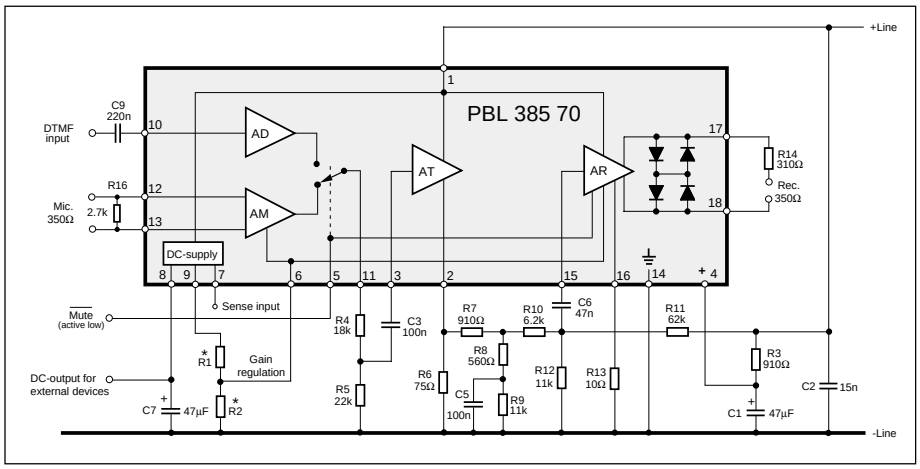


Figure 4. Circuit with external components for test set up.
* Not used in test set up.
18 pin DIP package.

Electrical Characteristics

At T_{Amb} = + 25° C. No cable and line rectifier unless otherwise specified.

Parameter	Ref. fig.	Conditions	Min	Typ	Max	Unit
Line voltage, V_L	2	I_L = 15 mA	3.3	3.7	4.1	V
	2	I_L = 100 mA	11	13	15	V
Transmitting gain, note 1		20 •[10] log (V_2 / V_3); 1 kHz				
	2	R_L = 0	41	43	45	dB
	2	R_L = 400 Ω	43.5	45.5	47.5	dB
	2	R_L = 900 Ω - 2.2 kΩ	46	48	50	dB
Transmitting range of regulation	2	1 kHz, R_L = 0 to 900 Ω	3	5	7	dB
Transmitting frequency response	2	200 Hz to 3.4 kHz	-1		1	dB
Transmitter input impedance pin 3	2	1 kHz	13.5	17	20.5	kΩ
Transmitter dynamic output	2	200 Hz - 3.4 kHz ≤ 2% distortion, I_L = 20 - 100 mA		1.5		V_p
Transmitter max output	2	200 Hz - 3.4 kHz I_L = 0 - 100 mA, V_3 = 0 - 1 V		3		V_p
Transmitter output noise	2	Psoph-weighting, Rel 1 V_{rms}, R_L = 0		-75		dB_{Psoph}
Microphone input impedance pin 12 (14),13 (15)	2	1 kHz		1.7(//2.7) note 3		kΩ
Receiving gain, note 1		20 • [10] log (V_4 / V_1); 1 kHz				
	2	R_L = 0 Ω	-18.5	-16.5	-14.5	dB
	2	R_L = 400 Ω	-16	-14	-12	dB
	2	R_L = 900 Ω - 2.2 kΩ	-13.5	-11.5	-9.5	dB
Receiving range of regulation	2	1 kHz, R_L = 0 to 900 Ω	3	5	7	dB
Receiving frequency response	2	200 Hz to 3.4 kHz	-1		1	dB
Receiver input impedance	2	1kHz	30.4	38	45.6	kΩ
Receiver output impedance	2	1 kHz,		3(+310), note 3		Ω
Receiver dynamic output note 2	2	200 Hz - 3.4 kHz ≤ 2% distortion, I_L = 20 - 100 mA		0.5		V_p
Receiver max output	3	Measured with line rectifier 200 Hz - 3.4 kHz, I_L = 0 - 100 mA, V_1= 0 - 50 V		0.9		V_p
Receiver output noise	2	A-weighting, Rel 1V_{rms}, with cable 0 - 5 km, Ø = 0.5 mm, 0 - 3 km, Ø = 0.4 mm		-85		dB_A
Mute input voltage at mute (active low)	2				0.3	V
DC-supply voltage	2	I_L = 20 - 100 mA				
		I_{DC} = 0 mA	2.1	2.35	2.6	V
		I_{DC} = 2 mA	1.95	2.2	2.6	V
DC-supply current, pin 8.	2		2			mA
DC-output pin 8 input leakage current (no supply)	4	V_{DC} = 2.35 V		0.1		µA
DTMF transmitting gain	2	V_M = 0.3 V, 1 kHz	24.5	26.5	28.5	dB
DTMF input impedance	2	1 kHz	20	25	30	kΩ

Notes

1. Adjustable to both higher and lower values with external components.
2. The dynamic output can be doubled, see applications information.
3. External resistor in the test set up.

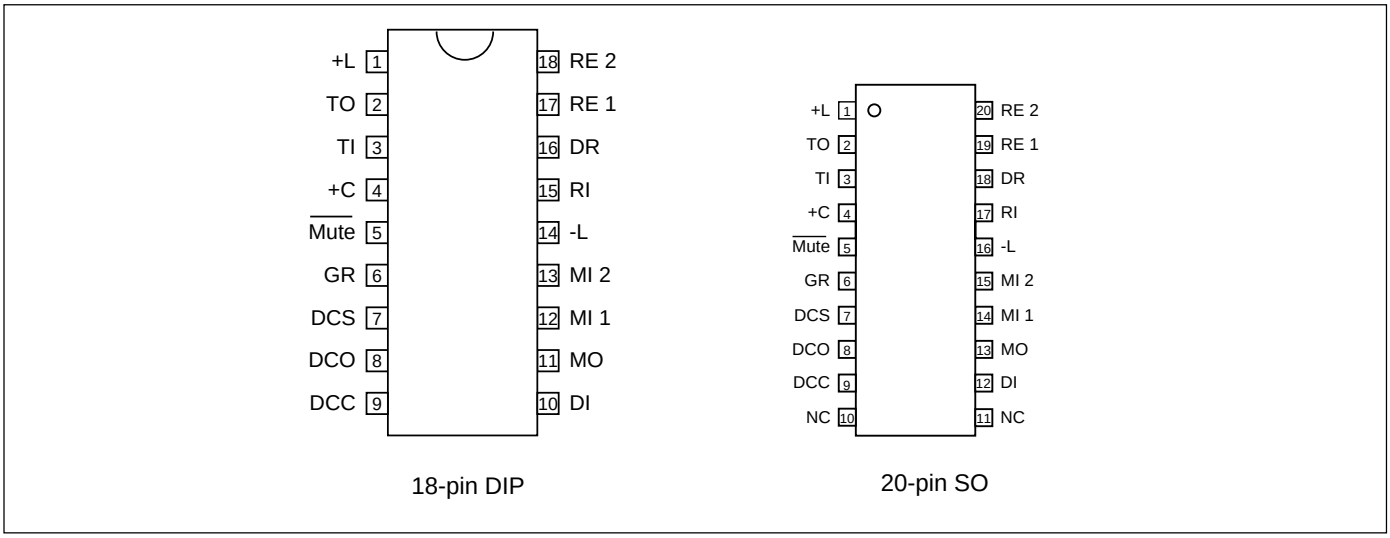


Figure 5. Pin configuration.

Pin Descriptions

Refer to figure 5.

DIP	SO	Name	Function
1	1	+L	Output of the DC-regulator and transmit amplifier, connected to the line through a polarity guard diode bridge.
2	2	TO	Output of the transmit amplifier, connected through a resistor of 47 to 100 ohm to -L, sets the DC-characteristics of the circuit. The output has a low AC output impedance and the signal is used to drive a side tone balancing network.
3	3	TI	Input of transmit amplifier. Input impedance 17 kohm ± 20 %.
4	4	+C	Positive power supply terminal for most of the circuitry inside the PBL 385 70 (about 1 mA current consumption). The +C pin must be connected to a decoupling capacitor of 47 µF to 150 µF.
5	5	$\overline{\text{Mute}}$	When low, speech circuit is muted and the DTMF input is enabled. Maximum voltage (at mute) is 0.3 V, current sink requirement of external driver is min. 50 µA.
6	6	GR	Control input for the gain regulation circuitry.
7	7	DCS	Sense input to the DC-supply.
8	8	DC1	Output from the DC-supply.
9	9	DC2	Control of the DC-supply.
10	12	DI	Input for the DTMF-signal. Input impedance is 25 kohm ± 20 %.
11	13	MO	Output of the microphone amplifier or DTMF-amplifier.
12	14	MI 1	Inputs to the microphone amplifier. Input impedance 1.7 kohm ± 20 %.
13	15	MI 2	
14	16	-L	The negative power terminal, connected to the line through a polarity guard diode bridge.
15	17	RI	Input of receiver amplifier. Input impedance is 38 kohm ± 20 %.
16	18	DR	Control input for the receiver amplifier driving capacity.
17	19	RE 1	Receiver amplifier outputs. Output impedance is approximately 3 ohm.
18	20	RE 2	
	10		NC
	11		NC

Functional description

Design procedure; ref. to fig.4.

The design is made easier through that all settable parameters are returned to ground (-line) this feature differs it from bridge type solutions. To set the parameters in the following order will result in that the interaction between the same is minimized.

1. Set the circuit impedance to the line, either 600Ω or complex. (R3 and C1). C1 should be big enough to give low impedance compared with R3 in the telephone speech frequency band. Too large C1 will make the start-up slow. See fig. 6.
2. Set the DC-characteristic that is required in the PTT specification or in case of a system telephone in the PBX specification (R6). There are also internal circuit dependent requirements like supply voltages etc.
3. Set the attac point where the line length regulation is supposed to cut in (R1 and R2). Note that in some countries the line length regulation is not allowed. In most cases the endresult is better and more readily achieved by using the line length regulation (line loss compensation) than without. See fig. 12.
4. Set the transmitter gain and frequency response.
5. Set the receiver gain and frequency response. See text how to limit the max. swing to the earphone.
6. Adjust the side tone balancing network.
7. Set the RFI suppression components in case necessary. In two piece telephones the often ”helically” wound cord acts as an aerial. The microphone input with its high gain is especially sensitive.
8. Circuit protection. Apart from any other protection devices used in the design a good practice is to connect a 15V 1W zener diode across the circuit , from pin 1 to -Line.

Impedance to the line

The AC- impedance to the line is set by R3, C1 and C2. Fig.4. The circuits relatively high parallel impedance will not influence it to any noticeable extent. At low frequencies the influence of C1 can not be neglected. Series resistance of C1 that is dependent on temperature and quality will cause some of the line signal to enter pin 4. This generates a closed loop in the transmitter amplifier that will create an active impedance thus lowering the impedance to the line. The impedance at high frequencies is set by C2 that also acts as a RFI suppressor.

In many specifications the impedance towards the line is specified as a complex network. See fig. 6. In case a). the error signal entering pin 4 is set by the ratio ≈Rs/R19 (909Ω), where in case b). the ratio at high frequencies will be Rs/220Ω because the 820Ω resistor is bypassed by a capacitor. To help up this situation the complex network capacitor is connected directly to ground (-line), case c). making the ratio Rs/220Ω+820Ω and thus lessening the error signal. Conclusion: Connect like in case c) when complex impedance is specified.

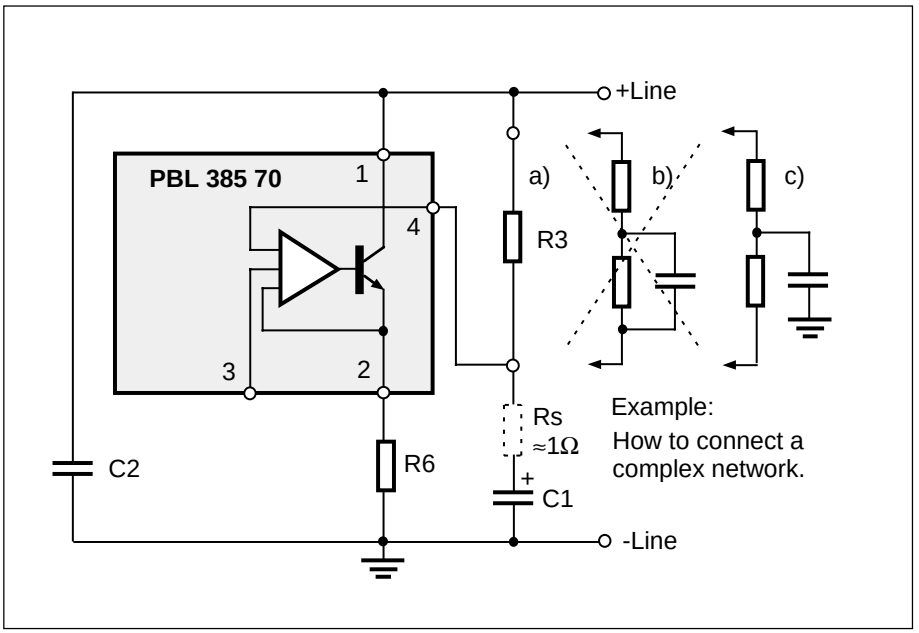


Figure 6. AC-impedence

DC - characteristic

The DC - characteristic that a telephone set has to fulfill is mainly given by the network administrator.Following parameters are useful to know when the DC behaviour of the telephone is to be set:

The voltage of the feeding system.

The line feeding resistance 2x... ohms.

The maximum current from the line at zero line length.

The min. current at which the telephone has to work (basic function).

The lowest and highest voltage permissible across the telephone set.

The highest voltage that the telephone may have at different line currents is normally set by the network owners specification. The lowest voltage for the telephone is normally set by the voltages that are needed for the different parts of the telephone to function. For ex. for transmitter output amplifier, receiver output amplifier, dialler, speech switching and loudspeaker amplifier in a handsfree telephone etc.

R6 will set the slope of the DC-char. and the rest of the level is set by some constants in the circuit as shown in the equation below. The slope of the DC-char. will also influence the line length regulation (when used) and thus the gain of both transmitter and receiver. See the table under gain regulation.

$$V_{Line} \approx 2 + 15 \cdot R6 \cdot I_{line}$$

$$V_{telephoneline} \approx 15V + V_{line}$$

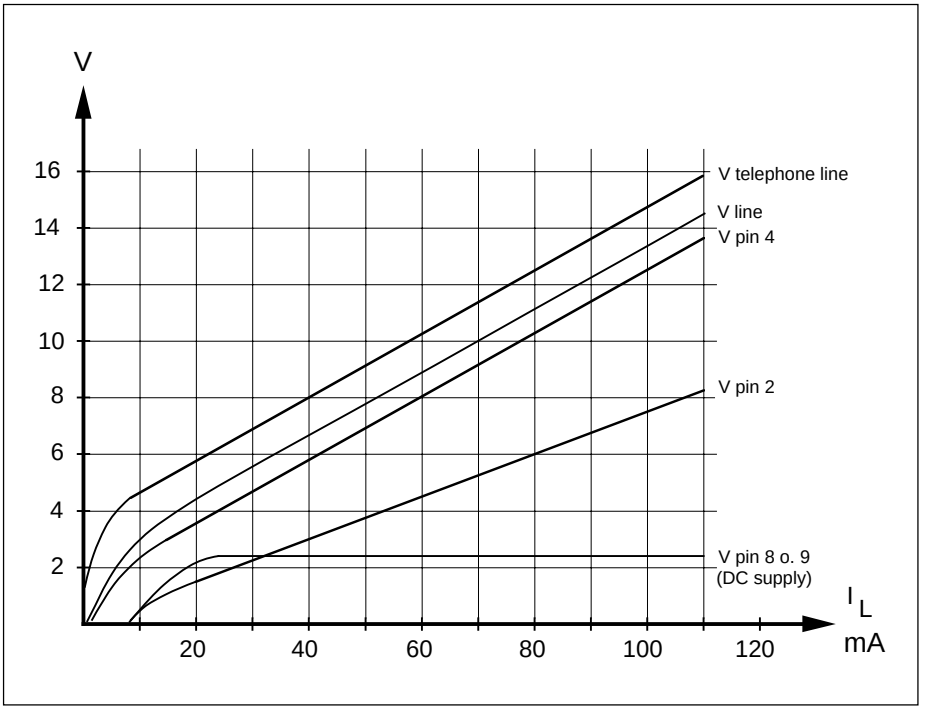


Figure 7. DC-characteristics. (R6 = 75Ω)

Microphone amplifier

The microphone amplifier in PBL38570 is divided into two stages. The first stage is a true differential amplifier providing high CMRR (-55 to -65 dB typical) with voltage gain of 19 dB. This stage is followed by a gain regulated amplifier with a regulation range of 5 ± 2 dB. The input of the microphone amplifier can be used for dynamic or electret transducers.
See fig. 8.

An electret microphone with a built in FET amplifier is to be seen from outside as a high impedance constant current generator and is normally specified with a load resistance of ≈ 2k. This is to be considered as max. value and by using it will render the max. gain from the microphone. This level of input signal that is unnecessary high will result in clipping in the microphone amplifier and could in mute condition permeate through the input to the circuits reference

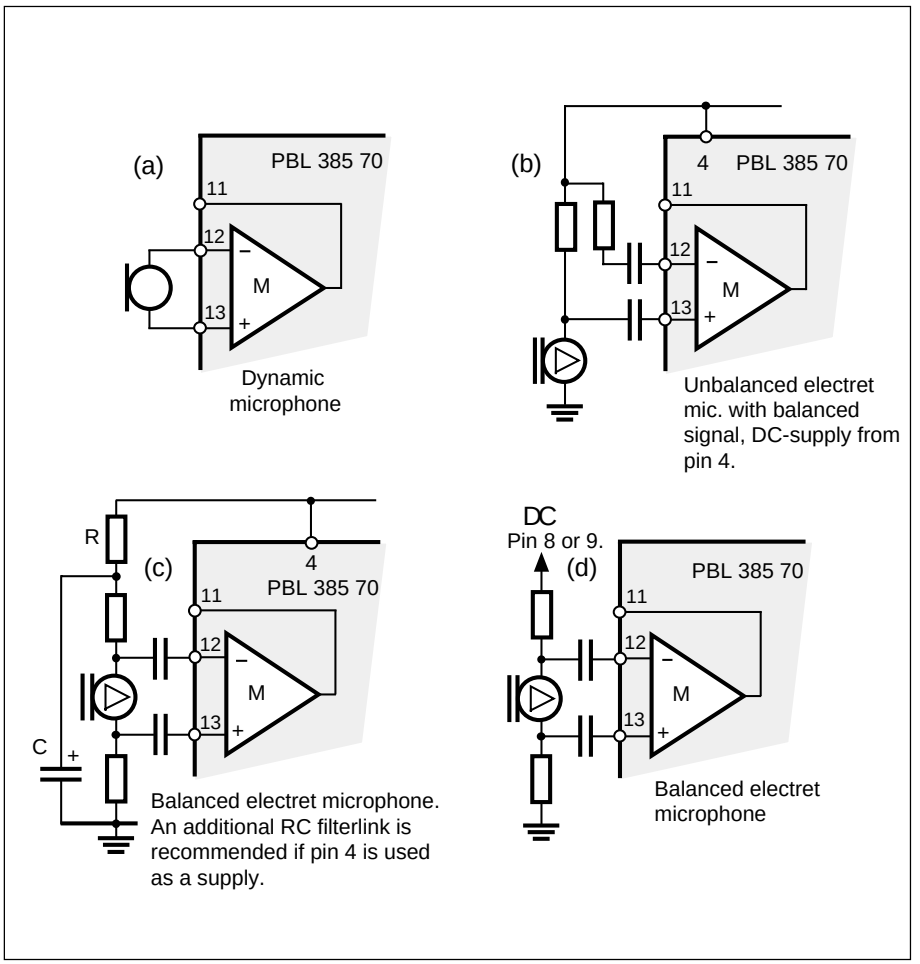


Figure 8. Microphone options.

and this way to all functions, resulting among other things in a bad mute. Hence it is better regarding noise perfomance and mute to rather use the gain of the microphone amplifier than the gain of the microphone itself (in case of electret) flat out. A more suitable level of gain from the microphone is achieved by using a load resistance of 330 - 820Ω. A low microphone impedance will also improve RFI suppression. Gain setting to the line is done at the input of the transmitter. The microphone amplifier has its own temperature stable reference to prevent overhearing to other parts and functions on the chip.

It is possible to use the microphone amplifier as a limiter (added to the limiter in the transmitter output stage) of the transmitted signal. See fig. 9. The positive output swing is then limited by the peak output current of the microphone amplifier. The negative swing is limited by the saturation voltage of the output amplifier. The output of the amplifier is DC-vice at internal reference level (1.2V). The lowest negative level for the signal is reference minus one diode and sat. transistor drop. (1.2-0.6-0.1 = 0.5V) The correct clipping level is found by determining the composite AC- and DC-load that gives a maximum symmetrical unclipped signal at the output. This signal is then fed into the transmitter amplifier at a level that renders a symmetrical signal clipping on the line. (adjust with ratio R4,R5) The total transmitter gain when an electret microphone is used can then be adjusted with the load resistor of the electret microphones buffer amplifier.

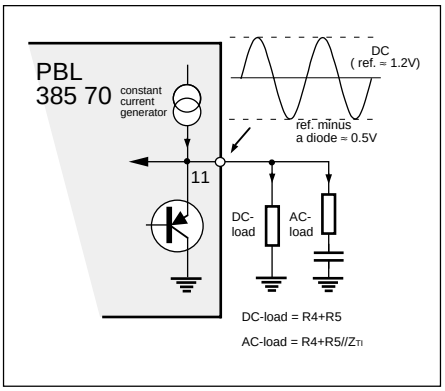


Figure 9. Micophone amplifier output clipping.

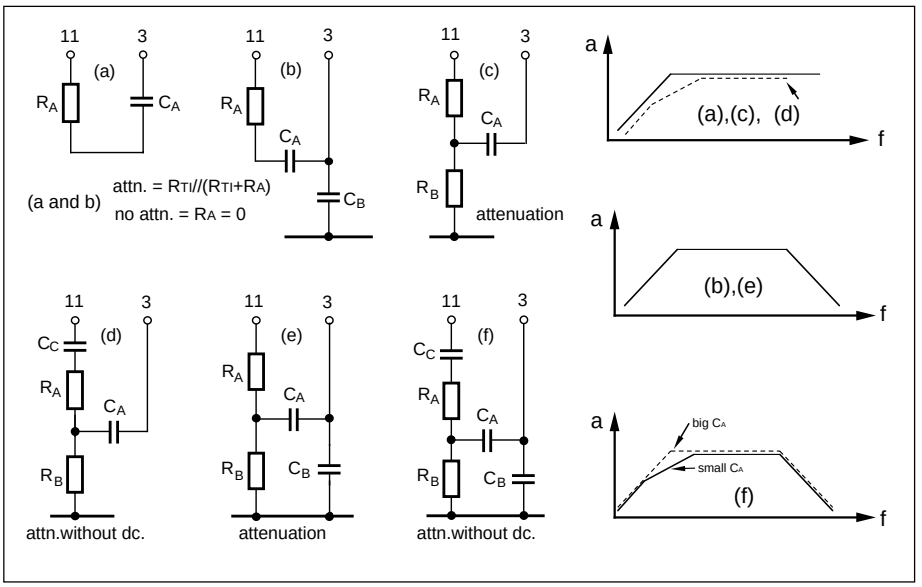


Figure 10. Network and frequency plots between microphone amplifier and transmitter.

Transmitter amplifier

The transmitter amplifier in PBL38570 consists of three stages. The first stage is an amplitude limiter for the input signal at TI, in order to prevent the transmitted signal to exceed a certain set level and cause distortion. The second stage amplifies further the signal from the first and adds it to a DC level from an internal DC-regulation loop in order to give the required DC characteristic to the telephone set. The output of this stage is TO. The third stage is a current generator that presents a high impedance towards the line and has its gain from TO to +L. The gain of this amplifier is ZL/R6 where ZL is the impedance across the telephone line. Hence, the absolute maximum signal

How to calculate the gains in the transmitter channel.
See fig. 2 and 4.
Microphone amplifiers first stage 19 dB.
Microphone amplifiers regulated second stage 10.5 dB - 15.5 dB
Regulation interval 10.5 - 15.5 dB low gain 19.0 + 10.5 dB = 29.5 dB
high gain 19.0 + 15.5 dB = 34.5 dB

$$\frac{V_2}{V_3} = \frac{R_M}{Z_{mic} + R_M} \cdot G_M \cdot \frac{R_5}{R_4 + R_5} \cdot G_{TX} \cdot \frac{R_{load}}{R_6}$$

RM = Microphone amplifier input resistance
$R_{load} = R_{line} // R_{telephone}$

ex. calculate the gain of the transmitter stage GTX at 0 - line length:

$$43 = 20\log\left(\frac{(1.7 // 2.7)k}{350\Omega + (1.7 // 2.7)k}\right) + 29.5 + 20\log\left(\frac{(17 // 22)k}{18k + (17 // 22)k}\right)$$
$$+ G_{TX} + 20\log\left(\frac{600\Omega // 910\Omega}{75\Omega}\right)$$

$$43 = -2.51 + 29.5 - 9.17 + G_{TX} + 13.66$$
$$G_{TX} = 11.52\,dB$$

amplitude that can be transmitted to the line undistorted is dependent of R6. (amplitude limiting).

The transmitter gain and frequency response are set by the RC-network between the pins 11 and 3. See fig.10. The capacitor for cutting the high end of frequency band is best to be placed directly at the microphone where it also will act as a RFI suppressor. The input signal source impedance to the transmitter amplifier input TI should be reasonably low in order to keep the gain spread down, saying that R4//R5 (see fig. 4) must be at least a factor 5 lower than the ZTin. Observe that the capacitor C1 should have a reasonably good temperature behaviour in order to keep the impedance rather constant. The V+C´s influence on the transmitter DC-characteristic is shown in the fig.7 (DC-characteristic), therefore the transmitter gain would change if the transmitted signal gives reason to an ac-voltage leak signal across C1 since this is a feedback point. If the transmitter has an unacceptable low sving to the line at low line currents $<\approx$10mA the first step should be to examine if the circuits DC characteristic can be adjusted upwards.

Receiver amplifier

The receiver amplifier consists of three stages, the first stage being an input buffer that renders the input a high impedance. The second stage is a gain regulated differential amplifier and the third stage a balanced power amplifier. The power amplifier has a differential output with low DC- offset voltage, therefore a series capacitor with the load is normally not necessary. The receiver amplifier uses at max. swing 4-6 mA peak. This current is drawn from the +Line. The gain and frequency response is set at the input RI with a RC-network. The receiver gain can be regulated. The range of regulation from the input to the output is 5 ± 2 dB (19 to 24dB). The driving capacity of the power stage can be optimized by a resistor on pin16, an other method is to connect a resistor series in with the earphone itself. The balanced earphone amplifier can not be loaded to full (both current and signal level) single ended.The signal would be distorded when returned to ground. A methode is shown in fig.11d. how to connect a light load (5k ac. or DC wise) to the output. It is preferred that both outputs are loaded the same. The receiver has, as a principal protection, two series diodes anti

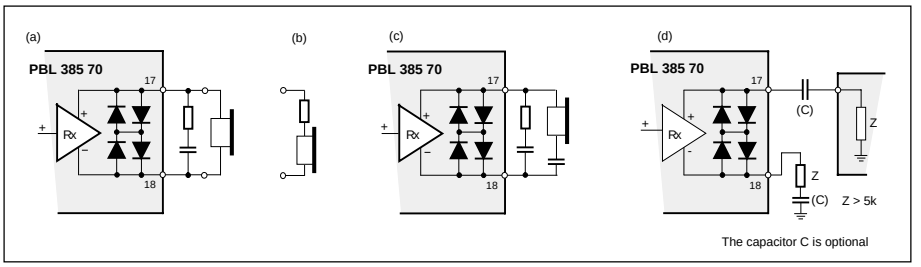


Figure 11. Receiver arrangements.

parallel across its output to limit the signal to the earphone and thus preventing an acoustical shock. A resistor in series with the output can very well be used to increase the protection level. Note, that the noise in the receiver is allways transmitter noise that has been more or less well balanced out by the side tone network.

The RC - network (optional) at the output is to stabilize against the inductive load that an earphone represents.

Gain regulation.

Both the receiver and transmitter are gain regulated (line loss compensated).

There is a fixed default compensation on the chip that can be adjusted or or set to constant high or low gain mode. The input impedance at the gain regulation pin 6 is 5.5k $\pm$ 20%. The default regulation pattern is valid when the input is left open. Fig. 12 shows a typical transmitter or receiver gain pattern versus line length. The following will show, what to alter, to change the look of the curve.

a). Adjustable with the divider R4,R5 for the transmitter and with R12 for the receiver.

b). The attack point of the regulator is adjusted with the divider R1,R2 to either direction , up or down ,on the line current axis.

c). The angle of elevation of the curve is mainly set by the value of R6. If the DC-characteristics is set according to the line parameters and a correct value for R6 is chosen the angle is mostly correct but it can be adjusted with R6. The adjustement will affect the DC-characteristics aswell as most of the other parameters. This is why the DC-characteristic is set early in the design phase.

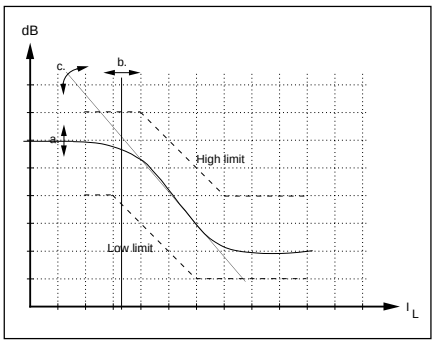


Figure 12. Gain regulation principle.

Battery feed	R1	R2	R6
Regulation:			
$48\,V, 2 \cdot 200\Omega$	∞	∞	47Ω
$48\,V, 2 \cdot 400\Omega$	∞	∞	75Ω
$48\,V, 2 \cdot 800\Omega$	∞	$180k$	100Ω
No regulation:			
Set for low gain			
All feedings	∞	22k	47 - 100Ω
Set for high gain	18k	∞	47Ω
Set for high gain	22k	∞	75 - 100Ω

What is balancing the side tone ?

- To understand that side tone balancing is to counteract the signal, that is transmitted via the microphone and transmitter to the line, returning to the earphone via the receiver.
- That presence of a strong side tone signal is disturbing in a way that one quite instictively lowers ones own voice level thus lowering the signal level for the other party. But again, if the balance is too good (seldom the case) the earphone will feel ”dead”. In practical terms what is expected is the same amplitude of ones own voice in the ear as when not talking in a telephone. The need to lower the side tone level where no balancing has been done is in the order of 6 - 12 dB.
- To understand that the side tone is influenced by other factors like, the impedance of the line and the signal that enters the ear acoustically directly from the mouth and from the mouth through the material in the handset. The signal that enters the microphone from the earphone acoustically will also influence the return loss factor to the telephone line.
- To understand that the side tone network can be trimmed to form a veritable ”distortion analyser”, so that the distortion that is present from the microphone, will be the only signal entering the earphone and this signal even being small will sound very bad. It is better to induce some of the fundamental frequency back by making the balance less perfect at that frequency. This is valid for a network that is trimmed to only one frequency. It is to strive to trim the network such that it will attenuate the fundamental and the harmonic frequencies alike throughout the different line combinations.
- To understand that if one of the two signals entering the balancing system from either direction, direct from microphone or via the line is clipped, will result in a very distorted signal entering the receiver amplifier and thus the earphone. Further , to remember that side tone is a small signal that is the difference of two large signals and that the amplitude of the distortion can be up to ten times the amplitude of the fundamental frequency.

A short guidance for understanding the side tone principle

(See fig.13.)

Assuming the line impedance to be 600Ω. (theorethical value)

Z1 = Line impedance

Z2 = The telephone set impedance 600Ω

Z1//Z2 = 300Ω

R6 will have a certain value 39 - 100Ω to give the telephone a specified DC-characteristic and overcurrent protection.

Assuming that this DC-characteristic requires R6=60Ω, hence it will be 1/5 of the Z1//Z2. This will in transmitting mode result that 1/5 of the ac-signal that is on the line appear across R6. Note that the signals at points a. and b. are 180 degrees off phase.

10 x R6 ≈ R7 + Zbal Note #1

R7 ≈ Zbal Note#2

The ac-signal at point c. is now 1/10 of the signal on the line because it is further divided by two from point b. (R7≈Zbal).

Hence 10 x R10 ≈ R11 to satisfy the balancing criteria. R12 is to set the receiver gain (can also be a volume control potentiometer).

Note #1 These values ensure that the frequency behaviour of the transmitter is not influenced. With the ratio 1/10 the influence is 1 dB, and with ratio 1/20 it´s 0.5 dB.

Note #2 If the R7 is made low ohmic compared with Zbal, it will load the latter and result in a bad side tone perfomannce, again if the R7 is made high ohmic compared with Zbal will result in a low signal to balance the side tone with and make the balancing difficult.

Making any of the impedances unnecessary high will make the circuit sensitive to RFI. All values given here are approximate and serve as starting entities only. The final trimming of side tone network is a cut and try proposition because a part of the balance lies in the acoustical path between the microphone and earphone.

Reverse side tone network.

This type of side tone balancing will help when of some reason there is a need to make the R6 low < 47Ω and thus the signal for balancing gets small across R6. By placing the balancing network like shown in fig.14. the possible signal level is 6 dB higher than in the first case and it will also help in case that a volume control is added to the receiver.

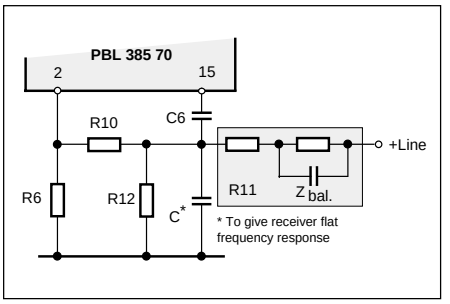


Figure 14. Sidetone network with complex R11.

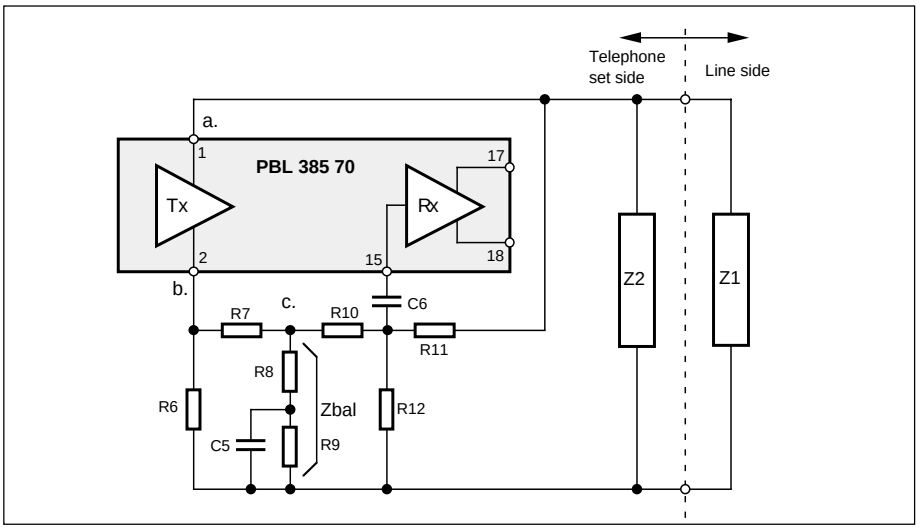


Figure 13. The side tone suppression principle.

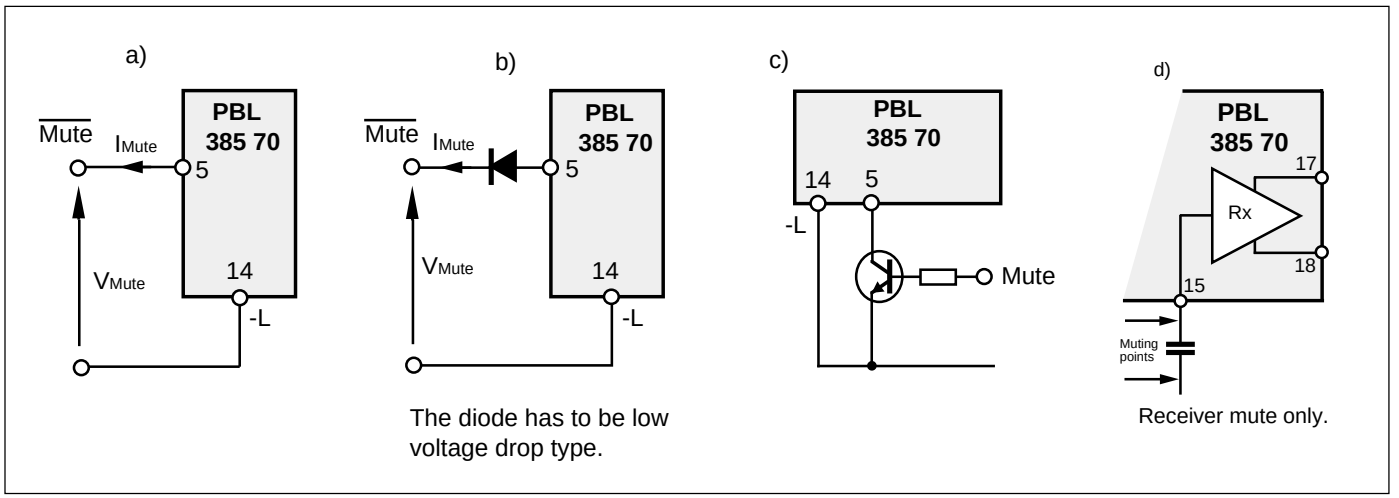


Figure 15. Mute principles.

Mute function

The circuit has a mute function at pin 5. Sinking current from this pin will cut off the gain in the microphone amplifier (attenuation min. 60dB) and decrease the gain in the receiver amplifier to reach the confidence tone level at DTMF-dialling. The receiver mute is ≈ 40dB down from the unmuted value to satisfy those who keep the handset close to the ear at dialling.

Optional conditions.

For users who keep the handset from the ear the confidence tone level is too low. To alter the level, a signal can be taken from DTMF generator output to receiver input before the capacitor C6. The added impedance to this point will hardly disturbe the signal condition in active speech mode. The microphone amplifier only, can be muted by sinking current from the output pin 11. See fig.4 or 9.

Figure 15 b.) If the system mute signal is used to other tasks than muting the speech circuit it has to be isolated. If a diode is used it has to be a low voltage drop type. The input at mute has to be below 300mV. If the mute signal has reverse polarity out of the system it can be phase changed like in e.) In case it is required to mute the receiver only, d.) it can be done by shorting the receiver input to ground before or after the input capacitor. Shorting the input pin to ground (does not have to be absolute ground) actuates a mute by driving the amplifier into saturation thus blocking the signal path and rendering a mute with high attenuation but will cause a DC-level shift at output which in its turn will cause a ”click ” in the earphone. This can be softened with a slower mute signal flank. If the second approach, grounding before the input capacitor is chosen, the grounding has to be low ohmic in order to render a high attenuating mute.

Start up circuit

The circuit contains a start up device which function is to fast charge the capacitor C1 when the circuit goes into hook- off condition. The fast charge circuit is a thyristor function between pins 1 and 4 that will stop conducting when the current drain at pin 4 is lower than ≈ 700 µA + the internal current consumption. (about 1 mA) This circuit can not retrigger before the voltage level at C1 drops below 2V or the line voltage below 1V. See fig 16.

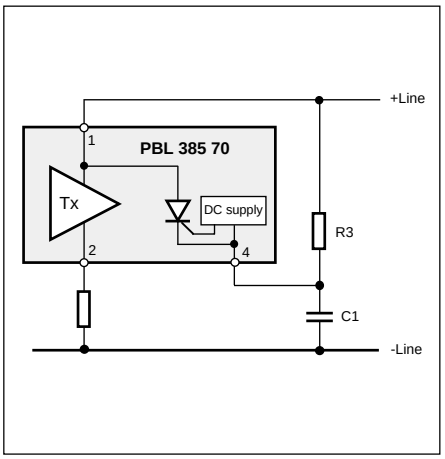


Figure 16. Fast start up principle.

Power supplies DC1, DC2, V_{+C} and V_{PA} (See fig.17)

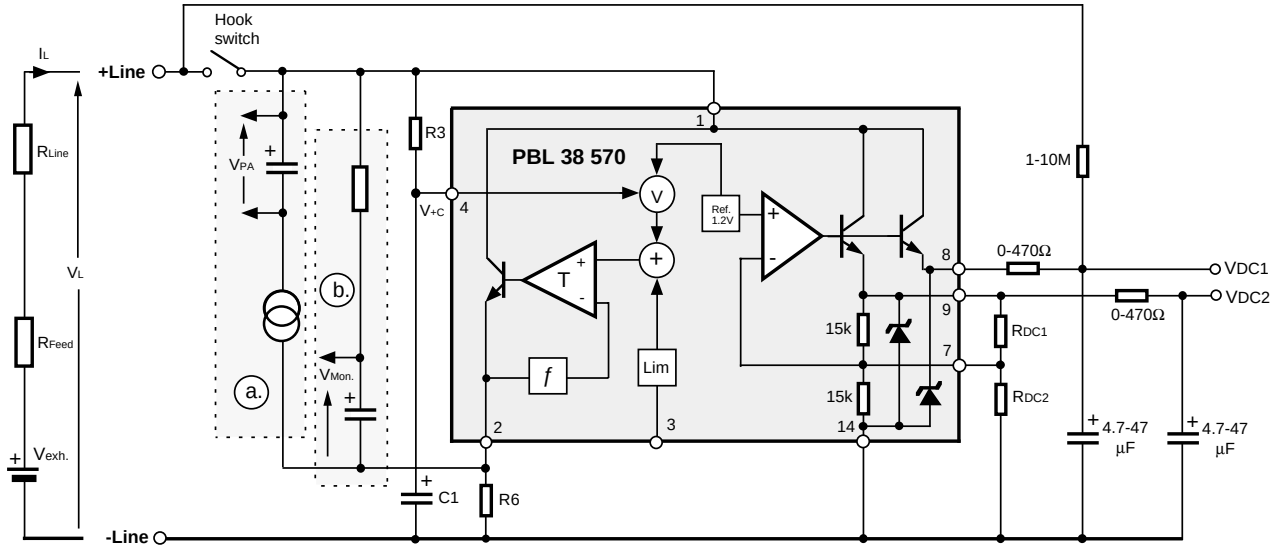
PBL 38570 generates its own DC supply V_{+C} dependent of line current with an internal shunt regulator. This regulator senses the line voltage V_L via R_3 and line current via R_6 in order to set the correct V_{+C} so the circuit can generate the required DC characteristic for a given line resistance R_{Line} and the line feeding data of the exchange. A decoupling capacitor is needed between pins +C and -L. The V_{+C} supply changes its voltage linearly with the line current. It can be used to feed an electret microphone. Caution must be taken though not to drain too much current out of this output because it will affect the internal quick start circuit by locking itself into active state. (max. permissible current drain 700µA).

Care has to be taken when deciding the resistance value of R3. All resistances that are applied from +Line to ground (-Line) will be in parallel, forming the real impedance towards the line. This will sometimes result in, that the ohmic value of R3 is increased in order to comply to the impedance specification towards the line. The speech circuit sinks ≈ 1mA into pin 4, which means that the working voltage for the speech function V+ will decrease with increasing R3, thus starving in the end the circuit of its working voltage . This dependency is often falsely taken as a sign of that the circuit does not work down to the low line current specified, but in fact it is the working voltage at pin 4 that has become too low. It is obvious that this problem is also connected into what kind of DC-characteristic is set. See fig. 7.

The circuit has further two temperature and line current compensated DC supplies DC1 and DC2. DC1 is a voltage supply for supplying diallers, can also be used for memory back up because it does not leak any current back into the circuit. Typical voltage 2.4V down to line voltage of 4.1V, in case the line voltage is lower than 4.1V calculate ; actual line voltage minus 1.9V. In order to prevent noise entering the line, a series resistor and a reservoir capaciotor is recommended in series at this output. The output current is given to be 2 mA in the specification. In case this would not be enough the current capability can be increased by connecting the outputs of DC1 and DC2 in parallel. The driving capacity will increase almost to the double but the voltage drop across the necessary series resistor will go upp thus limiting the useful current.

The voltage level that is common for both of these supplies is set by DC2. DC2 is a high precision, reference quality supply that can be used to supply microphones, opto couplers etc. The internally set voltage can be adjusted with external resitors when needed (R_{DC1} and R_{DC2}).

The fourth DC-supply V_{PA} has an advantage that it does not influence the circuits DC characteristics even at high current drain. The supply has a floating ground reference in the plus line in order to minimize RFI problems and is used to supply the power amplifier of a handsfree telephone (PBL3881, 38811---14). These circuits have a current controlled charging of the supply capacitor and the control signal is taken across the resistor R6. In case a monitor amplifier is required where the ground reference is hardly necessary, it can be supplied from V_{PA} or like in alt. b in fig. 17.



a. Supply arrangement for a handsfree system power amplifier. For ex. PBL 38811---14

b. Supply arrangement for a call monitor cicuit.

Figure 17. DC-supplies

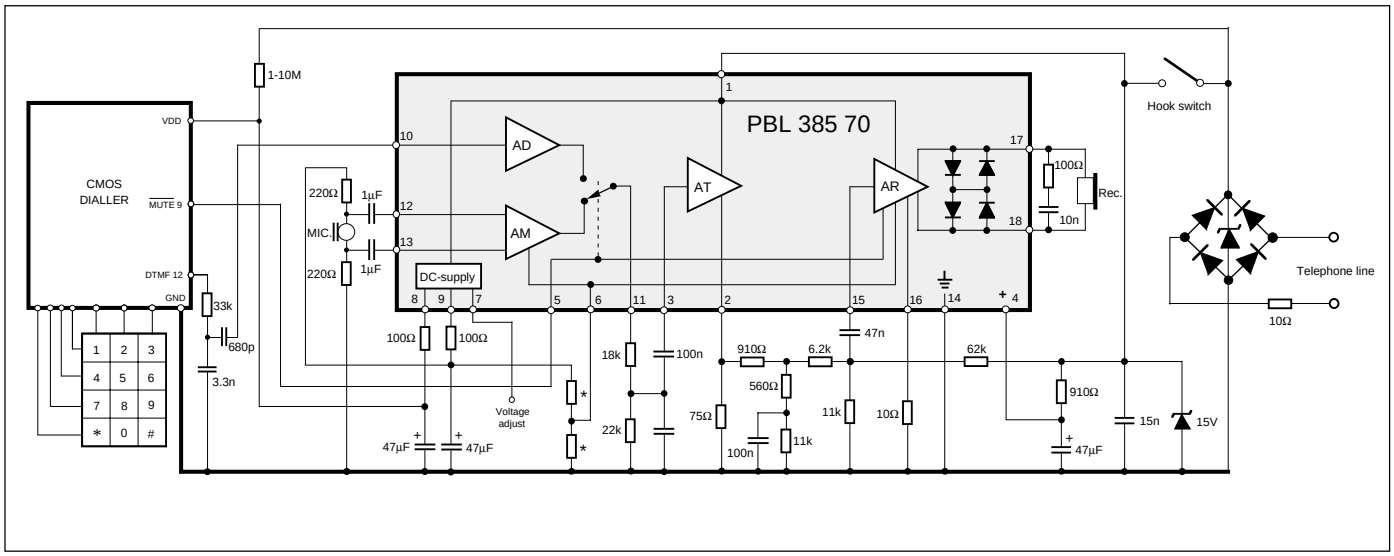


*Figure 18. Typical DTMF tone dialling telephone. 18-pin DIP package. * marked components for gain regulation.*

Ordering Information

Package	Temp. Range	Part No.
Plastic DIP	-40 to +70°C	PBL 385 70/1N
Plastic SO	-40 to +70°C	PBL 385 70/1SO
Plastic SO	-40 to +70°C	PBL 385 70/1SO:T

1522-PBL 385 70/1

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