Integer Divider
32-Bit, 20 MOPS

The TMC3211 is a fast monolithic two's complement integer divider which can divide a 32-bit dividend by a 16-bit divisor to produce a 32-bit quotient, with a maximum pipelined throughput of 20 MOPS (Million Operations Per Second). Data is input on separate busses, and quotients are available on a 32-bit output bus with synchronous three-state enable. All data inputs and outputs are registered and TTL compatible. All input and output signal timing is referenced to the rising edge of Clock.

The TMC3211 has a single system clock and separate load enable controls for the dividend and divisor registers. This allows the device to be used in applications requiring division by a constant. Underflow automatically produces the expected zero quotient, and dividing by zero sets a divide-by-zero output flag.

The internal architecture of the TMC3211 allows all 32-bit two's complement integer dividends and nonzero 16-bit two's complement integer divisors, without prenormalization. The output quotient format is 32-bit integer.

The TMC3211 makes a full-precision, full-speed divide function available to designers of Workstations, Image Processors, and Radar Systems who need to perform perspective extractions, matrix operations, range scaling, and other complex functions.

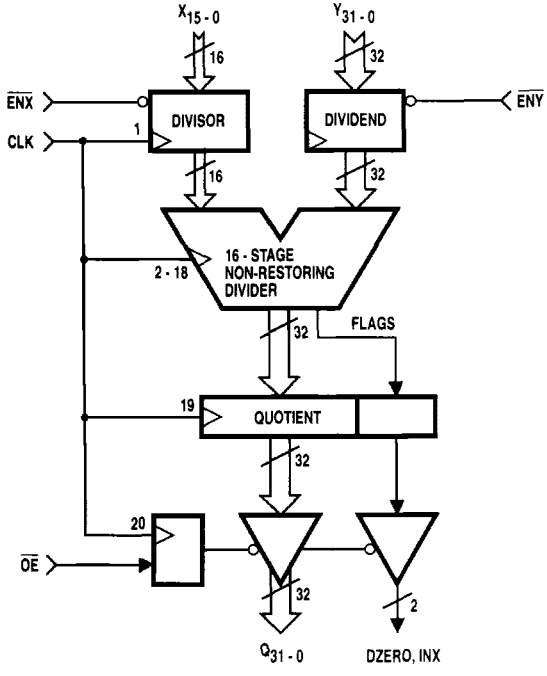
Features

- 32-Bit By 16-Bit Fixed-Point Integer Division With 32-Bit Quotient
- 20MHz Clock Rate And Pipelined Throughput Rate
- Three-Bus I/O Architecture Allows Unrestricted Throughput
- Easy System Interfacing
- Status Flags For Divide-By-Zero And Inexact Result
- All Inputs And Outputs TTL Compatible
- Low Power CMOS Technology
- Available In A 120 Pin Plastic Pin Grid Array Package

Applications

- Graphics And Image Processors
- Matrix Operations And Geometric Transforms
- Perspective Extraction
- Radar Signal Processing
- Range Scaling

Functional Block Diagram



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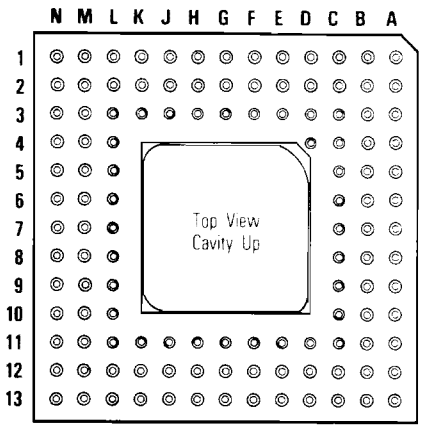
Pin Assignments

120-Pin Plastic Pin Grid Array – H5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	V_{DD}	L3	GND	L11	V_{DD}	C11	GND
B2	Y_{15}	M2	X_0	M12	GND	B12	Q_7
B1	$\overline{YEN}$	N2	X_1	M13	Q_{25}	A12	Q_6
D3	GND	L4	V_{DD}	K11	V_{DD}	C10	Q_5
C2	V_{DD}	M3	X_2	L12	GND	B11	Q_4
C1	Y_{16}	N3	X_3	L13	Q_{24}	A11	Q_3
D2	Y_{17}	M4	X_4	K12	Q_{23}	B10	Q_2
E3	GND	L5	GND	J11	V_{DD}	C9	Q_1
D1	Y_{18}	N4	X_5	K13	Q_{22}	A10	Q_0
E2	Y_{19}	M5	X_6	J12	Q_{21}	B9	DZ
E1	Y_{20}	N5	X_7	J13	Q_{20}	A9	REM
F3	V_{DD}	L6	X_8	H11	GND	C8	Y_0
F2	Y_{21}	M6	X_9	H12	Q_{19}	B8	Y_1
F1	Y_{22}	N6	X_{10}	H13	Q_{18}	A8	Y_2
G2	GND	M7	X_{11}	G12	V_{DD}	B7	Y_3
G3	V_{DD}	L7	V_{DD}	G11	Q_{17}	C7	Y_4
G1	Y_{23}	N7	X_{12}	G13	Q_{16}	A7	Y_5
H1	Y_{24}	N8	X_{13}	F13	Q_{15}	A6	Y_6
H2	Y_{25}	M8	X_{14}	F12	Q_{14}	B6	Y_7
H3	GND	L8	X_{15}	F11	V_{DD}	C6	Y_8
J1	Y_{26}	N9	$\overline{XEN}$	E13	Q_{13}	A5	Y_9
J2	Y_{27}	M9	CLK	E12	Q_{12}	B5	Y_{10}
K1	Y_{28}	N10	$\overline{OEQ}$	D13	Q_{11}	A4	V_{DD}
J3	V_{DD}	L9	Q_{31}	E11	GND	C5	Y_{11}
K2	Y_{29}	M10	Q_{30}	D12	Q_{10}	B4	Y_{12}
L1	Y_{30}	N11	Q_{29}	C13	Q_9	A3	Y_{13}
M1	Y_{31}	N12	Q_{28}	B13	Q_8	A2	Y_{14}
K3	GND	L10	Q_{27}	D11	V_{DD}	C4	GND
L2	V_{DD}	M11	GND	C12	GND	B3	V_{DD}
N1	GND	N13	Q_{26}	A13	V_{DD}	A1	GND



Functional Description

General Information

The TMC3211 consists of input registers, a pipelined array divider, and output (quotient) registers. The 16-bit divisor and 32-bit dividend input registers can each be loaded independently using the two synchronous load enable controls. The divider is a 16-stage pipelined non-restoring array which produces a 32-bit quotient and condition flags which indicate an attempted division by zero, or operations which yield a non-zero remainder or inexact result. The 32-bit parallel quotient output register includes three-state output drivers with synchronous enable control, which permits multiple TMC3211s to be operated in parallel or connected directly to a system bus.

The TMC3211 requires a total of 19 clock cycles to generate a full 32-bit quotient result. Once the internal pipeline is full, a new quotient is available at the output every clock cycle.

Signal Definitions

Power

V_{DD}, GND — The TMC3211 operates on a single +5V supply. All power and ground lines must be connected.

Clock

CLK — The TMC3211 has a single Clock input. All input and output signal timing is referenced to the rising edge of Clock.

Inputs

Y_{31-0} — The 32-bit Dividend is presented through the registered Y input port. Y_{31} is the sign bit. The LSB is Y_0.

X_{15-0} — The 16-bit Divisor is presented through the registered X input port. X_{15} is the sign bit. The LSB is X_0.

Outputs

Q_{31-0} — The current Quotient is available on the registered Q output bus. Q_{31} is the sign bit. The LSB is Q_0.

Controls

$\overline{YEN}$ — Data present at the Dividend input Y_{31-0} is latched into the input registers on the rising edge of clock when the enable control $\overline{YEN}$ is LOW.

$\overline{XEN}$ — Data present at the Divisor input X_{15-0} is latched into the input registers on the rising edge of clock when the enable control $\overline{XEN}$ is LOW.

$\overline{OEQ}$ — The quotient output bus Q_{31-0} and flags DZ and REM are in the high-impedance state when the registered Output Enable $\overline{OEQ}$ is HIGH. When $\overline{OEQ}$ is LOW, they are enabled on the next clock cycle.

Flags

DZ — Whenever a zero divisor is input, the resulting invalid output quotient will be accompanied by a registered Divide-By-Zero Flag HIGH.

REM — Whenever a division operation leaves a nonzero remainder, the resulting quotient is accompanied by a registered nonzero Remainder Flag HIGH.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package
Power	V_{DD}	Supply Voltage	B3, A4, A13, D11, F11, G12, J11, K11, L11, L7, L4, L2, J3, G3, F3, C2, C3
	GND	Ground	A1, C4, C11, C12, E11, H11, L12, M12, M11, L5, L3, N1, K3, H3, G2, E3, D3
Clock	CLK	System Clock	M9
Inputs	Y_{31-0}	Dividend Data	M1, L1, K2, K1, J2, J1, H2, H1, G1, F1, F2, E1, E2, D1, D2, C1, B2, A2, A3, B4, C5, B5, A5, C6, B6, A6, A7, C7, B7, A8, B8, C8
	X_{15-0}	Divisor Data	L8, M8, N8, N7, M7, N6, M6, L6, N5, M5, N4, M4, N3, M3, N2, M2
Outputs	Q_{31-0}	Quotient Data	L9, M10, N11, N12, L10, N13, M13, L13, K12, K13, J12, J13, H12, H13, G11, G13, F13, F12, E13, E12, D13, D12, C13, B13, B12, A12, C10, B11, A11, B10, C9, A10
Controls	$\overline{YEN}$	Dividend Write Enable	B1
	$\overline{XEN}$	Divisor Write Enable	N9
	$\overline{OEQ}$	Quotient Output Enable	N10
Flags	DZ	Divide-By Zero Flag	B9
	REM	Inexact Remainder Flag	A9
No Connect		Index Pin	D4

Applications Discussion

Division Using A Constant

By utilizing the separate input data register load enable controls, the TMC3211 can perform division by a constant. The data currently held remain in the input registers until updated by the user.

Data Formats

The TMC3211 supports fixed-point two's complement data formats. By keeping track of the binary points of the input data, the user can then interpret the resulting quotient properly. Two possible binary weightings of the input and output bits are as follows:

Figure 1. Integer Data Format

Pin	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Y	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
X																	-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Q	-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Figure 2. Fractional Data Format

Y	-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}
X																	-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
Q	-2^{15}	$.2^{14}$	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

where a leading minus sign indicates a sign bit.

Care must be taken when adopting fractional data formats. By observing the binary weighting applied to the input data in the dividend and divisor, the binary point of the quotient can then be correctly established. The difference lies only in constant scale factors, which must be considered in order to maintain a data format which is compatible with the bit weighting of the hardware system. The two most common choices are fractional and integer notation. If integer notation is used, the LSBs of the dividend, divisor, and quotient all have the same value. With fractional notation the MSBs are all of equal weight.

Divide by Zero

The flag DZ indicates that the divisor input for the current calculation was a zero, independent of the dividend. Dividing by zero is an undefined operation yielding a meaningless quotient. Thus, this flag must be monitored to guard against possible errors.

Inexact Results

The flag REM is provided to indicate that the current quotient left a nonzero remainder and was truncated toward zero.

Negative Full-Scale Overflow

Due to a finite data word width, a two's complement overflow error occurs under the following unique condition:

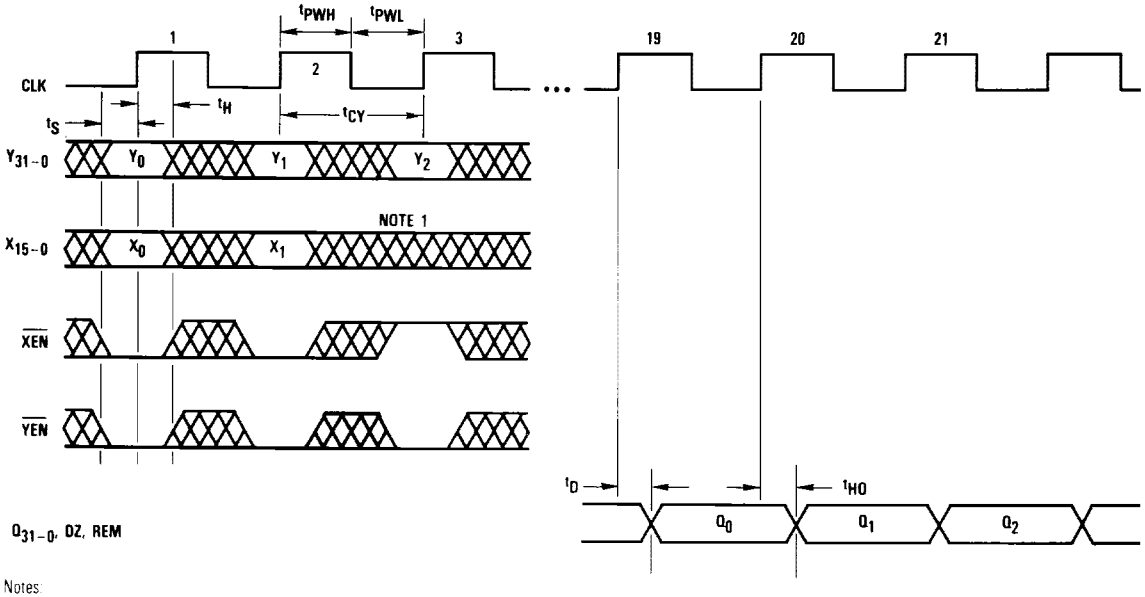
Divisor $Y = 80000000_H$ (−Full-Scale)
Dividend $X = FFFF_H$ (−1)

Result:

Quotient $Q = 80000000_H$ (−Full-Scale)

As stated above, this is due to a limitation in the number of bits available to indicate a positive full-scale quotient, and data overflows into the MSB position to indicate an incorrect sign.

Figure 3. Timing Diagram



Notes:

1. Demonstrates division by a constant, $Q_2 = Y_2/X_1$.
2. Assumes $\overline{OEQ}$ = LOW.

Figure 4. Equivalent Input Circuit

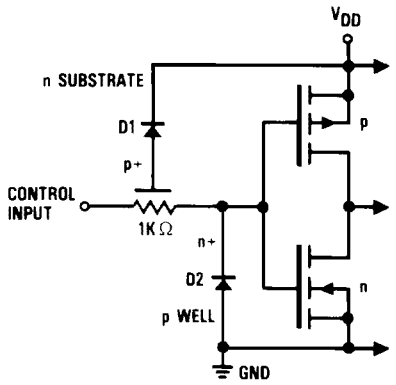
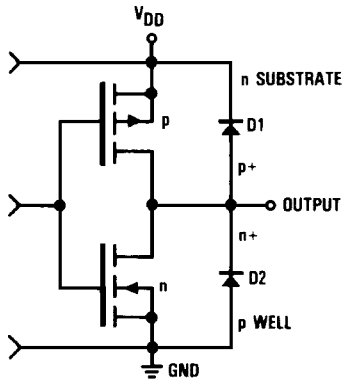


Figure 5. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD} + 0.5)V
Output	
Applied voltage[2]	−0.5 to (V_{DD} + 0.5)V
Forced current[3,4]	−3.0 to 6.0mA
Short−circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Nom	Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
V_{IL}	Input Voltage, Logic LOW				0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			V
I_{OL}	Output Current, Logic LOW				4.0	mA
I_{OH}	Output Current, Logic HIGH				−2.0	mA
t_{CY}	Cycle Time	V_{DD} = Min			50	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD} = Min	15			ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15			ns
t_S	Input Setup Time		12			ns
t_H	Input Hold Time		6			ns
T_A	Ambient Temperature, Still Air		0		70	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range (Standard) Min	Temperature Range (Standard) Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		5	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OEQ}$ = 5V, f = 20MHz		150	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.		−150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range (Standard) Min	Temperature Range (Standard) Max	Units
t_D	Output Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		35	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	5		ns

Note: 1. Equivalent to t_{DIS} and t_{ENA} of the three-state outputs.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3211H5C	STD − T_A = 0°C to 70°C	Commercial	120 Pin Plastic Pin Grid Array	3211H5C