8-Bit Two-Stage Pipelined Register/Latch

SN54/74LS548 SN54/74LS549

Feature/Benefits

- Two 8-bit high-speed registers/latches
- Faster than other LS-TTL registers/latches
- Three-state outputs drive bus lines
- 24-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Multiplexer selects either rank at input/output
- Output can drive bus directly: I_{OL} 32 mA (com), 24 mA (mil)
- Registers/latches configurable for nose-to-tail or side-by-side operation
- Individual clock/gate enables for each rank

Applications

- Registers for pipelined arithmetic units or digital signal processors
- Bus monitor for popular 8-bit microprocessors to restart instructions upon virtual memory page fault
- Video display character/attribute pipelined registers
- Sequence/state generator for systems: dual-rank registers/latches allow storing a backup previous state for redundancy, or diagnostics
- Two-stage buffer for pipelined interfacing input/output

Description

The 54/74LS548 and 54/74LS549 contain a pair of high-speed 8-bit registers ('LS548) or latches ('LS549) which perform various pipeline storage functions. Two control pins govern a pair of internal multiplexers, as shown in the block diagrams; using these, several useful data paths can be configured. The input selection multiplexer determines the source of data to the second register/latch, as controlled by the INSEL line. In this way, data from either the D7-D0 inputs, or the outputs of the first register/latch, are stored in the second register/latch. The output selection multiplexer determines the source of data that will be sent to the outputs Y7-Y0. This multiplexer is controlled by the OUTSEL line, and allows either the first or second register/latch data to be output. The outputs are fully buffered, provide high-drive current, and allow three-state control through the $\overline{OE}$ line.

Ordering Information

PART NUMBER	PKG	TEMP	TYPE	POWER
SN54LS548	JS,W,L(28)	Mil	Register	LS
SN74LS548	NS,JS,NL(28)	Com	Register	LS
SN54LS549	JS,W,L(28)	Mil	Latch	LS
SN74LS549	NS,JS,NL(28)	Com	Latch	LS

The arrangement of registers/latches within the 'LS548/'LS549 can be thought of a two 8-bit storage ranks, rank 1 and rank 2. The 'LS548 has a common clock line CK, and separate clock enables $\overline{CKE1}$ and $\overline{CKE2}$ for rank 1 and rank 2 respectively. In contrast, the 'LS549 operates as a flow-through latch, and has separate latch enables $\overline{G1}$ and $\overline{G2}$ for each rank, as well as a common latch-enable input G.

In the 'LS548, data present at the D7-D0 inputs are stored in rank 1 on the positive edge of CK, if $\overline{CKE1}$ has been previously asserted. Data for rank 2 are stored similarly, if $\overline{CKE2}$ is asserted prior to the clock. In the 'LS549, data pass through the latches when the latch controls ($\overline{G1}$ or $\overline{G2}$) for either rank are enabled simultaneously with the common latch enable G. Data remain in a rank when the latch controls are disabled, or 'unasserted'.

The clock/gate control lines are used with the INSEL and OUTSEL controls for flexible data storage and movement operations. Two representative examples are shown in Figure 1 (a) and 1 (b). The first example is a classical 2-stage pipelined register, or 'nose-to-tail' configuration. Data at D7-D0 are first stored in rank 1, then stored in rank 2 on the next clock/gate. If the clock/gate enable for either rank becomes unasserted, then the previously-stored data are simply retained. In the second example, data at D7-D0 are stored in either or both ranks if the respective clock/gate enable signals are asserted. In this 'side-by-side' configuration, data sent to the Y7-Y0 outputs are selected from either rank 1 or rank 2, under control of the OUTSEL line.

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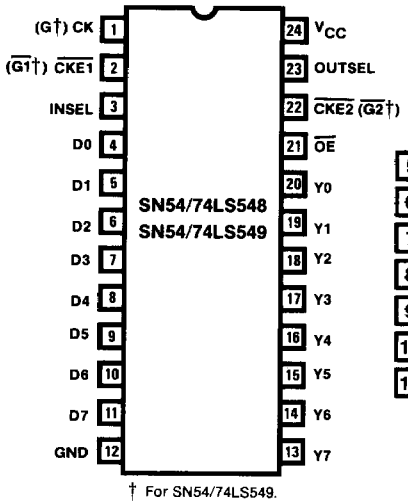
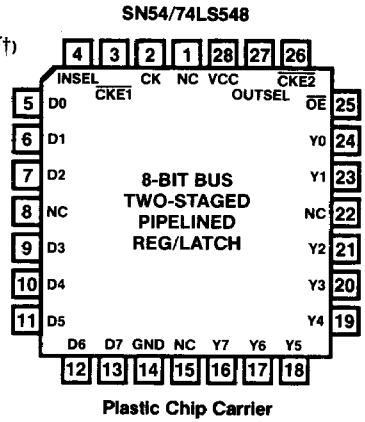
Monolithic Memories MMI

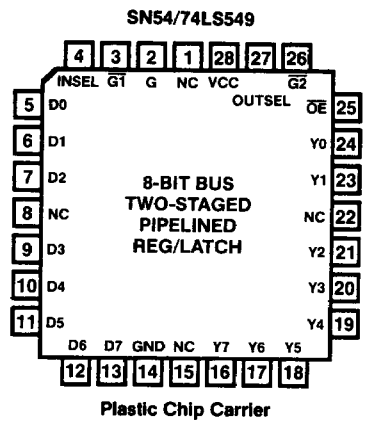
Pin Configurations



† For SN54/74LS549.

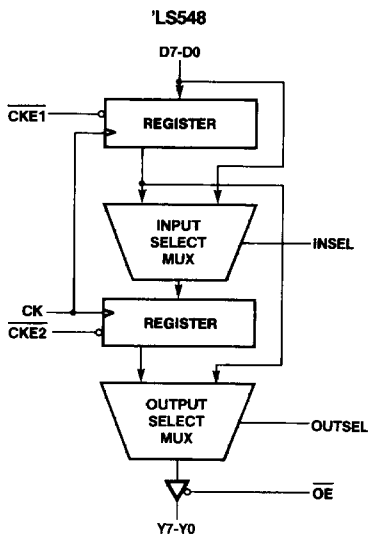


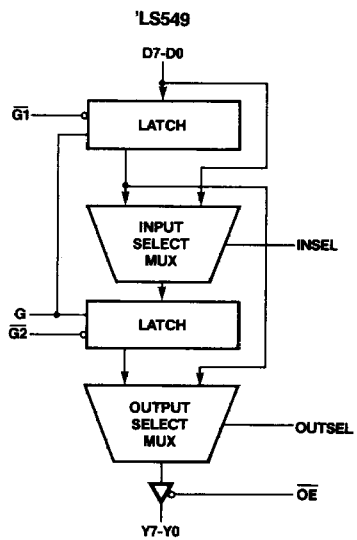
Plastic Chip Carrier



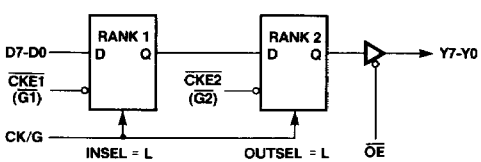
Plastic Chip Carrier

Block Diagrams

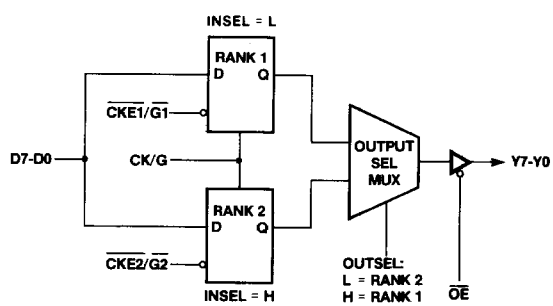




Typical Configurations



(a) Nose-to-Tail



(b) Side-by-Side

Figure 1

Function Table Nomenclature Description

Rank 1-Q or Rank 2-Q = Data available at the internal flip-flop/latch outputs for the 8 rank 1 or rank 2 registers/latches respectively.

D = Data at the D0-D7 input pins.

Y = Data at the Y0-Y7 output pins.

X = H or L state irrelevant ("don't care" conditions)

Q_0 = Previous states of the internal register/latch data are retained.

Z = Indicates that the Y0-Y7 outputs are in high-impedance state.

INSEL = Input select mux control pin; determines the source of input data for rank 2.

INSEL	RANK 2 INPUT
L	Rank 1
H	D

OUTSEL = Output select mux control pin; selects either rank 1 or rank 2 for output.

OUTSEL	OUTPUT
L	Rank 2
H	Rank 1

$\overline{\text{OE}}$ = Output enable pin.

$\overline{\text{OE}}$	OUTPUT
L	Rank 1 or Rank 2
H	Hi-Z

↑ = Positive edge of CK causes clocking, if clocking is enabled.

CK = The common clock line for the 54/74LS548.

$\overline{\text{CKE1}}/\overline{\text{CKE2}}$ = Clock enable line for the rank 1/ rank 2 register in the 54/74LS548.

CK	$\overline{\text{CKE1}}$	$\overline{\text{CKE2}}$	RANK 1	RANK 2
L or H or ↓	X	X	Disabled	Disabled
↑	L	L	Enabled	Enabled
↑	L	H	Enabled	Disabled
↑	H	L	Disabled	Enabled
X	H	H	Disabled	Disabled

G = The common latch control line for the 54/74LS549.

$\overline{\text{G1}}/\overline{\text{G2}}$ = Latch enable line for the rank 1/ rank 2 latch in the 54/74LS549.

G	$\overline{\text{G1}}$	$\overline{\text{G2}}$	RANK 1	RANK 2
L	L	L	Enabled (Flush)	Enabled (Flush)
L	L	H	Enabled (Flush)	Disabled (Freeze)
L	H	L	Disabled (Freeze)	Enabled (Flush)
L	H	H	Disabled (Freeze)	Disabled (Freeze)
H	X	X	Enabled (Flush)	Enabled (Flush)

'LS548 Function Table

CK	$\overline{CKE1}$	RANK 1	$\overline{CKE2}$	INSEL	RANK 2
L or H or ↓	X	Q0	X	X	Q0
↑	H	Q0	H	X	Q0
↑	L	D	H	X	Q0
↑	L	D	L	L	Rank 1-Q
↑	L	D	L	H	D
↑	H	Q0	L	L	Rank 1-Q
↑	H	Q0	L	H	D

'LS549 Function Table

G	$\overline{G1}$	RANK 1	$\overline{G2}$	INSEL	RANK 2
L	L	D	L	L	Rank 1-Q
L	L	D	L	H	D
L	L	D	H	X	Q0
L	H	Q0	L	L	Rank 1-Q
L	H	Q0	L	H	D
L	H	Q0	H	X	Q0
H	X	D	X	L	Rank 1-Q
H	X	D	X	H	D

'LS548/549 Output Function Table

OUTSEL	$\overline{OE}$	Y
L	L	Rank 2-Q
H	L	Rank 1-Q
X	H	Hi-Z

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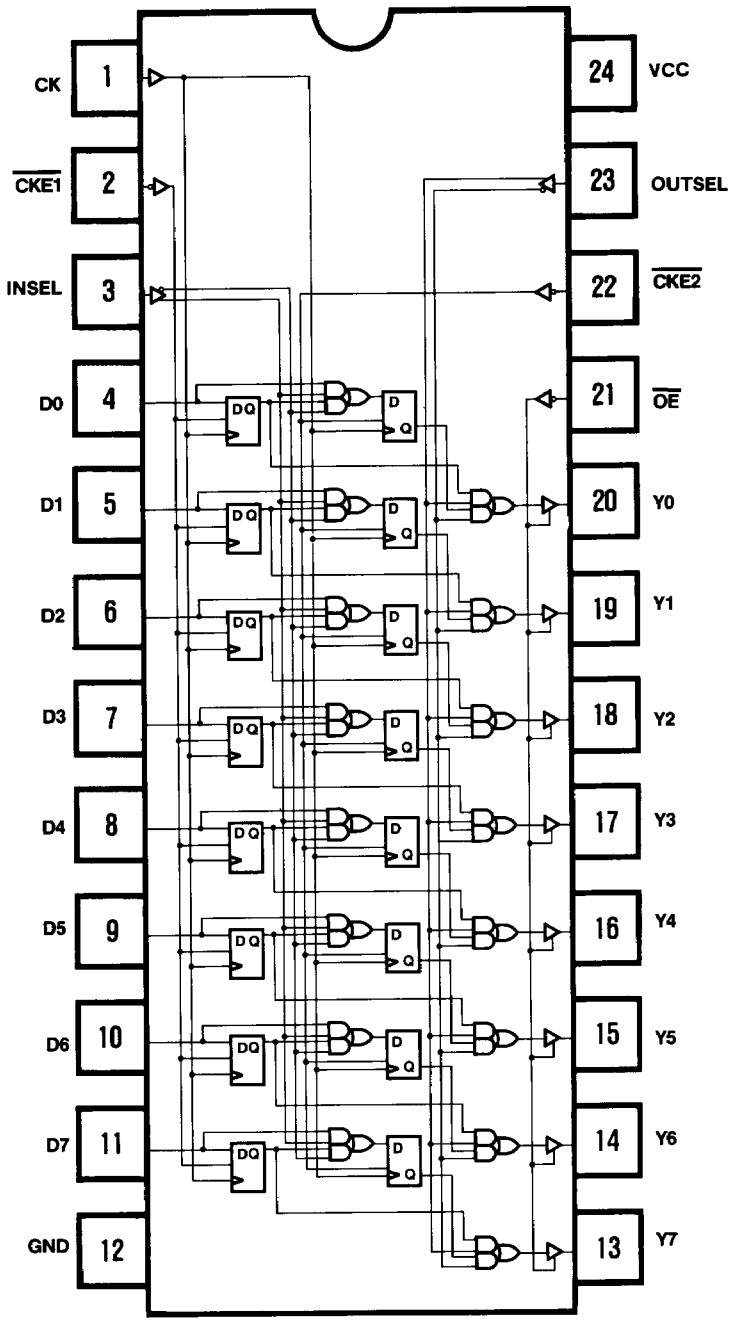
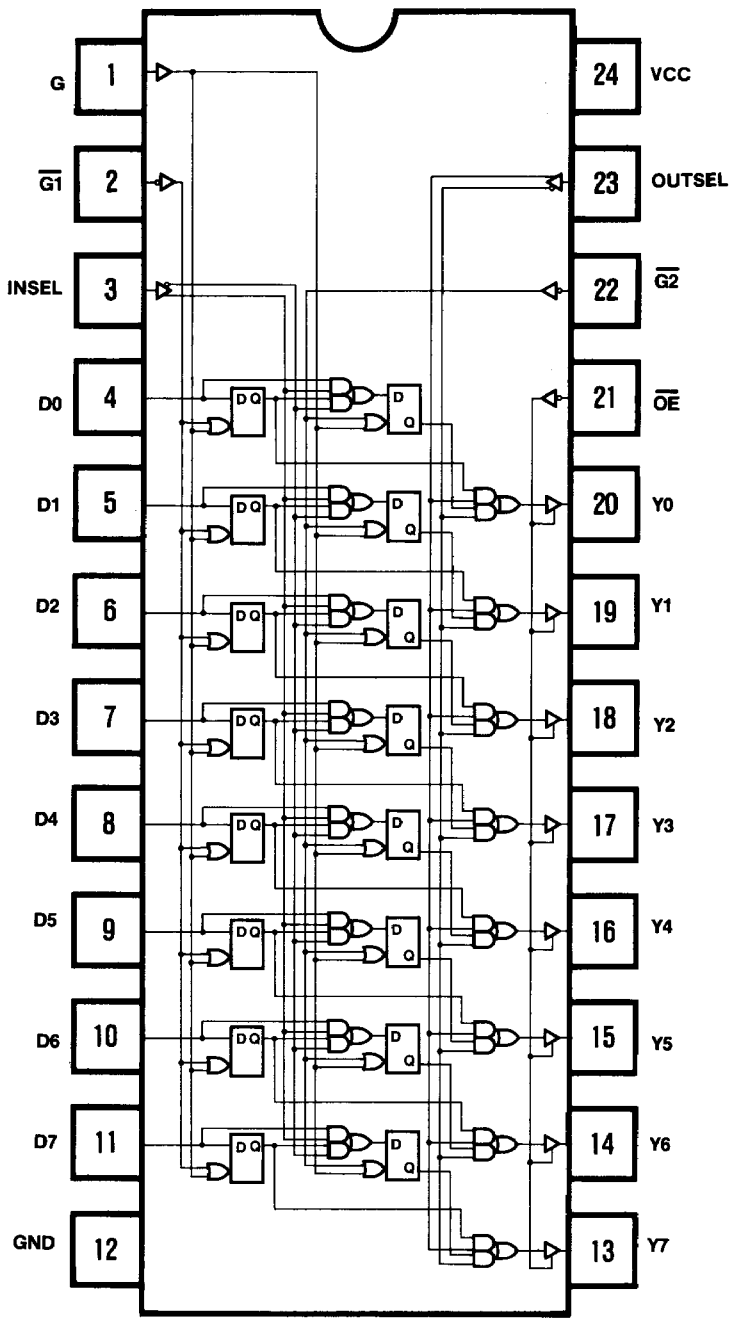
Logic Diagram

54/74LS548 Pipelined Register



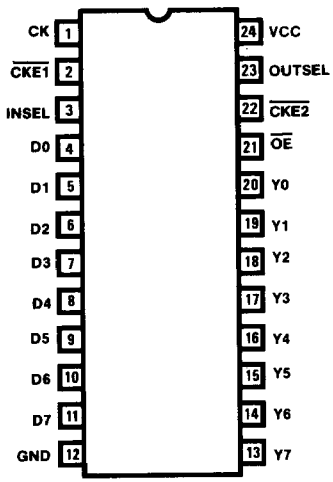
Logic Diagram

54/74LS549 Pipelined Latch

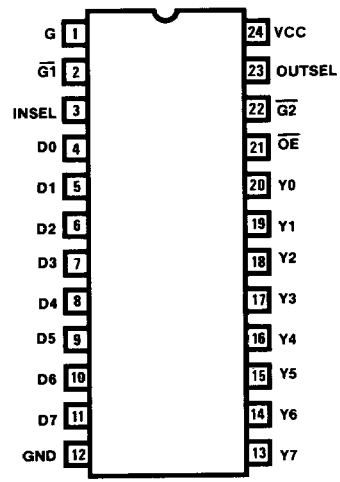


Pin Configurations

'LS548

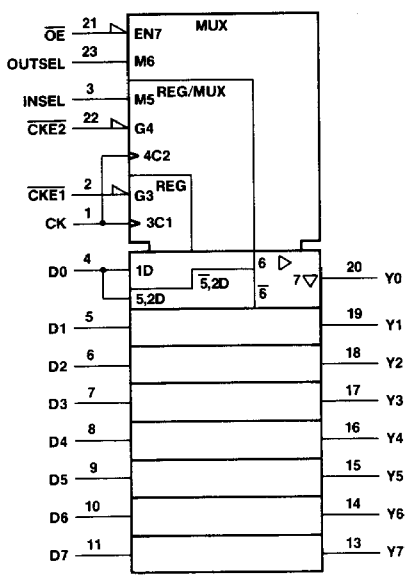


'LS549

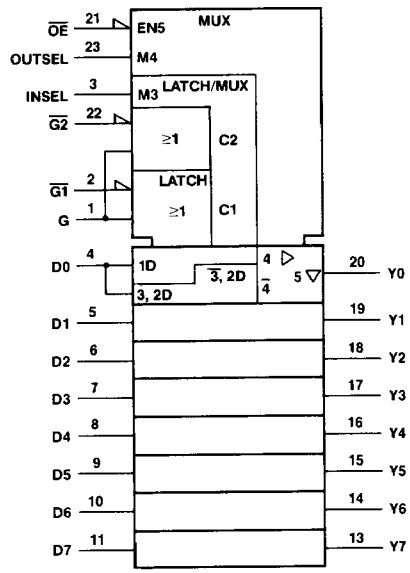


IEEE Symbols

'LS548



'LS549



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER				MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage				4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				-55		125	0		75	°C
t_w	Width of CK, G, $\overline{G1}$, $\overline{G2}$	High	'LS548	CK	15			11			ns
			'LS549	G							
		Low	'LS548	CK	15			11			ns
			'LS548	$\overline{G1}$, $\overline{G2}$	18			16			
t_{su}	Setup time for Data		'LS548	CK	20↑			15↑			ns
			'LS549	G	10↓			6↓			
				$\overline{G1}$, $\overline{G2}$	17↑			4↑			
t_h	Hold time for Data		'LS548	CK	0↑			0↑			ns
			'LS549	G	12↓			10↓			
				$\overline{G1}$, $\overline{G2}$	5↑			5			
$t_{su\text{-}CKEX}$	Setup time for clock enables $\overline{CKE1}$, $\overline{CKE2}$ ('LS548 only)				15↑			10↑			ns
$t_{h\text{-}CKEX}$	Hold time for clock enable $\overline{CKE1}$, $\overline{CKE2}$, ('LS548 only)				8↑			5↑			ns
$t_{su\text{-}INSEL}$	Setup time for INSEL[1]				30			25			ns
$t_{h\text{-}INSEL}$	Hold time for INSEL[2]				0			0			ns

NOTES: 1. This is the minimum setup time needed for INSEL prior to the rising edge of the clock/$\overline{GX}$, and to the falling edge of the G, to ensure data transfer to rank 2.
2. This is the minimum hold time needed for INSEL after the rising edge of the clock/$\overline{GX}$, and to the falling edge of the G, to ensure data transfer to rank 2.
↑↓ the arrow indicates the transition of the clock/gate input used for reference:
↑ for the low-to-high transitions,
↓ for the high-to-low transitions.

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Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2.0			2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V	D or Y			−250			−250	μA
				All others			−400			−400	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	D or Y	V_{CC} = MIN	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 32 mA					0.35	0.5	V
				I_{OL} = 24 mA			0.5				
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1 mA	2.4	3.4					V
				I_{OH} = −2.6 mA				2.4	3.1		
I_{OZL}	Off-State output current		V_{CC} = MAX, V_{IL} = MAX, V_{IH} = 2V	V_O = 0.4 V			−20			−20	μA
I_{OZH}				V_O = 2.7 V			20			20	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply Current		V_{CC} = MAX, Outputs open	'LS548			150			150	mA
				'LS549			160			160	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS548 MIN	'LS548 MAX	'LS549 MIN	'LS549 MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF, R_L = 280Ω, $\overline{OE}$ = L	50				MHz
t_{PLH}/t_{PHL}	CK, $\overline{G1}$, or $\overline{G2}$ to output delay			18		22	ns
t_{PLH}/t_{PHL}	G to output delay ('LS549)					23	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS549)					16	ns
t_{PLH}/t_{PHL}	Output multiplexer control OUTSEL to output delay			20		20	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF, R_L = 280Ω		18		18	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF, R_L = 280Ω		15		15	ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIL 'LS548 MIN	MIL 'LS548 MAX	MIL 'LS549 MIN	MIL 'LS549 MAX	COM 'LS548 MIN	COM 'LS548 MAX	COM 'LS549 MIN	COM 'LS549 MAX	UNIT
f_{MAX}	Maximum clock frequency		33				45				MHz
t_{PLH}/t_{PHL}	CK, $\overline{G1}$ or $\overline{G2}$ to output delay	C_L = 45 pF, R_L = 280Ω, $\overline{OE}$ = L		25		26		20		24	ns
t_{PLH}/t_{PHL}	G to output delay ('LS549)					28				25	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS549)					24				18	ns
t_{PLH}/t_{PHL}	Output multiplexer control OUTSEL to output delay			27		27		22		22	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF, R_L = 280Ω		23		23		20		20	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF, R_L = 280Ω		20		20		17		17	ns

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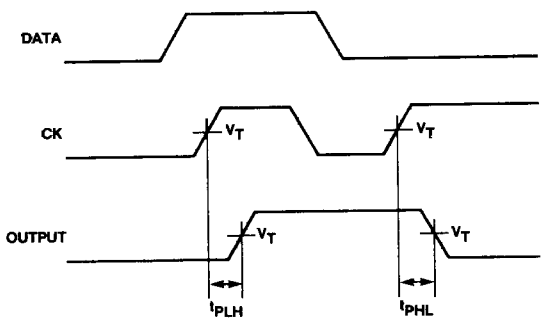
Test Waveforms

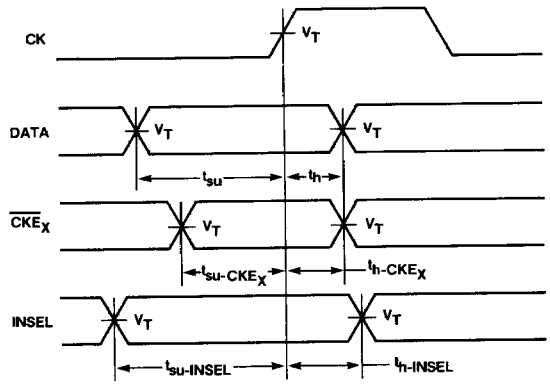
'LS548

CK to Output Delay



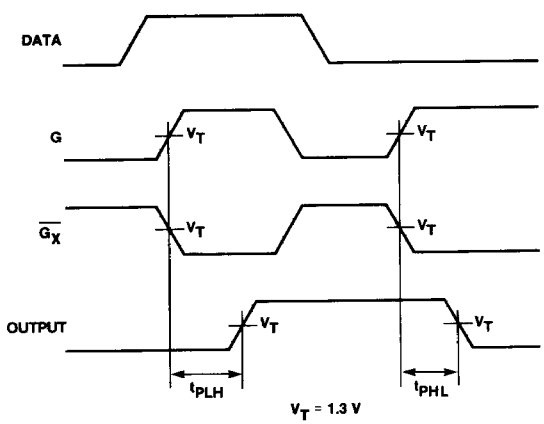
V_T = 1.3 V

Setup and Hold



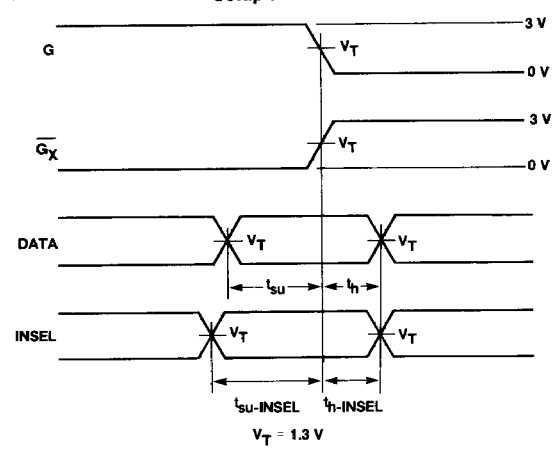
'LS549

G to Output Delay



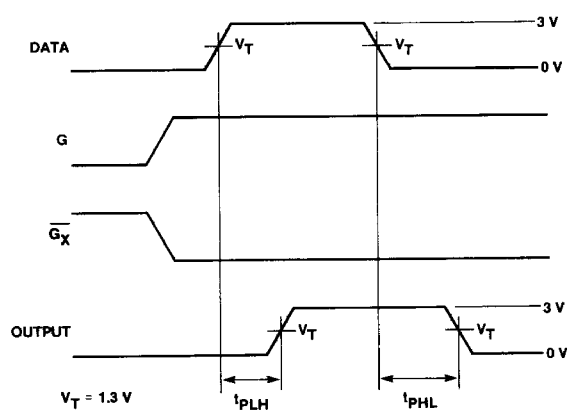
V_T = 1.3 V

Setup and Hold



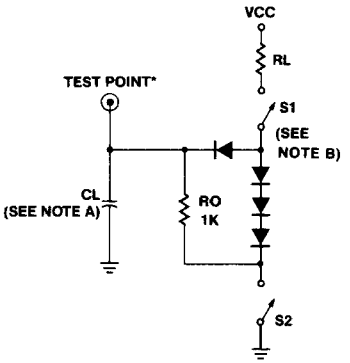
V_T = 1.3 V

Data D to Output Delay

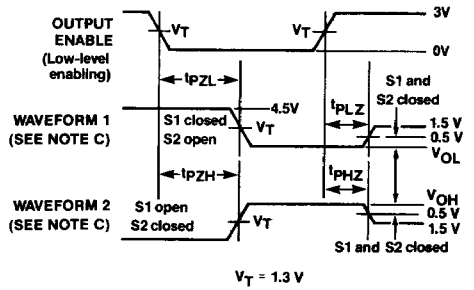


V_T = 1.3 V

Standard Test Load



Load Circuit for Three-state Outputs



'LS548/549 Enable and Disable

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{OUT} = 50 Ω and t_R = 15 ns t_F ≤ 6 ns.

F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

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