Features

- Fits for X.25 (level-2) data formats recommended by CCITT
- Supports up to 128 bytes FIFO in both transmit and receive directions
- Transmit/receive channel number arbitrarily selectable
- Programmable FIFO interrupt for full and empty
- Optional transparent mode, no HDLC frame is performed
- Memory-mapped read and write registers.
- Handshake signals for multiplexing data link
- 2 Mb/s ST-Bus compatible I/O
- Produces and detects various sequences and flags
- Supports single byte address detection
- Interface to Motorola microprocessor
- Independent Watchdog Timer
- TTL/CMOS compatible input/output
- Package Available: 28-pin PDIP and 28-pin PLCC

Applications

- Data link controllers and protocol generators
- Digital Phoneset, Pairgain, WLL, DLC, PBXs and private packet networks
- Analog Linecard signalling controllers
- D-channel controllers for ISDN access
- Interprocessor communication

Introduction

The PT7A8952 consists of single channel HDLC controller which is able to handle bit oriented protocol structure and to format the data as per the packet switching protocol defined in the X.25 (Level 2) recommendations of the CCITT. HDLC data format is shown in Table 4. In the transferring of the data packet, the PT7A8952 is responsible for zero insertion and deletion and performs cyclic redundancy check according to the polynomial specified by CCITT. In addition, it generates and detects various flags and sequences according to the state of transmission. It also performs the single byte address detection of the received packet by setting RxAD bit in the control register.

With provision to allow the PT7A8952 to be used in other protocol, the HDLC protocol process can be disabled. Thus, the microprocessor can process the data on the ST-Bus directly.

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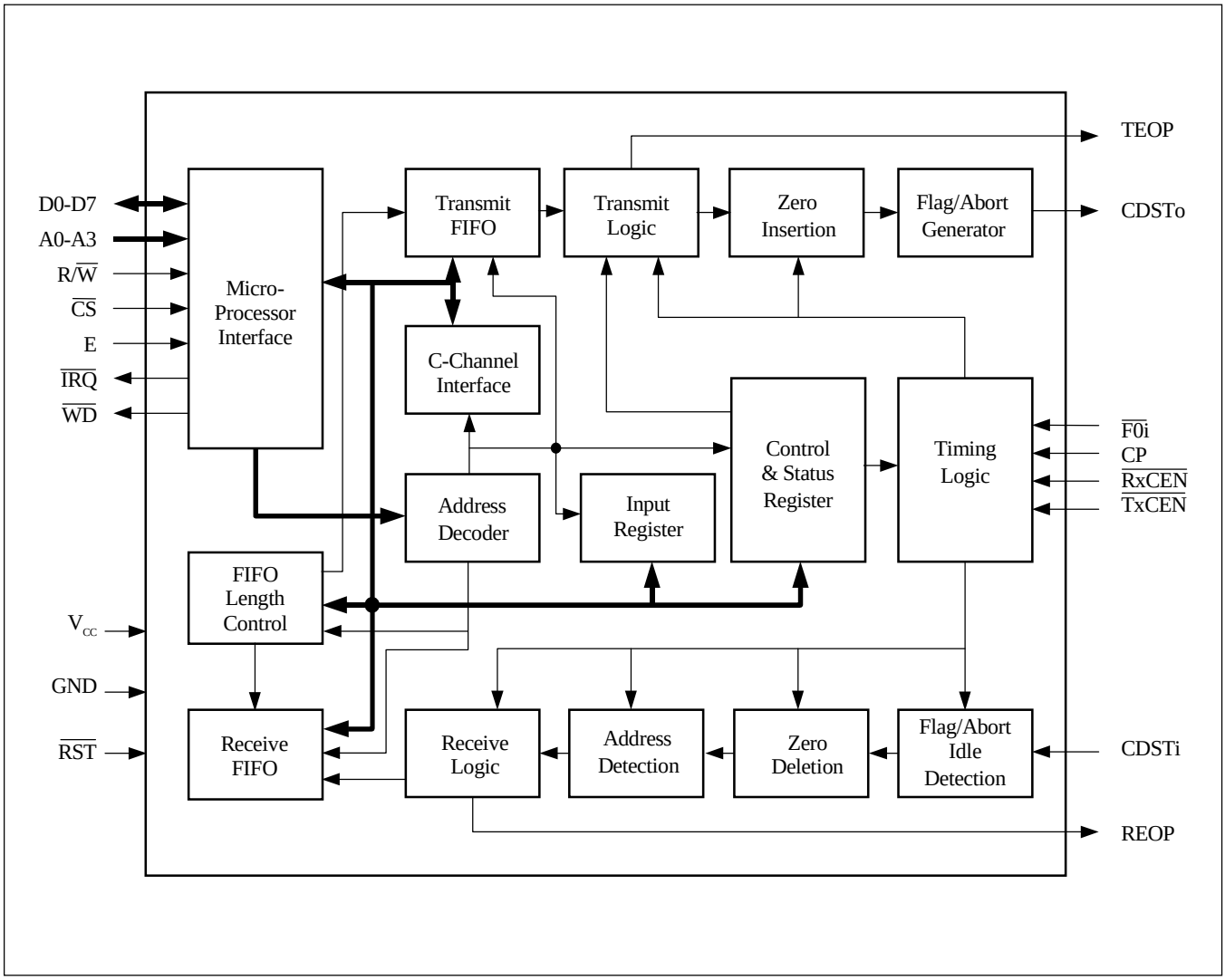
Block Diagram

Figure 1. Block Diagram



Pin Information

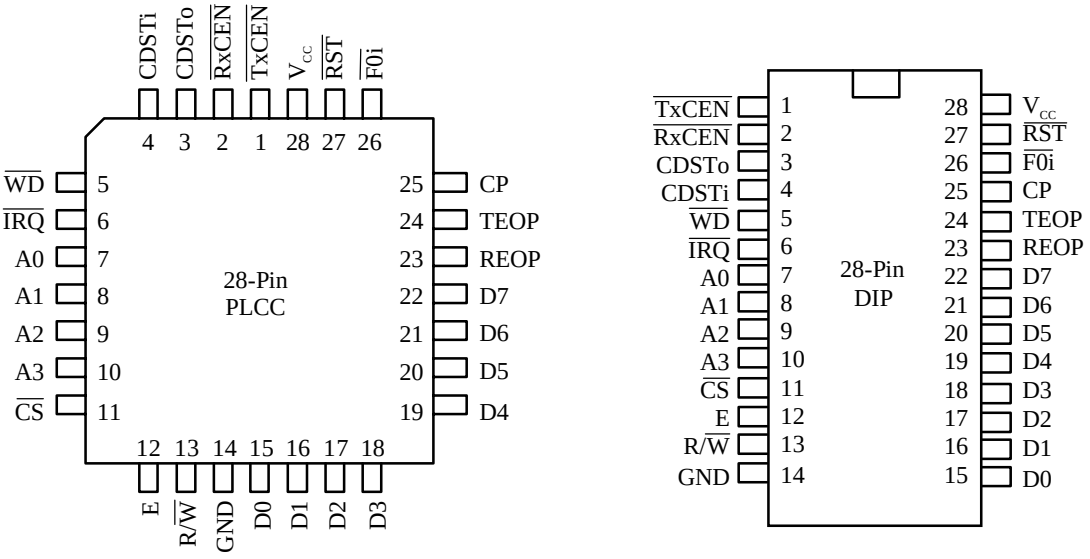
Pin Assignment

Table 1. Pin Assignment

Group	Symbol	Function
Chip Clock	$\overline{F0i}$, CP	Clock
Power & Ground	GND, Vcc	Power
Microprocessor Interface	D0-D7, A0-A3, $\overline{TxCEN}$, $\overline{RxCEN}$, E, $\overline{CS}$, $\overline{IRQ}$, $\overline{WD}$, R/$\overline{W}$, REOP, TEOP, $\overline{RST}$	Control, Data, or Address
Serial Interface	CDSTo, CDSTi	Serial Data

Pin Configuration

Figure 2. Pin Configuration



Top View

Pin Description

Table 2. Pin Description

Pin	Name	Type	Description
1	$\overline{\text{TxCEN}}$	I	**Transmit Control Enable**. In the External Timing Mode, CDSTo is enabled when this pin is LOW. A HIGH level present at this pin would put CDSTo in high impedance state. In the Internal Timing Mode, this input is ignored.
2	$\overline{\text{RxCEN}}$	I	**Receive Control Enable.** In the External Timing Mode, a low level at this pin would enable CDSTi .When the level is HIGH, CDSTi is inhibited. In the Internal Timing Mode, this input is ignored.
3	CDSTo	O	**C and D Channel Transmit Data**. In the Internal Timing Mode, the data is output from the device via the pin according to the ST-Bus format. D channel data would go out in any selected timeslots except timeslot 1. C channel data would go out only in timeslot 1. In the External Timing Mode, packeted data would go out from this pin on the rising edge of the clock CP when $\overline{\text{TxCEN}}$ is LOW. If $\overline{\text{TxCEN}}$ is HIGH, CDSTo is in high impedance state.
4	CDSTi	I	**C and D Channel Receive Data.** In the Internal Timing Mode, the serial data on the ST-Bus is input to the device via the pin. D channel data is input in any selected timeslots except timeslot 1. C channel data is input only in timeslot 1. In External Timing Mode, when $\overline{\text{RxCEN}}$ is LOW, CDSTi data is sampled on the falling edge of the clock CP. If $\overline{\text{RxCEN}}$ is HIGH, CDSTi is inhibited.
5	$\overline{\text{WD}}$	O	**Watch-Dog Timer Output**. Normally output a HIGH level. Going LOW if the watchdog timer times out or if the external reset ($\overline{\text{RST}}$) is held LOW. The $\overline{\text{WD}}$ output remains LOW as long as $\overline{\text{RST}}$ is held LOW.
6	$\overline{\text{IRQ}}$	O	**Interrupt Request (Open Drain)**. When in LOW level, this pin notifies the microprocessor that an interrupt request from this device is present.It is effective only when the corresponding bits in the Interrupt Enable Register are programmed to acknowledge the interrupt. The source of interrupt is according to the setting in the Interrupt Flag Register.
7-10	A0-A3	I	**Address Bus**. It is the address bus of the microprocessor interface used to select various internal registers in conjunction with $\overline{\text{CS}}$, R/$\overline{\text{W}}$ signals and E clock.
11	$\overline{\text{CS}}$	I	**Chip Select.** When in LOW level, this pin enables the Read or Write operation to the internal register of the device.
12	E	I	**Enable.** This Pin enables the followings : A0-A3, R/$\overline{\text{W}}$ and D0-D7.
13	R/$\overline{\text{W}}$	I	**Read/Write.** When this input is HIGH, the device is in read operation. When LOW, the device is in write operation.
14	GND	Power	**Ground (0 Volt)**
15-22	D0-D7	I/O	**Data Bus.** Data bus of the microprocessor interface.
23	REOP	O	**Receive End of Packet.** This pin would present a one bit wide positive pulse as either of the followings is detected: 1. Closing flag 2.abort flag 3. 24 bits (or more) of the invalid packets.

Table 2. Pin Description (Continued)

Pin	Name	Type	Description
24	TEOP	O	**Transmit End of Packet.** When transmission of the packet is closed (normal or abnormal close), this pin has one bit wide positive pulse output.
25	CP	I	**Data Clock.** This is the clock used for shifting in/out the serial data to/from the device. In the Internal Timing Mode, the BRCK bit in the Timing Control Register decides this clock either at the bit rate or twice the bit rate. In the External Timing Mode, the clock is at the bit rate only.
26	$\overline{F0i}$	I	**Frame Pulse.** In the Internal Timing Mode , this input is the Frame synchronous signal and the clock of the watchdog timer as well. In the External Timing Mode, this input is the clock of the watchdog timer only.
27	$\overline{RST}$	I	**Reset Signal (Schmitt Trigger).** When in LOW, it resets all the registers, including the transmit and receive FIFO registers and the watchdog timer.
28	V_{CC}	Power	**Power Supply (+5V).**

Functional Description

The functional diagram of the PT7A8952 is shown in figure 1. It has two kinds of interfaces, one is serial interface and another is microprocessor interface. The former is used to transceive data between the communication link, and the latter is used for the microprocessor to access the registers in the PT7A8952 .

The serial interface can be programmed to work in internal or external timing mode through IC bit of the Timing Control Register. In internal timing mode, it transfers data packet in selected timeslot according to ST-BUS format. In external mode, it transfers data at the same rate as the clock CP by using the enable signals ($\overline{\text{TxCEN}}$ & $\overline{\text{RxCEN}}$) .

The microprocessor interface contains the following pins : D0-D7, A0-A3, E, $\overline{\text{CS}}$ and R/$\overline{\text{W}}$. The microprocessor can access various registers through this interface. The addresses of these registers are given in Table 3.

$\overline{\text{IRQ}}$ is an open drain output. When in LOW level, it notifies the microprocessor that there is an interrupt request. The level of $\overline{\text{IRQ}}$ is controlled by both the Interrupt Flag Register and Interrupt Enable Register. This not only requires the associated bit of interrupt flag register to be 1, but also requires the corresponding bit of Interrupt Enable Register to be 1 to generate a LOW level at $\overline{\text{IRQ}}$. When $\overline{\text{IRQ}}$ is in LOW level, IRQ bit of status register is 1. When $\overline{\text{IRQ}}$ is in High level, IRQ bit of status register is 0.

Table 3. Register Addresses

Address Bits				Registers	
A3	A2	A1	A0	Read	Write
0	0	0	0	FIFO Status Register	-
0	0	0	1	Receive FIFO Register	Transmit FIFO Register
0	0	1	0	Control Register	Control Register
0	0	1	1	Receive Address Register	Receive Address Register
0	1	0	0	C-Channel Transmit Register	C-Channel Transmit Register
0	1	0	1	Timing Control Register	Timing Control Register
0	1	1	0	Interrupt Flag Register	Watchdog Timer Register
0	1	1	1	Interrupt Mask Register	Interrupt Enable Register
1	0	0	0	Status Register	-
1	0	0	1	C-Channel Receive Register	C-Channel Receive Register
1	1	0	0	-	Transmit Valid Channel Register
1	1	1	0	-	Receive Valid Channel Register
1	1	1	1	-	FIFO Length Control Register

HDLC Frame Format

Except in transparent mode, all data packets start with an opening flag and end with a closing flag. Between these two flags contained is the data field and Frame Check Sequence (FCS), which should be at least 32 bits in length (at least 16 bits data field and 16 bits FCS). Any data packets less than 32 bits are considered as invalid packets. During receiving, any data packet with length less than 24 bits between flags will be ignored. For the packet in length of 24-32 bits between flags, the PT7A8952 will deposit the data field in the receive FIFO and indicate it as bad FCS in FIFO status registers.

Table 4. Data Packet Format

Opening Flag	**Data Field**	**FCS**	**Closing** Flag
One Byte	n Bytes ($n \geq 2$)	Two Bytes	One Byte

Flag

The Opening Flag and the Closing Flag are 8 bits (01111110), which define the data packet boundary. They are generated automatically and added to the data packet during transmission. On receiving side, they are checked on a bit-by-bit basis on the incoming data packet and are used to establish receive synchronization. As they are only used to identify and synchronize the received data packet, they are not present in the transmit and receive FIFO.

Data Field

For a valid data packet, the length of its data field is at least 16 bits. The first byte in the data field is the address of the data packet. If RxAD bit in the Control Register is 1, the received data packet is recognized only when the data packet address matches the content in the Receive Address Register or the data packet address is the All-Call Address (all Ones). The lowest bit of the Receive Address Register is always 0. If the bit RA6/7 of the Control Registers is 0, the address detection will only be performed on the upper seven bits. If the bit RA6/7 of the Control Register is 1, only the upper six bits are used for address detection.

Frame Check Sequence (FCS)

The 16 bits following the data field are the Frame Check Sequence bits. The generator polynomial is:

$$G(X) = X^{16}+X^{12}+X^{5}+1$$

During transmitting, after calculating all the bits of the data field by this formula, the PT7A8952 inserts the calculated FCS into the data packet before the closing flag. During receiving, the PT7A8952 performs similar computation to the received data field and FCS, and then compares the result with the value F0B8 (Hex). If matched, the received data is assumed to be error free. If not, there are errors in the received data, and the error status is indicated by D7 and D6 bits in the FIFO status Register.

Zero Insertion and Deletion

During transmitting, the PT7A8952 will automatically inserts a ZERO after every five continuous ONEs to the out going data stream (including the last five bits of FCS) to ensure that no other data field in the bit stream would be mixed up with the Opening and Closing flags. Similarly, it will delete the zero following the five continuous ONEs to resume the original data pattern.

Channel State

When the PT7A8952 has no data packet to transmit, it will work in one of the following three channel states: Channel Idle State, Interframe Fill State and Go Ahead State. In which state the PT7A8952 works dependents on IFTF0 and IFTF1 bits in the Control Register. These two bits are also used to select transparent data transmit state in which all the protocol will be forbidden. The meaning of each state is shown in Table 5.

Timing Modes

There are two timing modes, Internal Timing Mode and External Timing Mode.

Internal Timing Mode

In Internal Timing Mode, the data is transmitted in ST-BUS format synchronized by Frame Sync. signals $\overline{F0i}$ and Clock CP. The PT7A8952 reserves one channel (Channel 1) for carrying control information (C-channel). The data can be transferred only in some specific timeslot and in some specific bits in each timeslot which are defined by TC0-TC3 bits of Timing Control Register and the values of D4~D0 bits of Transmit/ Receive Valid Channel Register. The BRCK bit of Timing Control Register is used to select the rate of CP clock (see Table 6). In this mode, the pins $\overline{TxCEN}$ and $\overline{RxCEN}$ are invalid.

Table 5. Channel State

IFTF1	IFTF0	State	State Sequence	Description
0	0	Idle State	More or Equal 15 Continuous Ones	After the chip detects the Idle state sequence in receiving the data, it will set the Idle Bit in the status Register as 1. On the transmission side, if the chip is in the idle state, it will send continuously the idle state sequence until data is loaded into the transmit FIFO register to end this state.
0	1	Interframe Fill State	7E(Hex)	If the chip is in the Interframe Fill state, it will send continuously to CDSTo the interframe fill state until data is loaded into the transmit FIFO register to end this state.
1	0	Transparent Data Transfer State		In this state, the chip will disable the above described protocol function. The device no longer sends various flags and sequences, adds 0 and calculates FCS. The chip only sends directly the content in the Transmit FIFO. The last byte or part of it loaded in the Transmit FIFO will be sent repeatedly. Meanwhile, during receiving, the data received from CDSTi will not contain the protocols of various sequences and flags, etc. The received data is loaded directly into the Receive FIFO. This state can work in two kinds of timing modes. However, it cannot work in the situation of Timing Control Bits being set as 1 bit per frame in the internal timing mode.
1	1	Go Ahead State	011111110 (7F(Hex) Adds One Zero)	If the chip is in the Go Ahead state, it will send continuously to CDSTo the go ahead sequence. This state will not change even when there is data being loaded into the transmit FIFO. This state can only be ended by setting the IFTF0 and IFTF1 bits in the Control Register to reselect other states. During receiving, after detecting the go ahead state sequence, the device sets the GA bit of the Status Register as 1. If the GA bit of the Interrupt Enable Register is 1 (agrees to interrupt), it will generate an interrupt by setting $\overline{IRQ}$ to LOW.

Table 6. Bit Rate in Internal Timing Mode

BRCK Bit	CP Input	Bit Rate
0	4.096MHz / $\overline{C4i}$	2.048 Mb/s
1	2.048 MHz / C2i	2.048 Mb/s

External Timing Mode

In External Timing Mode, the data transfer rate is equal to CP clock rate under controlled of $\overline{\text{TxCEN}}$ and $\overline{\text{RxCEN}}$. The data is transmitted on the rising edge of the CP clock and received on the falling edge of the CP clock. $\overline{\text{TxCEN}}$ and $\overline{\text{RxCEN}}$ are valid only after the transmission/receiving of the current bit of data is finished.

Watchdog Timer

The chip has an eleven-bit binary counter with $\overline{\text{F0i}}$ as the input and $\overline{\text{WD}}$ as the output. This timer has two ways to reset, (1) external reset (2) software reset by writing xxx01010 to the Watchdog Timer Register. The $\overline{\text{WD}}$ output is normally HIGH. If xxx01010 is not written to the Watchdog Timer Register again within 2^{10} cycles of $\overline{\text{F0i}}$, the $\overline{\text{WD}}$ output will go LOW for a period of 2^{10} cycles of $\overline{\text{F0i}}$. No matter in which timing mode, the operation of $\overline{\text{F0i}}$ to the Watchdog Timer is always effective.

Registers

There are many registers in the chip, they can be accessed by microprocessor to change operation of the device. The addresses of them are given in table 3, and the function details of them are described below.

Status Register (Read)

This register (Table 7) contains the general status information of the chip.

FIFO Length Control Register (Write)

Only D0, D1 bits in this register are useful, they are used to define the length of the transmit/receive FIFO register. The content of this register controls the FIFO operation with the concerned bit of FIFO status register and interrupt flag register together. Refer to Table 8 for details.

FIFO Status Register (Read)

The FIFO Status Register and FIFO Length Control Register (Table 8) indicate the status of transmit/receive FIFO and the status of the current received byte.

Table 7. Status Register (Read)

Bit	Name	Description
D7	RxOFLW Receives FIFO Overflow	This bit is set to 1 to indicate that the Receive FIFO is being overflowed. All the bytes causing this overflow and the following bytes will be lost. This bit and the RxOFLW bit of the Interrupt Flag Register are same and they can be cleared only through reading the Interrupt Flag Register.
D6	TxURUN Transmits FIFO Underrun	This bit is set to 1 to indicate that the Transmit FIFO Register is being underrun. Under this condition, the packet will be aborted by the device. This bit and the TxURUN of the Interrupt Flag Register are same which can be cleared only through reading the Interrupt Flag Register.
D5	GA Go Ahead	The bit is set to 1 to indicate that the chip has detected the Go Ahead state sequence from the received data at CDSTi. This bit and GA bit in the Interrupt Flag Register are the same and they can be reset only through reading the Interrupt Flag Register.
D4	ABRT Abnormal Closing	This bit is set to 1 when the chip detects the abnormal closing sequence from the received data at CDSTi. Under this condition, the chip will begin to search the Opening Flag. Reading the Status Register will reset this bit.
D3	IRQ Interrupt Request	This bit is the reverse of $\overline{\text{IRQ}}$. When it is 1, $\overline{\text{IRQ}}$ is in the Low level. When it is 0, $\overline{\text{IRQ}}$ is in the High level.
D2	IDLE Idle State	This bit is set to 1 when the chip detects the idle state sequence from the received data at CDSTi. It can be reset only by reading the Status Register.
D1-D0	Low High	0-1

Table 8. FIFO Status Register

Bit	Name	Value	Status	FIFO length control Register D1-D0	Description
D7-D6	Receive Byte Status	0 0	Data Packet Byte		The two bits indicate the status of the byte that is ready to be read from the receive FIFO register.
		0 1	First Byte		
		1 0	Last Byte (Good FCS)		
		1 1	Last Byte (Bad FCS)		
D5-D4	Receive FIFO Register Status	0 0	Vacant		Receive FIFO register (vacant).
		0 1	≤14 Byte	0 0	The two bits and the D1~D0 bits of the FIFO length control register indicate the status of bytes remained in the RFIFO.
			≤112 Bytes	0 1	
			≤96 Bytes	1 0	
			≤64 Bytes	1 1	
		1 0	≥19 Bytes	0 0	Receive FIFO register (full).
			≥128 Bytes	Other values except 0 0	
		1 1	≥15 Bytes	0 0	The two bits and the D1~D0 bits of the FIFO length control register indicate the status of bytes remained in the RFIFO.
			≥113 Bytes	0 1	
			≥97 Bytes	1 0	
			≥65 Bytes	1 1	
D3-D2	Transmit FIFO Register Status	0 0	≥19 Bytes	0 0	Transmit FIFO register (full)
			≥128 Bytes	Other values except 0 0	
		0 1	≥5 Bytes	0 0	The two bits and the D1~D0 bits of the FIFO length control register indicate the status of bytes remained in the TFIFO
			≥16 Bytes	0 1	
			≥32 Bytes	1 0	
			≥64 Bytes	1 1	
		1 0	Vacant		Transmit FIFO register (vacant)
		1 1	≤4 Bytes	0 0	The two bits and the D1~D0 bits of the FIFO length control register indicate the status of bytes remained in the TFIFO
			≤15 Bytes	0 1	
			≤31 Bytes	1 0	
			≤63 Bytes	1 1	
D1-D0		0 0	-	-	

Control Register (Read/Write)

The bits and their respective functions in the Control Register are described below.

Table 9. Control Register

Bit	Name	Description
D7	TxEN Transmit Enable	Setting this bit to 1 will enable the transmitter. Otherwise, the CDSTo will be put in the high impedance state. If this bit is set to 0 during transmission of a packet, CDSTo will not be in the high impedance state until the transmission of the whole data packet is finished with either closing flag or the abnormal closing sequence. If this bit is set from 1 to 0 with the chip in transparent data transfer state, the CDSTo will be put in the high impedance state within two bit periods (maximum).
D6	RxEN Receive Enable	Setting this bit to 1 will enable the receiver. If this bit is set from 1 to 0 during receiving of a packet, the receiver will not be disabled until the receiving of the whole data packet is finished with the closing flag or the abnormal closing sequence. If this bit is set from 1 to 0 with the chip in transparent data transfer state, the receiver will be disabled immediately.
D5	RxAD Receive Address Detect	Setting this bit to 1 will enable the single byte address detection for the received data packet. The data packet is received only when the received data packet address matches with the content in the Receive Address Register or the received address is the ALL-CALL Address (all ONEs). When this bit is set to 0, the single byte address detection will be disabled. So every valid packet will be received.
D4	RA6/7 Receive Address Six/Seven bits	Setting this bit to 1 will limit the single byte address detection only to the upper six bits of the data packet address, and the all ONE address only means the address in the upper six bits is 1. When set to 0, the chip compares the upper seven bits of the incoming data packet address. If the single byte address detection is forbidden (RxAD=0), RA6/7 will be invalid.
D3-D2	IFTF1-IFTF0	These are state selection bits. One can select freely the channel state and transparent data transmission state through these two bits: IFTF1=0, IFTF0=0: Idle State; IFTF1=0, IFTF0=1: Interframe Fill State; IFTF1=1, IFTF0=0: Transparent Data Transmission State; IFTF1=1, IFTF0=1: Go-Ahead State.
D1	FA Data Packet Abnormal Closing	When setting to 1, this bit will cause the device to "mark" the next byte which will be written into the transmit FIFO. Then, the device will produce immediately an abnormal closing sequence (eight ONEs) instead of transmitting the "marked" byte when this data byte reaches the bottom of the FIFO. Writing data to the transmit FIFO will reset the FA bit to 0.
D0	EOP Packet Closing	When setting at 1, this bit will "mark" the next byte which will be written into the transmit FIFO to indicate that this byte is the last byte of the data packet. Writing data to the transmit FIFO will reset the EOP bit to 0.

Receive FIFO Register (Read)

Reading from the Receive FIFO Register (Table 10) is to take a byte from the bottom of the Receive FIFO. When receiving, the first bit of the data received from CDSTi input is considered as the lowest bit, so it acts as the D0.

Table 10. Receive FIFO Register

D7	D6	D5	D4	D3	D2	D1	D0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Transmit FIFO Register (Write)

Writing to the Transmit FIFO Register (Table 11) is to write the data on the top of the transmit FIFO. When transmitting, the D0 bit of the byte at the bottom of the Transmit FIFO is transmitted firstly to CDSTo output.

Table 11. Transmit FIFO Register

D7	D6	D5	D4	D3	D2	D1	D0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Receive Address Register (Read / Write)

This register defines the address of the receiving data packet. If the RxAD bit of the Control Register enables the Single Byte Address Detection function, and the address of the incoming data packet (whether seven or six highest effective bits depends on the state of the bit RA6/7) matches the content of this register or it is ALL-CALL Address, the data packet will be recognized.

Table 12. Receive Address Register

D7	D6	D5	D4	D3	D2	D1	D0
RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0

C-Channel Transmit Register (Read / Write)

This register is active only in Internal Timing Mode. When the C1EN bit of the Timing Control Register enables the C-Channel transmit function of the device, the content of this register (Table 13) will be transmitted in timeslot 1 on the CDSTo.

Table 13. C-Channel Transmit Register

D7	D6	D5	D4	D3	D2	D1	D0
CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Timing Control Register (Read / Write)

This register is used to select the timing mode and its related operation, or to provide a software reset to the chip. The functions of various bits in this register are described below (Table 14 and Table 15).

Watchdog Timer Register (Write)

The relation among Watchdog Timer Register, Watchdog Timer and $\overline{WD}$ is: writing xxx01010 to the Watchdog Timer Register will reset the Watchdog Timer.

After resetting the Watchdog Timer, if this register is not rewritten within 2^{10} cycles of $\overline{F0i}$, $\overline{WD}$ output will go LOW.

Interrupt Enable Register (Read/Write)

Each bit of this register and the Interrupt Flag Register is corresponding one to one (see Table 17 for details). It is used to enable/disable the corresponding interrupts.

If any bit in this register is 1, it will enable the corresponding interrupt. Similarly, when this bit is 0, it will disable the corresponding interrupt. However, this disabled interrupt is still active inside the device and cannot cause the IRQ to LOW.

C-Channel Receive Register (Read)

C-Channel Receive Register (Table 16) is active only in the internal timing mode. The data of timeslot 1 received from CDSTi input are stored in this register and are updated continuously.

Table 16. C-Channel Receive Register

D7	D6	D5	D4	D3	D2	D1	D0
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Table 14. Timing Control Bit

Timing Control Bits				ST-BUS Transmit Channel Number	ST-BUS Receive Channel Number	Bits/Frame
TC3	TC2	TC1	TC0	D4-D0	D4-D0	
x	0	0	0	0+m	0+n	1
x	0	0	1	0+m	0+n	2
0	0	1	0	0+m	0+n	6
1	0	1	0	0+m	0+n	7
x	0	1	1	2+m	2+n	8
x	1	0	0	3+m	3+n	8
x	1	0	1	4+m	4+n	8
x	1	1	0	2+m, 3+m	2+n, 3+n	16
x	1	1	1	2+m, 3+m, 4+m	2+n, 3+n, 4+n	24

Legend: x : arbitrary
m: the D4-D0 value of Transmit Valid Channel Register
n: the D4-D0 value of Receive Valid Channel Register

Table 15. Timing Control Register

Bit	Name	Description
D7	RST Reset	When 1, this bit resets all the registers in the chip and the data in the Transmit/Receive FIFO are lost. This is similar to the external reset with exception that this reset does not affect RST bit itself or the Watchdog Timer Register and $\overline{WD}$ output. When RST=0, this bit must be written into this register twice before the chip is removed from its reset state (see section of Reset Operation).
D6	IC Mode Control	When 1, the chip is in the Internal Timing Mode in which the data transmit sequence is controlled by clock signal CP and frame synchronous signal $\overline{F0i}$ (Figure 12). The data is transmitted only in the timeslot specified by TC0-TC3 bits of this register and D0~D4 bits of transmit/receive valid register (Table14). When this bit is set to 0, the chip is in the External Timing Mode. The data transmission and reception are controlled by $\overline{TxCEN}$ and $\overline{RxCEN}$ respectively, and $\overline{F0i}$ is only used for the clock of the Watchdog Timer.
D5	CIEN C-Channel Enable	Only effective in the Internal Timing Mode. when set to 1, this bit enables C-Channel data transmission, during which the data in the C-Channel Transmit Register is put on the CDSTo on the timeslot 1. When set to 0, CDSTo enters high impedance state on timeslot 1. When receiving, the data in timeslot 1 is received independently and sent to the C-Channel Receive Register. So this Register is updated continuously.
D4	BRCK Bit Rate Clock	Only effective in the Internal Timing Mode. This bit is used to select CP clock rate. When set to 1, CP clock rate is the same as the bit rate. When set to 0, CP clock rate is twice the bit rate. In both cases, the phase relation of CP clock and $\overline{F0i}$ is shown in Figure 12.
D3-D0	TC0-TC3 Timing Control Bits	These bits specify the timeslot and the number of bits to be transmitted and received on the ST-BUS according to Table14. The receive channel number and bits/frame are specified by TC0~TC3 of Timing Control Register and D4~D0 bits of the Receive valid Register, while the transmit channel number and bits/frame are specified by TC0~TC3 of Timing Control Register and D4~D0 bits of the Transmit valid Register. In other unspecified channels, no data is read from CDSTi and CDSTo is put in the high impedance state.

Table 17. Interrupt Flag Register

Bit	Name	Status	FIFO Length Control Register D1-D0	Description
D7	GA Go-Ahead Signal			When 1, indicates that the Go-ahead status sequence detected from the received data of the CDSTi.
D6	EOPD Packet Closing Signal			When 1, indicates the Closing Flag or Abnormal Closing sequence, or a invalid packet constituted of 24 or more bits detected from the received data of the CDSTi.
D5	TxDONE Transmit Done Signal			When 1, indicates data packet transmission ended. When the Transmit FIFO Register is empty, the falling edge of TEOP output makes this bit to 1.
D4	FA Data Packet Abnormal Closing			When 1, it means the chip has detected an Abnormal Closing sequence after receiving the Opening Flag following at least 4 bytes (least valid packet).
D3	Tx Transmit FIFO Register status	Tx 4/19 Full	0 0	When this bit is 1 and D1~D0=00 (FIFO length control Register), it means there are only 4 bytes remained in Transmit FIFO and the FIFO can receive up to 15 bytes more from microprocessor.
		Tx 15/128 Full	0 1	When this bit is 1 and D1~D0=01 (FIFO length control Register), it means there are only 15 bytes remained in Transmit FIFO and the FIFO can receive up to 113 bytes more from microprocessor.
		Tx 31/128 Full	1 0	When this bit is 1 and D1~D0=10 (FIFO length control Register), it means there are only 31 bytes remained in Transmit FIFO and the FIFO can receive up to 97 bytes more from microprocesor.
		Tx 63/128 Full	1 1	When this bit is 1 and D1~D0=11 (FIFO length control Register), it means there are only 63 bytes remained in Transmit FIFO and the FIFO can receive up to 65 bytes more from microprocessor.
D2	TxURUN Transmit FIFO Underrun			When 1, it indicates that Transmit FIFO is empty, but the indication of end of data packet is not given by the microprocessor.At this time the chip will automatically transmit an Abnormal Closing sequence.After TxURUN is 1,TxDONE will be set to 1 for 8-bit time.
D1	Rx Receive FIFO Register status	Rx 15/19 Full	0 0	When this bit is 1 and D1~D0=00 (FIFO length control Register), it means Receive FIFO Register has 15 bytes and can only receive 4 bytes more.
		Rx 113/128 Full	0 1	When this bit is 1 and D1~D0=01 (FIFO length control Register), it means Receive FIFO Register has 113 bytes and can only receive 15 bytes more.
		Rx 97/128 Full	1 0	When this bit is 1 and D1~D0=10 (FIFO length control Register),it means Receive FIFO has 97 bytes and can only receive 31 bytes more.
		Rx 65/128 Full	1 1	When this bit is 1 and D1~D0=11 (FIFO length control Register), it means Receive FIFO has 65 bytes and can only receive 63 bytes more.
D0	RxOFLW Receive FIFO Overflow	≥19	0 0	When 1, it means Receive FIFO Register is full, and at this time more data is coming from CDSTi causing the RFIFO overflow. The bytes causing overflow and the bytes following will all be lost. The receiving circuit returns to detection of Opening Flag.
		≥128	Other values except 0 0	

Interrupt Flag Register (Read)

This register and FIFO Length Control Register indicate the status of Transmit/Receive FIFO. The functional details are provided in Table 17.

In order to avoid Underrun of the Transmit FIFO, the Transmit FIFO Full Interrupt is used to control the transmission. For example, if the D1-D0 bits of FIFO Length Control Register are 00, and there are only 4 bytes remained in the Transmit FIFO, 4/19 Full Interrupt is generated. The microprocessor has to write no more than 15 bytes to the Transmit FIFO before all bytes in the FIFO is run out. If a byte among these bytes is the last byte of a packet, EOP will be set in the Control Register to indicate this. So the chip will automatically insert the Closing Flag after this byte in the TFIFO.

To avoid Overflow of the Receive FIFO Register, Receive FIFO Full Interrupt is used to control the data packet reception. For example, when 15/19 Full Interrupt occurs, the Receive FIFO can hold 4 more bytes from the CDSTi. The microprocessor must read the data bytes out from the Receive FIFO immediately (Maximum 15 Bytes) to ensure room in Receive FIFO available to hold the incoming data.

Transmit Valid Channel Register (Write)

This register is effective only in the internal timing mode. Its F4-F0 value and the Timing Control Register TC3-TC0 bits define concurrently the timeslot and bit number of each frame, as shown in table 14. When TC3-TC0 = X101, F4-F0 = 00101, the timeslot number of the data transmission is 9, the bit number per frame is 8.

Table 18. Transmit Valid Channel Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	F4	F3	F2	F1	F0

Receive Valid Channel Register (Write)

This register works similarly to the Transmit Valid Channel Register except that it works on the receive side. Refer to Table 19.

Table 19. Receive Valid Channel Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	R4	R3	R2	R1	R0

Reset Operation

When $\overline{RST}$ goes low (external reset) or RST bit of the Timing Control Register is 1 (internal reset), the chip will enter immediately the following status:

All bits in the Timing Control Register are cleared (logic 0) by an external reset. All bits except RST bit in the Timing Control Register are cleared (logic 0) by an internal reset.
All bits in the Transmit/Receive Valid Channel Register are cleared (logic 0).
All bits in the Interrupt Enable Register are cleared (logic 0).
All bits in the Control Register are cleared ((logic 0).
All bits in the Interrupt Flag Register are cleared (logic 0).
Except two lowest effective bits, all bits in the Status Register are cleared (logic 0).
The pointers of the Receive and Transmit FIFO Register return to the start. At this time the FIFO Status Register reflects immediately their status.
The $\overline{WD}$ goes LOW if the watchdog timer times out or if the external reset ($\overline{RST}$) is held LOW. The $\overline{WD}$ output remains LOW as long as $\overline{RST}$ is held LOW. It is not affected by the internal reset.
The transmission and receiving are disabled.

Transmit Operation

Power-on will cause a hardware reset to the chip. At this time the transmit section is disabled and the chip is in External Timing Mode. After selecting a proper timing mode and enabling transmission, the chip will enter to one of the Channel States.

If the device is in Idle or Interframe Fill State, writing data into the Transmit FIFO via the Transmit FIFO Register will make the transmitter begin to transmit the data through the pin CDSTo. An Opening flag will be put prior to the first byte of the data packet.

If the current state is Go-ahead state, the PT7A8952 will not begin to transmit the data until the device is programmed to enter other state. If the chip is currently in the Transparent Data Transmit state, the data in the Transmit FIFO will be transmitted directly through CDSTo with the protocol function disabled.

For normal ending of transmission of the present data packet, the EOP bit of the Control Register must be set at 1 before writing the last byte of the data packet to the Transmit FIFO. Then the chip will attach the 16 bits Frame Check Sequence (FCS) and Closing Flag after the last byte of the data packet. If there is other data packet to be transmitted in the Transmit FIFO following the last byte of the previous packet, an Opening Flag will be transmitted first before transmitting the new data packet. If there is no data in the Transmit FIFO, the transmitter will return to the selected channel state. In the transmission of the data or Frame Check Sequence, the chip will check the transmitted data bit by bit, and insert one 0 when it meets five successive 1. The bit corresponding to D0 is to be transmitted first through CDSTo.

Receive Operation

After reset, the receiver is disabled and the chip is in External Timing Mode. The Single Byte Address Detection function is disabled as well. After receiving enabling and initialization, the data begin to be input to the Receive FIFO according to the clock rate through CDSTi. In this stage, the chip also begins to detect various state sequence and flag on the input data. If the device recognizes certain state sequence, it will show this state in the corresponding bits in the Status Registers.

If the chip recognizes the Opening Flag, it will begin to receive data. During receiving, the chip will delete the inserted 0 and count at the same time. The data of the incoming packet will be stored into the Receive FIFO, but FCS and flags will not be found in the Receive FIFO. If the Address Detection function of the device is enabled, the first byte following the Opening Flag will be compared with the byte in the Received Address Register. If the address is not matched, the whole data packet will be neglected. If the address is matched or the address is ALL-CALL address, the data packet will be received in the normal way; the first bit received is the LSB corresponding to D0 on the Data Bus.

Detailed Specifications

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) ... -0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) -0.3V to +7.0V
DC Input Voltage ..... -0.3V to +7.0V
DC Output Current 120mA
Power Dissipation 900mW

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Table 20. Recommended Operation Conditions

Sym	Description	Test Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage - except $\overline{RST}$ Pin	For a noise margin of 400 mV	2.8		V_{CC}	V
V_{IL}	Input LOW Voltage - except $\overline{RST}$ Pin	For a Noise Margin of 400 mV	0		0.4	V
V_{SIH}	Schmitt Input HIGH Voltage - $\overline{RST}$ Pin		4.2			V
V_{SIL}	Schmitt Input LOW Voltage - $\overline{RST}$ Pin				0.8	V
f_{CL}	Frequency of Operation	When clock input is at twice the bit rate			5.0	MHz
T_A	Operating Temperature		-40	25	85	°C

Note:
Typical figures are at 25°C and for design aid only; not production tested.

DC Electrical, Power Supply and Capacitance Characteristics

Table 21. DC Electrical, Power Supply and Capacitance Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage - except $\overline{RST}$ Pin		2.4			V
V_{IL}	Input LOW Voltage - except $\overline{RST}$ Pin				0.8	V
V_{T+}	HIGH Switching Point for Schmitt Trigger ($\overline{RST}$) pin			4.0		V
V_{T-}	Low Switching Point for Schmitt Trigger ($\overline{RST}$) Input			1.0		V
V_H	Hysteresis on Schmitt Trigger ($\overline{RST}$) Input			0.5		V
I_{ILK}	Input Leakage Current	V_{IN} = 0V or V_{IN} = 5V			10.0	µA
I_{OH}	Output HIGH Current (on All the Outputs Except $\overline{IRQ}$)	V_{OH} = 4V	-5	-16		mA
I_{OL}	Output LOW Current (on All the Outputs)	V_{OL} = 0.4V	5	10		mA
I_{CCQ}	Quiescent Supply Current	Outputs unloaded and clock input (CP) grounded		16	20	mA
I_{CC}	Supply Current	See Note 1.		29	35	mA
C_{IN}	Input Capacitance			8		pF
C_{OUT}	Output Capacitance			10		pF

Note:
1. Outputs unloaded. Input pins 12 and 25 clocked at 2.048 MHz. All other input pins connected to GND.
2. Typical figures are at 25ºC and are for design aid only; not production tested.

AC Electrical Characteristics

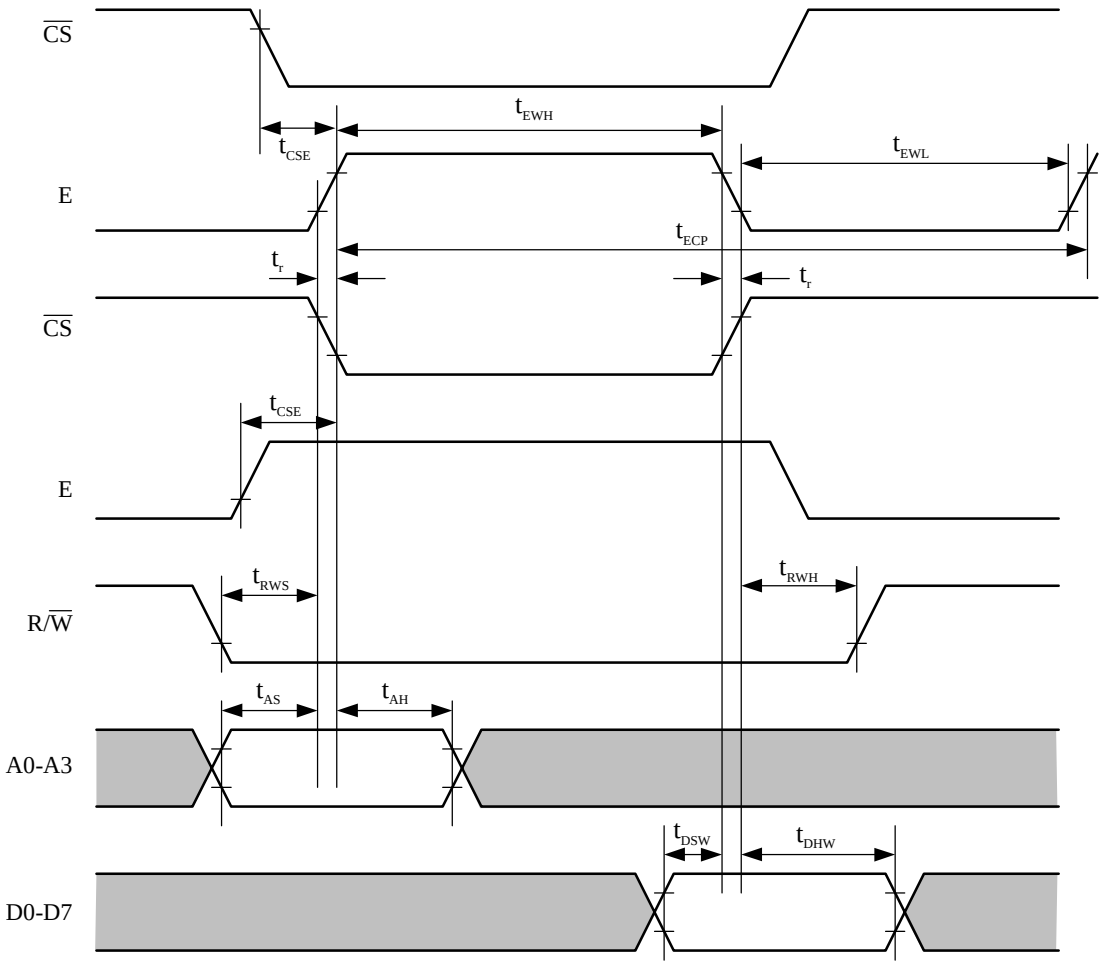
Microprocessor Interface

Table 22. Timing Characteristics of Microprocessor Interface

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{CSE}	Delay between $\overline{CS}$ and E Clock		0			ns
t_{ECP}	Cycle Time		205			ns
t_{EWH}	E Clock Pulse width HIGH		145			ns
t_{EWL}	E Clock Pulse width LOW		60			ns
t_{RWS}	Read/Write Setup Time		10			ns
t_{RWH}	Read/Write Hold Time		10			ns
t_{AS}	Address Setup Time		20			ns
t_{AH}	Address Hold Time		60			ns
t_{DSW}	Data Setup Time (Write)		35			ns
t_{DHW}	Data Hold Time (Write)		10			ns
t_{EDD}	E Clock to Valid Data Delay				145	ns
t_{DHR}	Data Hold Time (Read)		10		60	ns

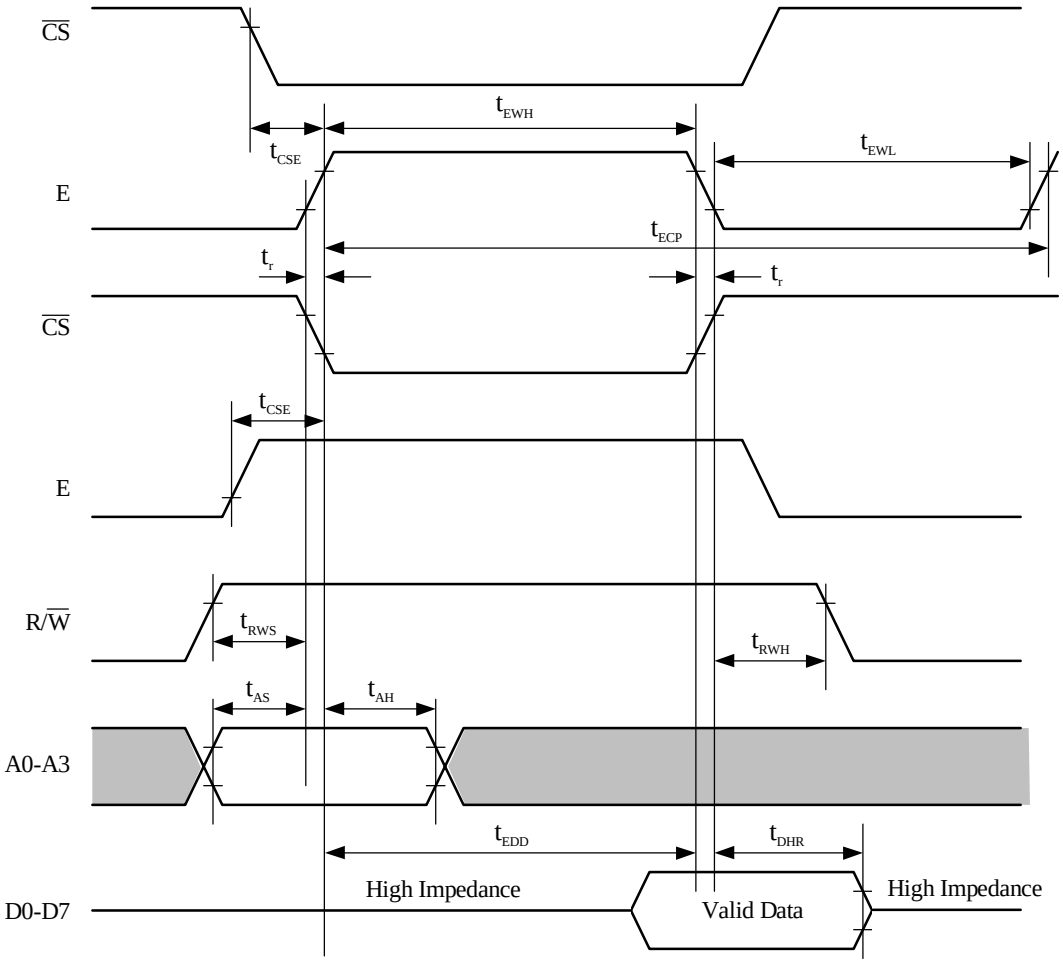
Note:
Typical figures are at 25ºC and are for design aid only; not production tested.

Figure 5. Timing Diagram of Microprocessor Write



Note:
The write cycle can be initiated either by the falling edge of $\overline{CS}$ or the rising edge of E clock whichever occurs last. Similarly the cycle can be terminated by $\overline{CS}$ (rising edge) or E clock (falling edge) whichever occurs first. The timing relations are to be referenced from two edges causing actually the initiation and termination of the clock cycle.

Figure 6. Timing Diagram of Microprocessor Read



Note:
The read cycle can be initiated by the falling edge of $\overline{CS}$ or the rising edge of E clock whichever occurs last. Similarly the cycle can be terminated by $\overline{CS}$ (rising edge) or E clock (falling edge) whichever occurs first. The timing relations are to be referenced from two edges causing actually the initiation and termination of the clock cycle.

Serial Port, RESET, $\overline{WD}$ Timer and $\overline{IRQ}$ Release Time

Table 23. Timing Characteristics of Serial Port, Reset, $\overline{WD}$ and $\overline{IRQ}$ Release Time

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{IRQR}	Interrupt Request Release Time				120	ns
t_{WDHL}	$\overline{WD}$ Output Delay HIGH to LOW				135	ns
t_{WDLH}	$\overline{WD}$ Output Delay LOW to HIGH				135	ns
t_{EOPD}	TEOP/REOP Output Delay				110	ns
t_{EOPH}	TEOP/REOP Output Hold Time				110	ns
t_{STOD}	CDSTo Delay from Clock				125	ns
t_{STIS}	CDSTi Setup Time		20			ns
t_{STIH}	CDSTi Hold Time		65			ns
t_{RST}	RESET Pulse Width			100		ns

Note:
Typical figures are at 25ºC and are for design aid only; not production tested.

Figure 7. Diagram of Interrupt Request Release Time

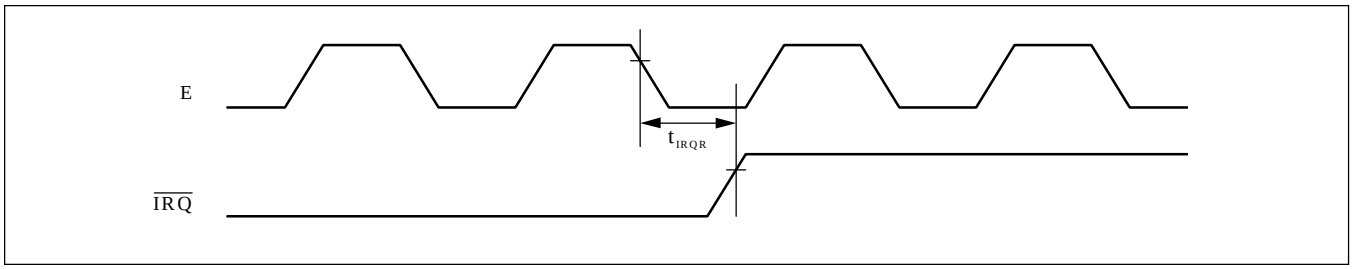


Figure 8. Timing Diagram of Watchdog Timer Input and Output

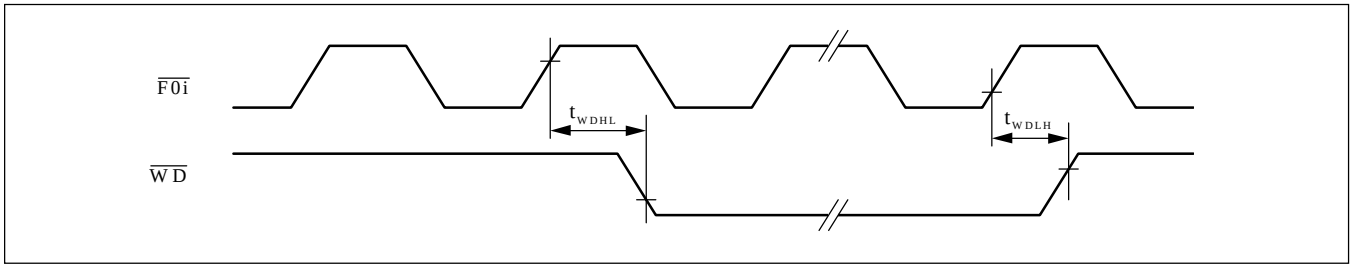


Figure 9. RESET Timing Diagram

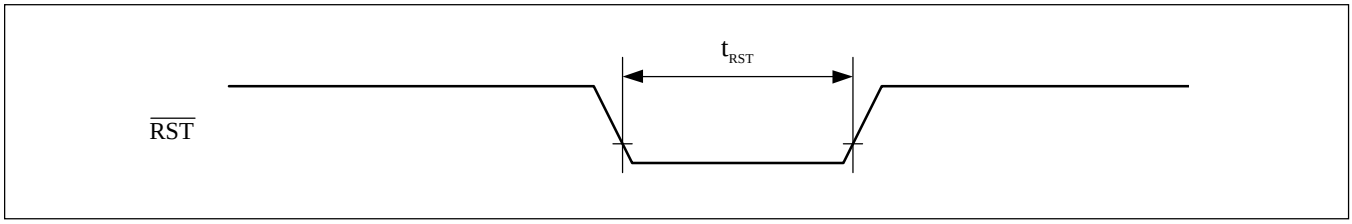
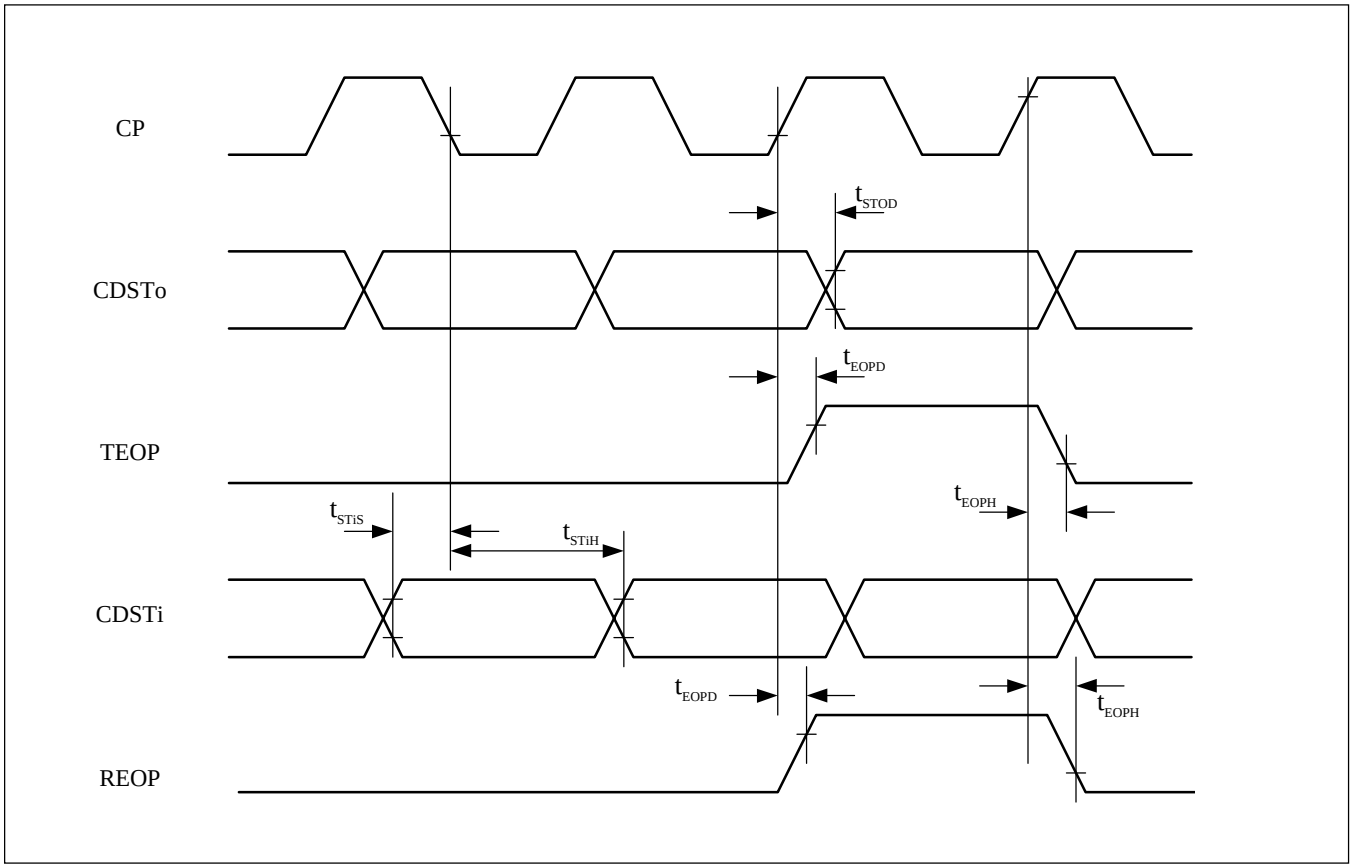


Figure 10. Timing Diagram of Serial Port Input and REOP, Output and TEOP



Note:
The frequency of the clock input CP is assumed to be at the output bit rate. However, it can be at twice the bit rate in the Internal Timing Mode.

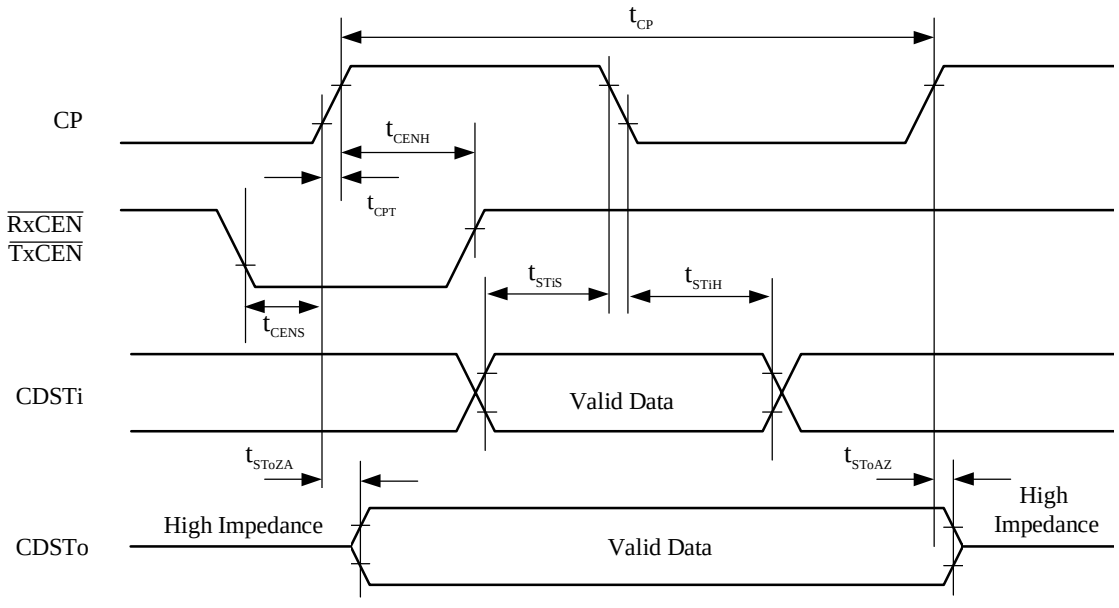
Serial Port in External Timing Mode

Table 24. Timing Characteristics of Serial Port in External Timing Mode

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{CP}	Clock Period on CP Pin		400			ns
t_{CPT}	CP Transition Time			20		ns
t_{CENS}	$\overline{TxCEN}$ and $\overline{RxCEN}$ Setup Time		60			ns
t_{CENH}	$\overline{TxCEN}$ and $\overline{RxCEN}$ Hold Time		40			ns
t_{STiS}	CDSTi Setup Time		20			ns
t_{STiH}	CDSTi Hold Time		65			ns
t_{SToZA}	CDSTo Delay				125	ns
t_{SToAZ}	CDSTo Disable Time				85	ns

Note:
Typical figures are at 25ºC and are for design aid only; not production tested.

Figure 11. Timing Diagram of Serial Port Inputs and Outputs in External Timing Mode



Note:
The frequency of the clock input CP should be at the output bit rate in the External Timing Mode.

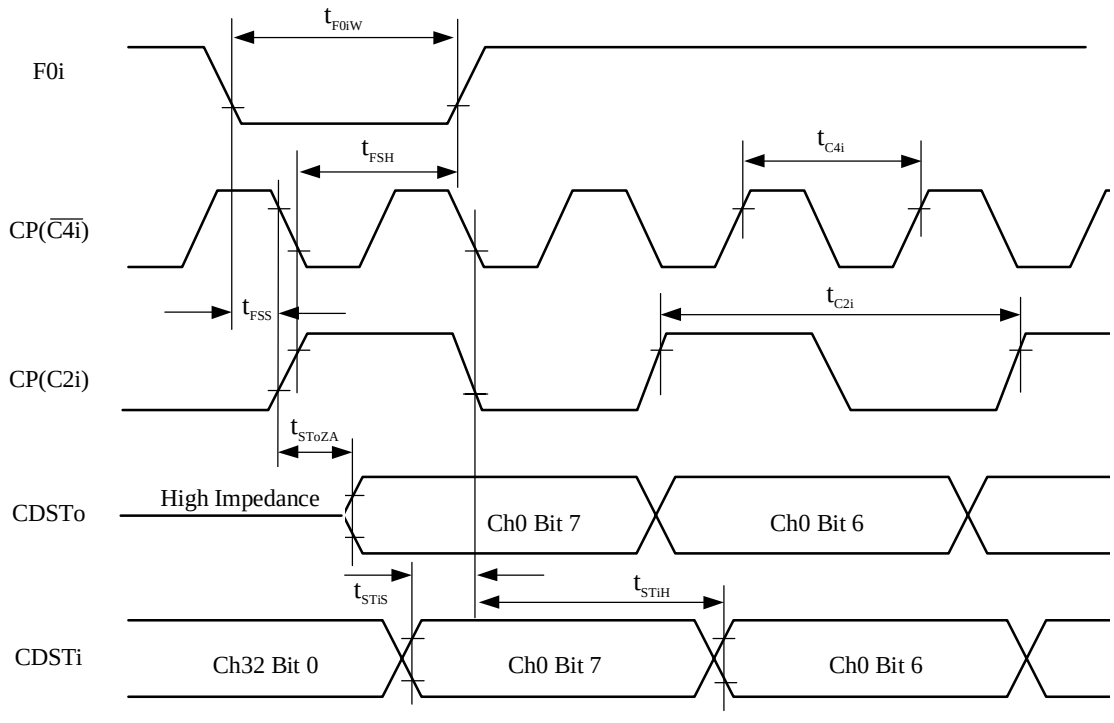
Serial Port in Internal Timing Mode

Table 25. Timing Characteristics of Serial Port in Internal Timing Mode

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{FOiW}	Frame Pulse ($\overline{F0i}$) width		90			ns
t_{FSS}	Frame Pulse ($\overline{F0i}$) setup time		30			ns
t_{FSH}	Frame Pulse ($\overline{F0i}$) hold time		60		125	ns
t_{SToZA}	CDSTo delay				125	ns
t_{STiS}	CDSTi setup time		20			ns
t_{STiH}	CDSTi hold time		65			ns
t_{C2i}	C2i clock period		400			ns
t_{C4i}	$\overline{C4i}$ clock period		200			ns

Note:
Typical figures are at 25ºC and are for design aid only; not production tested.

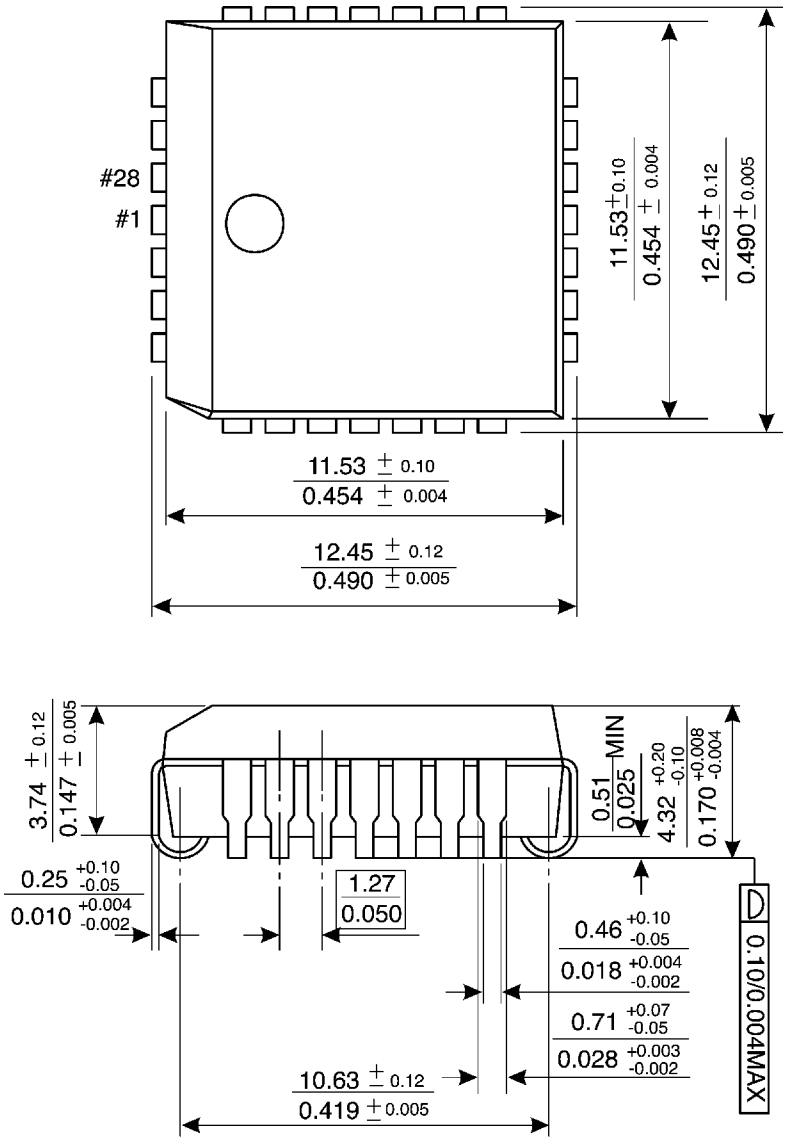
Figure 12.Timing Diagram of Serial Port Input and Output in ST-BUS Format (Internal Timing Mode)



Note:
Clock input CP can be either the ST-BUS clock C2i (2.048 MHz) or $\overline{C4i}$ (4.096MHz) in the Internal Timing Mode. The Frame Pulse setup and hold time measurements are to be referenced from the falling edge of $\overline{C4i}$ or the rising edge of C2i, depending on the present clock selected.

Mechanical Information

Figure 13. 28-Pin PLCC



Dimensions in Milimeters/Inches

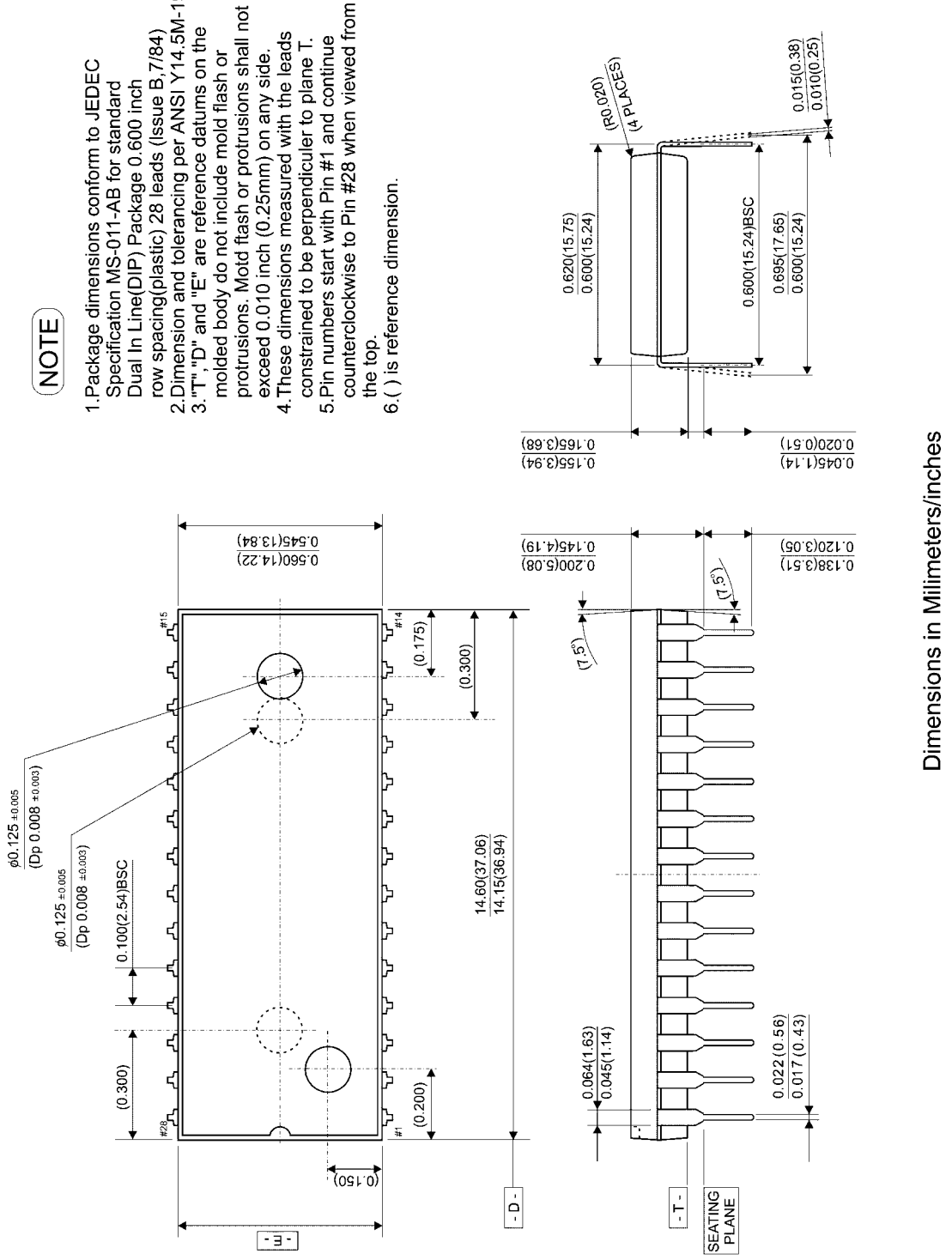


Figure 14. 28-Pin DIP

Ordering Information

Table 26. Ordering Information

Part Number	Package
PT7A8952J	28-Pin PLCC
PT7A8952P	28-Pin PDIP

Notes

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