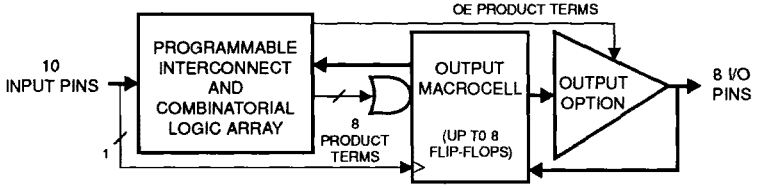
Features

- **High Speed Electrically Erasable Programmable Logic Device**
  - **7.5 ns Max Propagation Delay**
  - **5 ns Max From Clock to Data Output**
  - **F_{MAX} = 100 MHz**
  - **5 V ±10% Operation**
- **Low Power ATF16V8BL - 10 mA Standby**
- **Eight Output Logic Macrocells**
  - **Maximum Flexibility for Complex Logic Designs**
  - **Programmable Output Polarity**
  - **Emulates 20-pin PAL® Devices with Full Function/Fuse-Map/ Parametric Compatibility**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **150 µA Leakage Maximum**
  - **Active Pull-Ups on All Pins**
- **Reprogrammable - 100% Tested**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial and Industrial Temperature Ranges**
- **Dual-In-Line and Surface Mount Packages in Standard Pinouts**

Logic Diagram



Description

The ATF16V8B and ATF16V8BL are high performance CMOS Electrically Erasable Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full 5 V ±10% range for military and industrial temperature ranges and 5 V ±5% for commercial ranges.

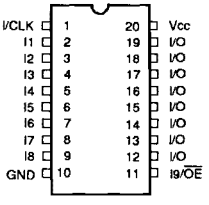
The ATF16V8BL provides the fastest low power CMOS PLD solution, with low DC current (5.0 mA typical). The ATF16V8BL significantly reduces total system power and enhances system reliability.

The generic architecture provides maximum design flexibility by allowing the output macrocell (OMC) to be configured by the user. An important subset of the many architecture configurations possible with the ATF16V8B/L is the PAL architectures listed in the table in the macrocell description section. ATF16V8B/L devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

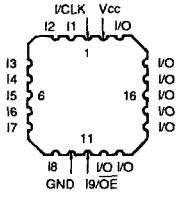
Pin Configurations

Pin Name	Function
I/CLK	Logic Input and Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
Vcc	+5 V Supply
I/$\overline{OE}$	Logic Input and Output Enable

DIP/SOIC



LCC/PLCC



High Performance Flash PLD

2

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

	Commercial ATF16V8B/L -7,-10, -15, -25	Industrial ATF16V8B/L -10, -15, -25	Military ATF16V8B/L -10, -15, -25
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}(1)	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)					150	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current	F_{IN} = 25 MHz, V_{CC} = MAX, Outputs Open, $V_{IL} \le 0.5$ V, $V_{IH} \ge 3.0$ V	ATF16V8B	Com.		80	120	mA
				Ind., Mil.		90	130	mA
			ATF16V8BL	Com.		5.0	10	mA
				Ind., Mil.		10	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	ATF16V8BL	Com.			15	mA/MHz
				Ind., Mil.			20	mA/MHz
I_{OS} (2)	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC}+0.75	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN	I_{OL} = 16 mA	Com.,Ind.			0.5	V
			I_{OL} = 12 mA	Mil.			0.5	V
			I_{OL} = 24 mA	Com.			0.8	V
V_{OH}	Output High Voltage	$V_{IN}=V_{IH}$ or V_{IL}, V_{CC}=MIN	I_{OH} = -100 µA		V_{CC}-0.3			V
			I_{OH} = -4.0 mA		2.4			V

Notes: 1. The leakage current is due to the internal pull-up resistors on all pins.
2. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

A.C. Characteristics, Commercial

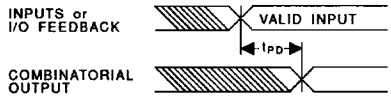
Symbol	Parameter	ATF16V8B -7		ATF16V8B/L -10		ATF16V8B/L -15		ATF16V8B/L -25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input or I/O to Combinatorial Output	3	7.5	3	10	3	15	3	25	ns
t_{CO}	Clock to Output Delay	2	5	2	7	2	10	2	12	ns
t_{CF}	Clock to Feedback Delay		3		6		8		10	ns
t_{SU}	Setup Time, Input or Feedback Before Clock	7		10		12		15		ns
t_H	Hold Time, Input or Feedback After Clock	0		0		0		0		ns
F_{MAX}	Maximum Clock Frequency with External Feedback $1/(t_{SU}+t_{CO})$	83.3		58.8		45.5		37		MHz
	Maximum Clock Frequency with Internal Feedback $1/(t_{SU}+t_{CF})$	100		62.5		50		40		MHz
	Maximum Clock Frequency with No Feedback	100		62.5		62.5		41.6		MHz
t_{WH}	Clock Pulse Duration, High	5		8		8		12		ns
t_{WL}	Clock Pulse Duration, Low	5		8		8		12		ns
t_{EA}	Input or I/O to Output Enable	3	9	3	10	3	15	3	25	ns
t_{ER}	Input or I/O to Output Disable	2	9	2	10	2	15	2	25	ns
t_{OEA}	OE to Output Enable	2	6	2	10	2	15	2	20	ns
t_{OER}	OE to Output Disable	1.5	6	1.5	10	1.5	15	1.5	20	ns

A.C. Characteristics, Industrial and Military

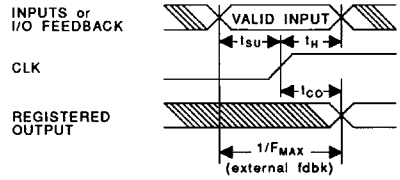
Symbol	Parameter	ATF16V8B/L -10		ATF16V8B/L -15		ATF16V8B/L -25		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Input or I/O to Combinatorial Output	3	10	3	15	3	25	ns
t_{CO}	Clock to Output Delay	2	7	2	10	2	12	ns
t_{CF}	Clock to Feedback Delay		6		8		10	ns
t_{SU}	Setup Time, Input or Feedback Before Clock	10		12		15		ns
t_H	Hold Time, Input or Feedback After Clock	0		0		0		ns
F_{MAX}	Maximum Clock Frequency with External Feedback $1/(t_{SU}+t_{CO})$	58.8		45.5		37		MHz
	Maximum Clock Frequency with Internal Feedback $1/(t_{SU}+t_{CF})$	62.5		50		40		MHz
	Maximum Clock Frequency with No Feedback	62.5		62.5		41.6		MHz
t_{WH}	Clock Pulse Duration, High	8		8		12		ns
t_{WL}	Clock Pulse Duration, Low	8		8		12		ns
t_{EA}	Input or I/O to Output Enable	3	10	3	15	3	25	ns
t_{ER}	Input or I/O to Output Disable	2	10	2	15	2	25	ns
t_{OEA}	OE to Ouput Enable	2	10	2	15	2	20	ns
t_{OER}	OE to Output Disable	1.5	10	1.5	15	1.5	20	ns

A.C. Waveforms

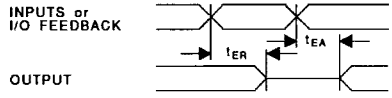
Combinatorial Output



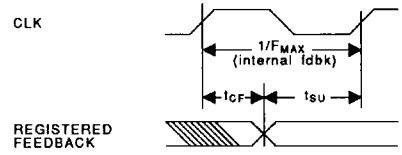
Registered Output



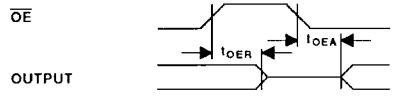
Input or I/O to Output Enable/Disable



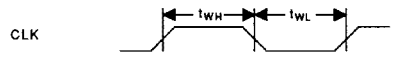
fMAX with Feedback



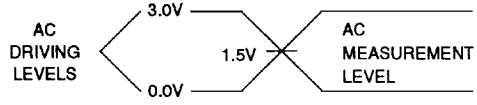
Output Enable to Output Enable/Disable



Clock Width

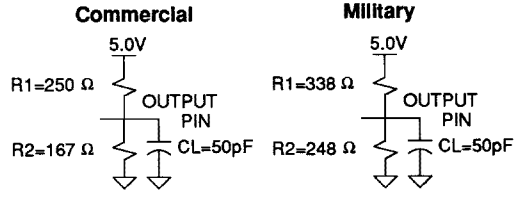


Input Test Waveforms and Measurement Levels



tR, tF < 3 ns (10% to 90%)

Output Test Loads



Output Macrocell

The following discussion pertains to configuring the output macrocell (OMC). It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OMC configuration modes possible: **simple, complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits control the mode configuration for all macrocells. A bit in each macrocell controls the polarity of the output in any of the three modes, while another bit in each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in an ATF16V8B/L. The information given on the architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architectures bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the ATF16V8B and ATF16V8BL can emulate. It also shows the OMC mode under which the ATF16V8B/L emulates the PAL architecture.

PAL Architectures Emulated by ATF16V8B/L	ATF16V8B/L Global OMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple

PAL Architectures Emulated by ATF16V8B/L	ATF16V8B/L Global OMC Mode
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

Macrocell Configuration

Software compilers support the three different OMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
Abel™	P16V8R	P16V8C	P16V8AS	P16V8
Cupl™	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC®	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD®-PLD	"Registered" (1)	"Complex" (1)	"Simple" (1)	GAL16V8A
PLDesigner™	P16V8R (2)	P16V8C (2)	P16V8C (2)	P16V8A
Tango-PLD™	G16V8R	G16V8C	G16V8AS (3)	G16V8

Note: 1. Used with **Configuration** keyword.
2. Prior to version 2.0 support.
3. Supported on version 1.20 or later.

Registered Mode

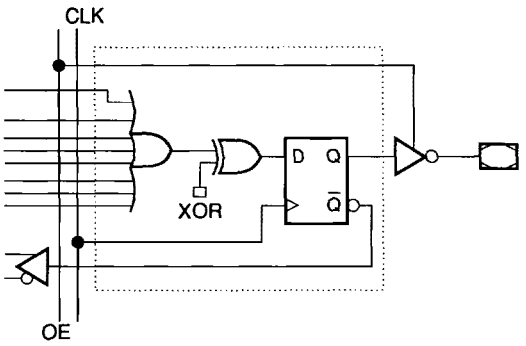
In the registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and registered placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or combinatorial I/O. Up to eight registers or up to eight I/Os are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

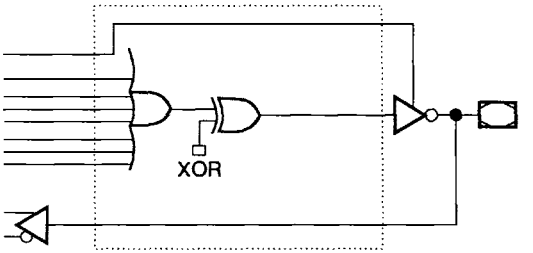
Registered outputs have eight product terms per output. I/Os have seven product terms per output.

Registered Configuration for Registered Mode (1,2)



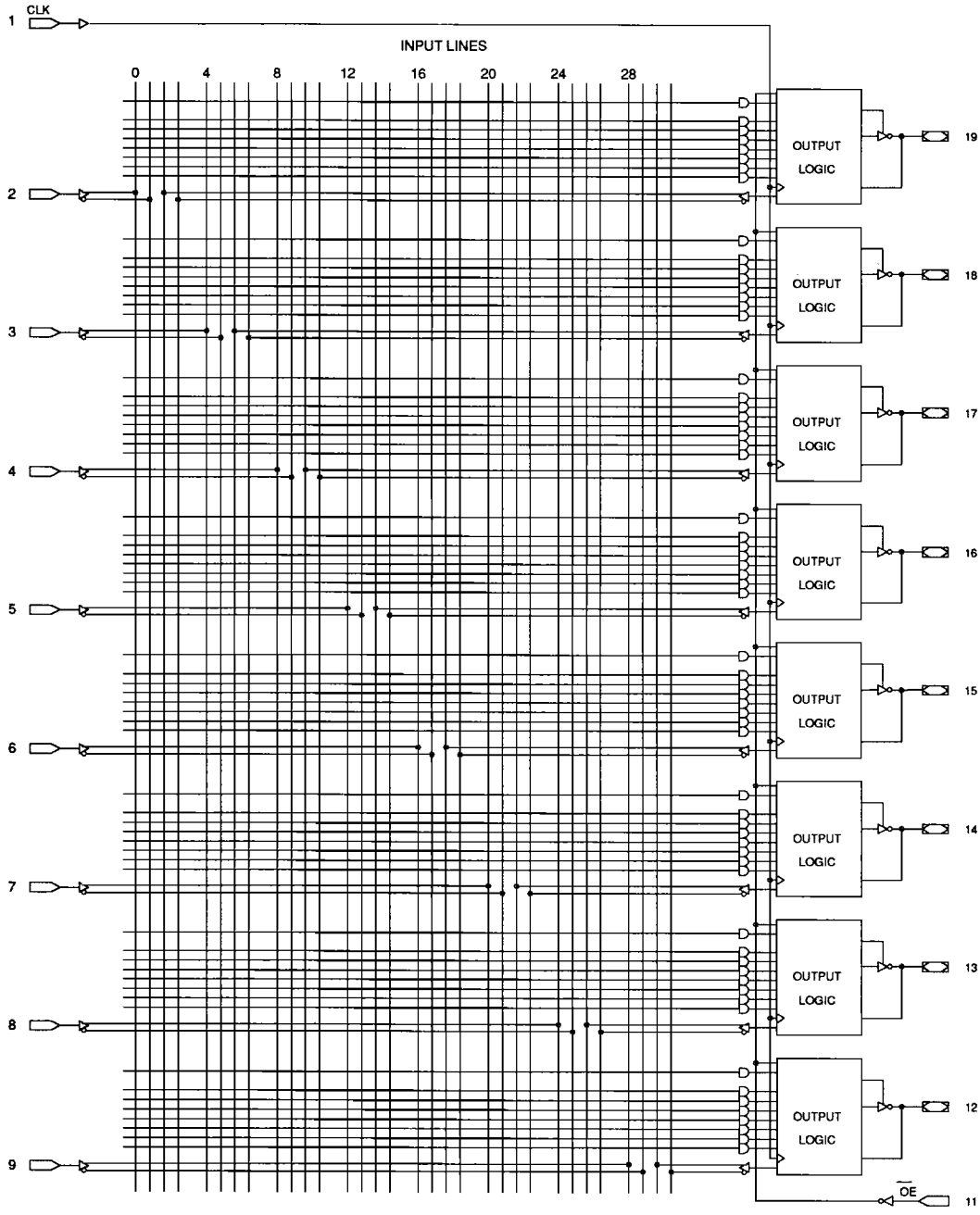
Notes:
1. Pin 1 controls common CLK for the registered outputs. Pin 11 controls common $\overline{OE}$ for the registered outputs. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Combinatorial Configuration for Registered Mode (1,2)



Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram



Complex Mode

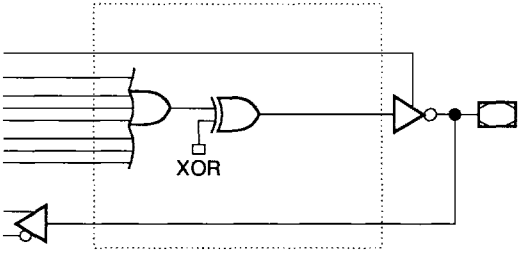
In the complex mode, macrocells are configured as outputs only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outermost macrocells (pin 12 and 19) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

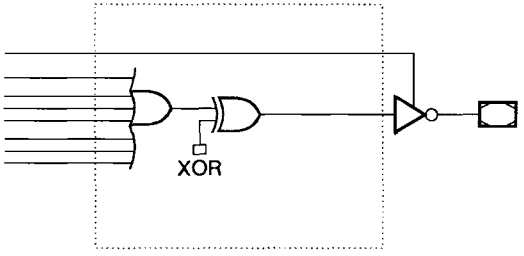
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1 and 11 are always available as data inputs into the AND array.

Combinatorial I/O Configuration for Complex Mode [1,2]



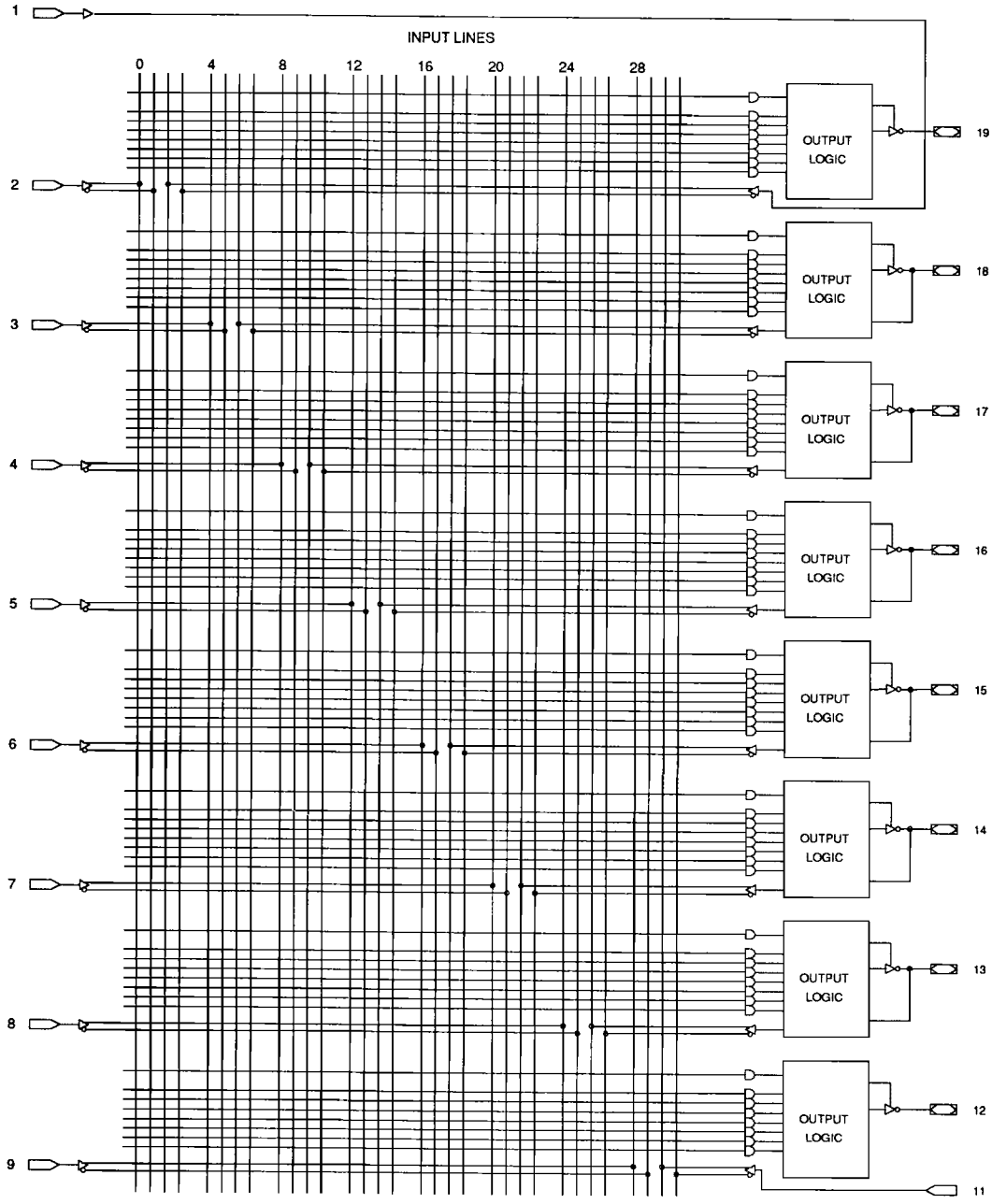
Notes:
1. Pin 13 through Pin 18 configured to this function.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Combinatorial Output Configuration for Complex Mode [1,2]



Notes:
1. Pin 12 and Pin 19 are configured to this function.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram



Simple Mode

In the simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

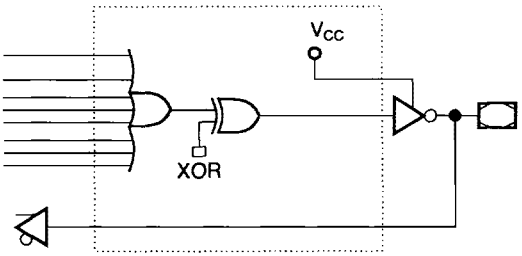
Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Dedicated input or output functions can be implemented as subsets of the I/O function.

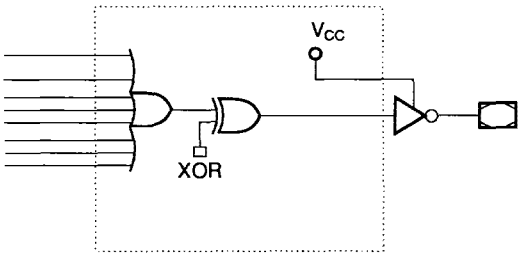
Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pin 15 and 16) cannot be used as inputs or I/Os, and are only available as dedicated outputs.

Combinatorial Output with Feedback Configuration for Simple Mode (1,2)



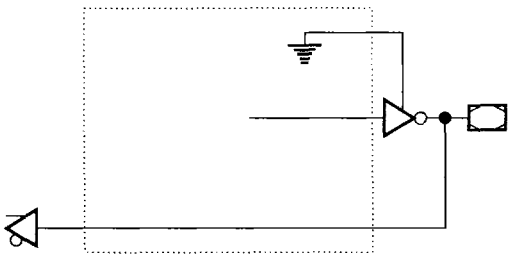
Notes:
1. All OMC **except** pins 15 and 16 can be configured to this function.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Combinatorial Output Configuration for Simple Mode (1,2)



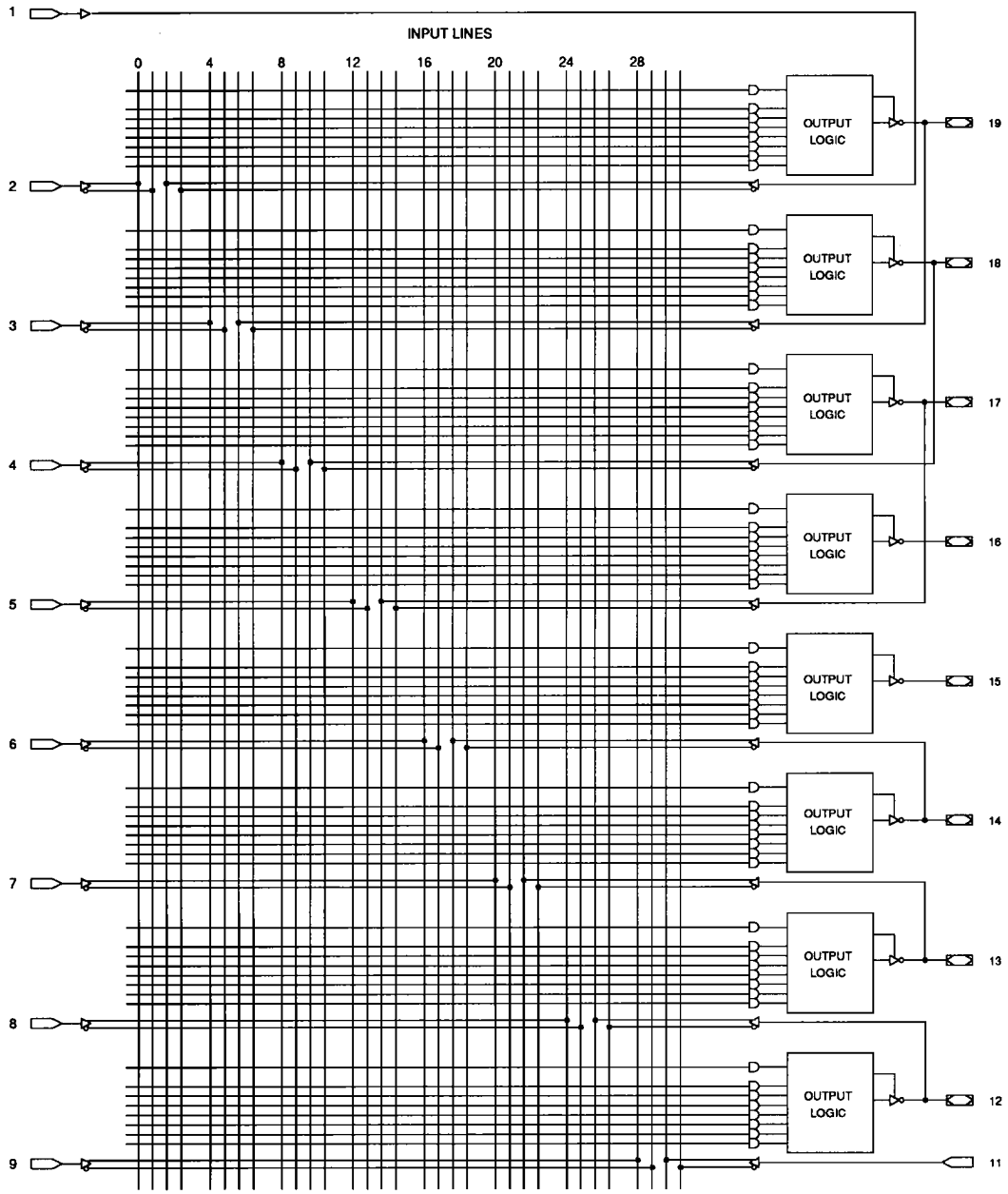
Notes:
1. Pins 15 and 16 are permanently configured to this function.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Dedicated Input Configuration for Simple Mode (1,2)



Notes:
1. All OMC **except** pins 15 and 16 can be configured to this function.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram



Power Up Reset

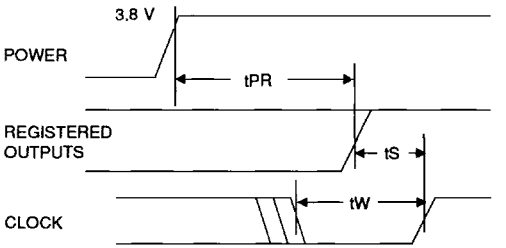
The registers in the ATF16V8B and ATF16V8BL are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8 V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and

3) The clock must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Device Programming

ATF16V8B/L devices are programmed using Atmel-approved logic programmers, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	7	5	ATF16V8B-7GC ATF16V8B-7JC ATF16V8B-7NC ATF16V8B-7PC ATF16V8B-7SC	20D3 20J 20L 20P3 20S	Commercial (0°C to 70°C)
10	10	7	ATF16V8B-10GC ATF16V8B-10JC ATF16V8B-10NC ATF16V8B-10PC ATF16V8B-10SC	20D3 20J 20L 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8B-10GI ATF16V8B-10JI ATF16V8B-10NI ATF16V8B-10PI ATF16V8B-10SI	20D3 20J 20L 20P3 20S	Industrial (-40°C to 85°C)
			ATF16V8B-10GM ATF16V8B-10NM	20D3 20L	Military (-55°C to 125°C)
			ATF16V8B-10GM/883 ATF16V8B-10NM/883	20D3 20L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	12	10	ATF16V8B-15GC ATF16V8B-15JC ATF16V8B-15NC ATF16V8B-15PC ATF16V8B-15SC	20D3 20J 20L 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8B-15GI ATF16V8B-15JI ATF16V8B-15NI ATF16V8B-15PI ATF16V8B-15SI	20D3 20J 20L 20P3 20S	Industrial (-40°C to 85°C)
			ATF16V8B-15GM ATF16V8B-15NM	20D3 20L	Military (-55°C to 125°C)
			ATF16V8B-15GM/883 ATF16V8B-15NM/883	20D3 20L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	12	ATF16V8B-25GC ATF16V8B-25JC ATF16V8B-25NC ATF16V8B-25PC ATF16V8B-25SC	20D3 20J 20L 20P3 20S	Commercial (0°C to 70°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	15	12	ATF16V8B-25GI ATF16V8B-25JI ATF16V8B-25NI ATF16V8B-25PI ATF16V8B-25SI	20D3 20J 20L 20P3 20S	Industrial (-40°C to 85°C)
			ATF16V8B-25GM ATF16V8B-25NM	20D3 20L	Military (-55°C to 125°C)
			ATF16V8B-25GM/883 ATF16V8B-25NM/883	20D3 20L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
10	10	7	ATF16V8BL-10GC ATF16V8BL-10JC ATF16V8BL-10NC ATF16V8BL-10PC ATF16V8BL-10SC	20D3 20J 20L 20P3 20S	Commercial (0°C to 70°C)
15	12	10	ATF16V8BL-15GC ATF16V8BL-15JC ATF16V8BL-15NC ATF16V8BL-15PC ATF16V8BL-15SC	20D3 20J 20L 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8BL-15GI ATF16V8BL-15JI ATF16V8BL-15NI ATF16V8BL-15PI ATF16V8BL-15SI	20D3 20J 20L 20P3 20S	Industrial (-40°C to 85°C)
			ATF16V8BL-15GM ATF16V8BL-15NM	20D3 20L	Military (-55°C to 125°C)
			ATF16V8BL-15GM/883 ATF16V8BL-15NM/883	20D3 20L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	12	ATF16V8BL-25GC ATF16V8BL-25JC ATF16V8BL-25NC ATF16V8BL-25PC ATF16V8BL-25SC	20D3 20J 20L 20P3 20S	Commercial (0°C to 70°C)
			ATF16V8BL-25GI ATF16V8BL-25JI ATF16V8BL-25NI ATF16V8BL-25PI ATF16V8BL-25SI	20D3 20J 20L 20P3 20S	Industrial (-40°C to 85°C)
			ATF16V8BL-15GM ATF16V8BL-15NM	20D3 20L	Military (-55°C to 125°C)
			ATF16V8BL-25GM/883 ATF16V8BL-25NM/883	20D3 20L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
20D3	20 Lead, 0.300" Wide, Ceramic Dual Inline Package (Cerdip)
20J	20 Lead, Plastic J-Leaded Chip Carrier (PLCC)
20L	20 Pad, Ceramic Leadless Chip Carrier (LCC)
20P3	20 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)