Signetics

FAST Products

FAST 74F582
4-Bit BCD Arithmetic Logic Unit

FEATURES

- Performs four BCD functions
- P and G outputs for high speed expansion
- Add/Subtract delay 28ns max
  Look ahead delay 22.5ns max
- Supply current 85mA max
- 24 pin 300 mil Slim Dip package

DESCRIPTION

The 74F582 Binary Coded Decimal (BCD) Arithmetic Logic Unit (ALU) is a 24 pin expandable unit that performs addition, subtraction, comparison of two numbers and binary to BCD conversion.

The 'F582 input and output logic includes a Carry/Borrow which is generated internally in the look-ahead mode, allowing BCD to computed directly. For more than one BCD decade, the Carry/Borrow term may ripple between 'F582s.

When $\overline{A}$/S is Low, BCD addition is performed (A+B+C/$\overline{B}$=F). If an input is greater than 9 binary to BCD conversion results at the output.

When $\overline{A}$/S is High, subtraction is performed. If the C/$\overline{B}$ is Low, then the subtraction is accomplished by internally computing the nine's complement addition of the two BCD numbers(A-B-1=F). When C/$\overline{B}$ is High, the difference of the two numbers is figured as A-F=F. If A is greater than or equal to B, the BCD difference appears at the output F in its true form. If A is less than B and C/$\overline{B}$ is Low, the 9s complement of the true form appears at the output F. As long as A is less than B, an active Low borrow is also generated. The 'F582 also performs binary to BCD conversion. For inputs from 10 to 15, binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying the binary number to the other set of inputs. This will generate a carry term to the next decade.

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F582	12.0 ns	55mA

ORDERING INFORMATION

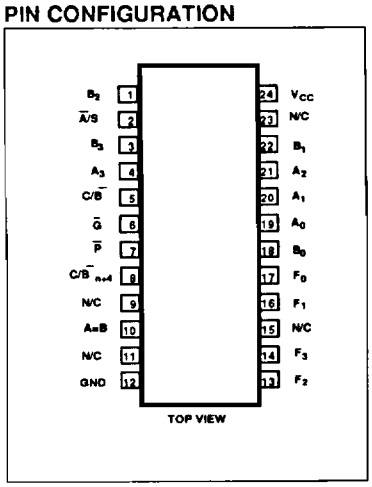
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F582N
24-Pin Plastic SOL	N74F582D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

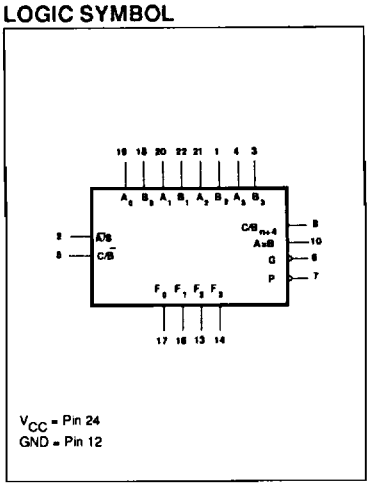
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0	B operand input	1.0/1.0	20µA/0.6mA
B_1	B operand input	1.0/4.0	20µA/2.4mA
B_2	B operand input	1.0/3.0	20µA/1.8mA
B_3	B operand input	1.0/2.0	20µA/1.2mA
$\overline{A}$/S	Add/Subtract input	1.0/3.0	20µA/1.8mA
C/$\overline{B}$	Carry/Borrow input	1.0/1.0	20µA/0.6mA
C/$\overline{B}_{n+4}$	Carry/Borrow output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry Generator output	50/33	1.0mA/20mA
A=B	Comparator output	OC/33	OC/20mA
F_0-F_3	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

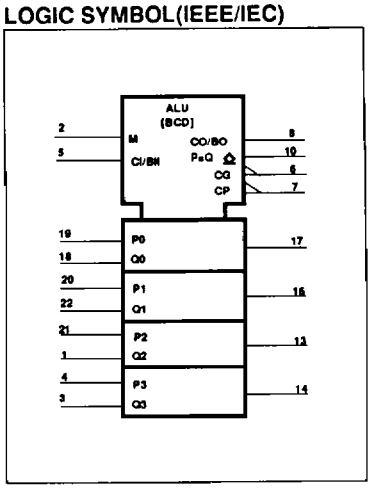
PIN CONFIGURATION



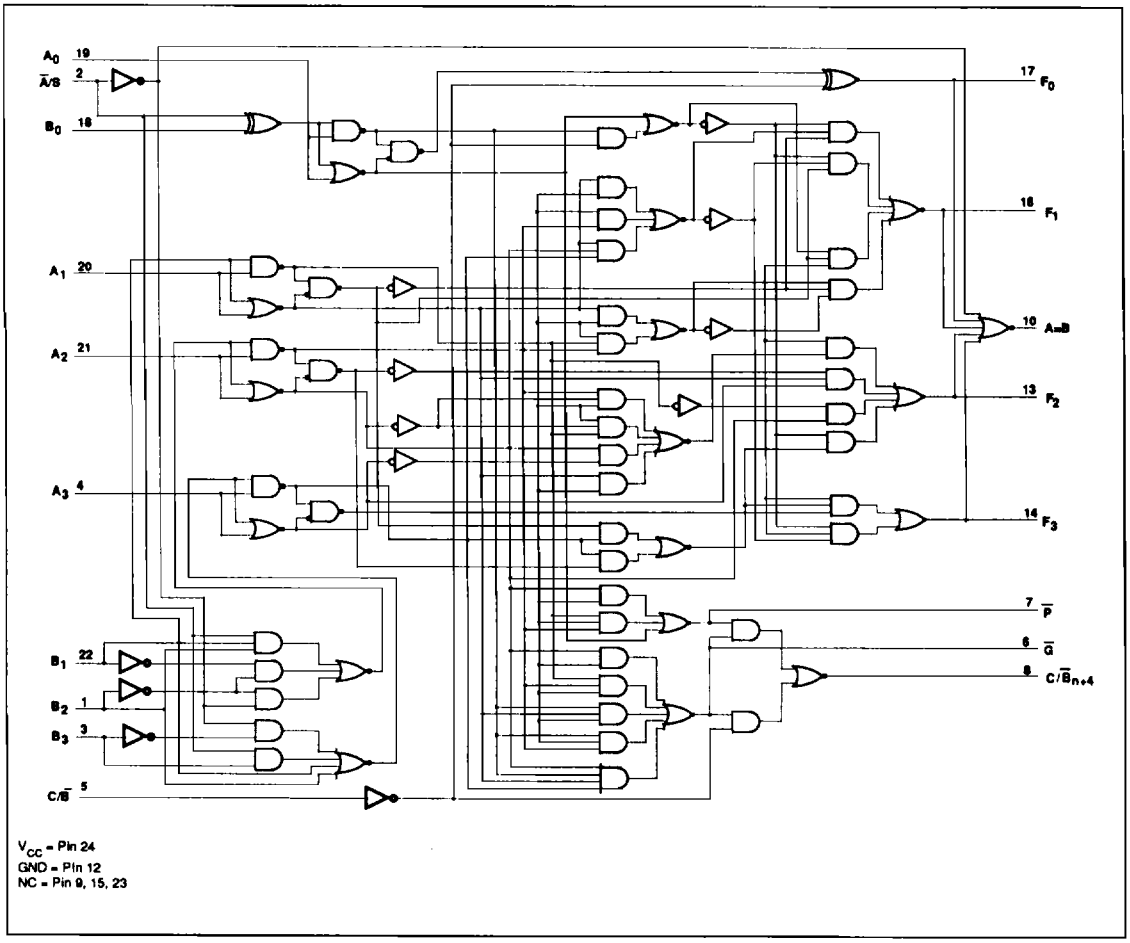
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	$\overline{A}/S$	A_n	B_n	$C/\overline{B}$	F_n	$C/\overline{B}_{n+4}$	A=B
Add	L	BCD Augend	BCD Addend	H=Carry	IF $C/\overline{B}$=H F=A+B+1	F≤9 $C/\overline{B}_{n+4}$=L	X
				L=No carry	IF $C/\overline{B}$=L F=A+B	F>9 $C/\overline{B}_{n+4}$=H	
Subtract	H	BCD Minuend	BCD Subtrahend	L=Borrow	IF $C/\overline{B}$=L F=A-B-1	A>B $C/\overline{B}_{n+4}$=H A≤B $C/\overline{B}_{n+4}$=L	X
				H=No Borrow	IF $C/\overline{B}$=H F=A-B	A<B $C/\overline{B}_{n+4}$=L A≥B $C/\overline{B}_{n+4}$=H	
Compare	H	BCD Word A	BCD Word B	H	A-B	A<B $C/\overline{B}_{n+4}$=L A>B $C/\overline{B}_{n+4}$=H	IF A=B Compare=H IF A≠B Compare=L
Binary to BCD Conversion	L	0≤A≤15	B=0	X	BCD	A≤9 $C/\overline{B}_{n+4}$=L A>9 $C/\overline{B}_{n+4}$=H	X

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High-level output voltage	A=B only			4.5	V
I_{OH}	High-level output current	Except A=B			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	A=B only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Except A=B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7		3.4	V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	mA
					±5%V_{CC}		0.30	0.50	mA
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximuminput voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	B_0, C/$\overline{B}$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		A_n, B_3						-1.2	mA
		B_2, $\overline{A}$/S						-1.8	mA
		B_1						-2.4	mA
I_{OS}	Short circuit output current[3]	Except A=B	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				55	85	mA

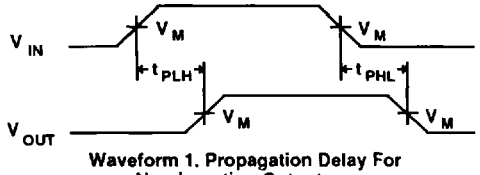
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

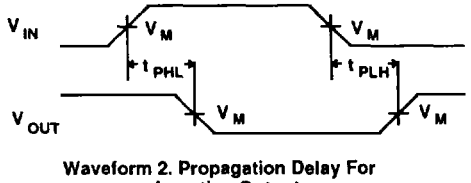
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to F_n	Waveform 1,2	5.0 4.0	17.5 14.0	23.0 19.0	5.0 4.0	25.0 20.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $C/\overline{B}_{n+4}$	Waveform 1,2	7.0 4.0	16.0 10.0	20.0 14.0	6.0 4.0	22.5 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to $C/\overline{B}_{n+4}$	Waveform 1,2	3.5 2.5	5.5 5.0	8.0 7.0	3.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to A=B	Waveform 1,2	8.0 6.0	18.0 14.0	24.0 18.0	8.0 5.5	27.0 21.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{G}$ or $\overline{P}$	Waveform 1,2	4.0 4.0	11.0 11.0	14.0 14.0	4.0 4.0	16.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to F_n	Waveform 1,2	8.0 8.0	15.0 14.0	20.0 18.0	7.0 7.0	25.0 19.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to A=B	Waveform 1,2	10.0 4.0	18.0 6.0	24.0 9.0	10.0 3.5	28.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to $\overline{G}$ or $\overline{P}$	Waveform 1,2	6.0 6.0	11.0 11.0	14.5 14.5	6.0 6.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to $C/\overline{B}_{n+4}$	Waveform 1,2	8.0 7.0	14.0 12.0	19.0 15.0	8.0 7.0	20.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to F_n	Waveform 1,2	4.0 3.0	13.0 9.0	17.5 13.0	4.0 3.0	18.5 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to A=B	Waveform 1,2	8.0 4.0	15.0 8.0	20.0 12.0	8.0 3.5	22.5 13.0	ns

AC WAVEFORMS



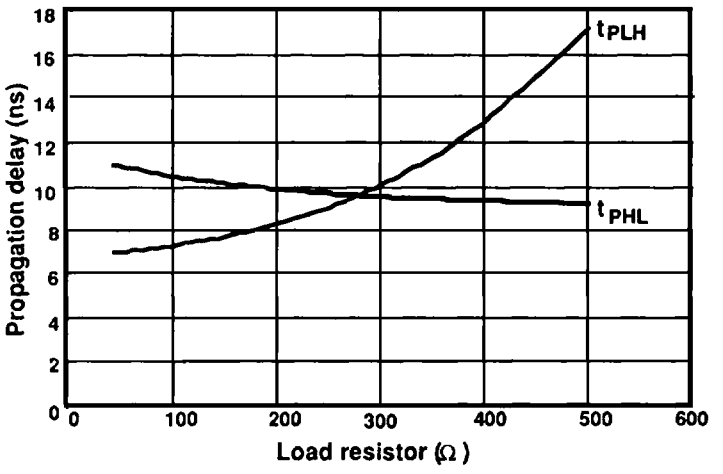
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output

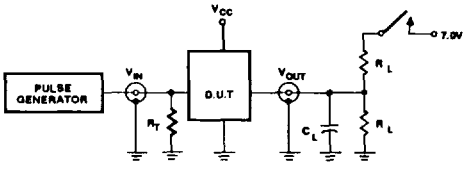
NOTE: For all waveforms, V_M = 1.5V

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Output and Totem-Pole Outputs

SWITCH POSITION

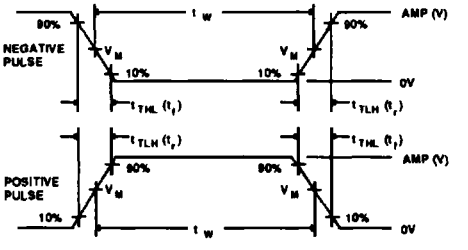
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns