GIGABIT ETHERNET CHIPSET S2046/S2047

FEATURES

- Functionally compliant with the IEEE 802.3z Specification
- S2046 transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- S2047 receiver PLL configured for clock and data recovery
- 1250 Mb/s (Gigabit Ethernet) operation
- 10-bit or 20-bit parallel TTL compatible interface
- 1 watt typical power dissipation for chipset
- +3.3/+5 V power supply
- Low-jitter serial PECL compatible interface
- Lock detect
- Local loopback
- Compact 52 pin PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- TTL compatible outputs possible with +5V I/O power supply

APPLICATIONS

High-speed data communications

- Ethernet backbone connections
- Mainframe
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

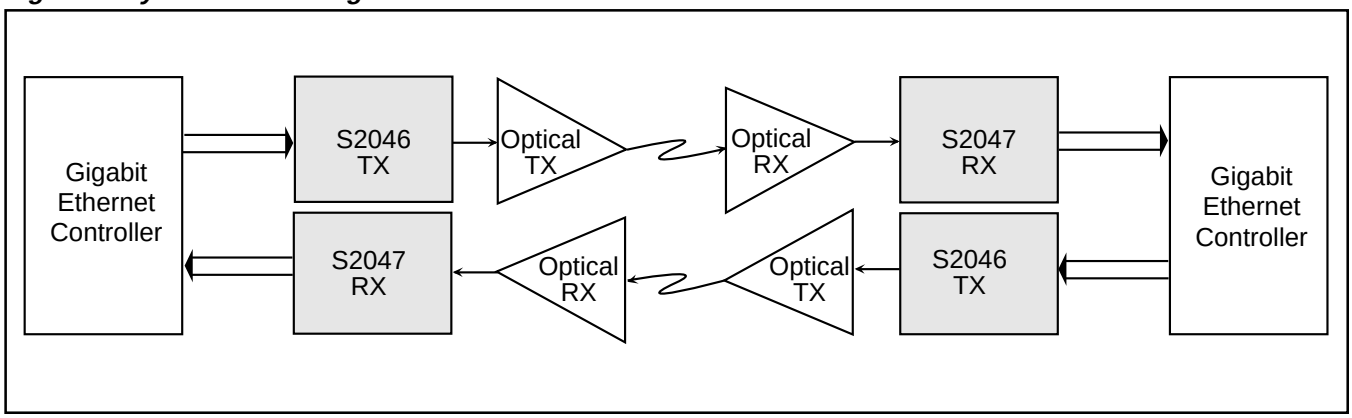
GENERAL DESCRIPTION

The S2046 and S2047 transmitter and receiver pair are designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the IEEE 802.3z specification. The chipset is Gigabit Ethernet compliant and supports 1250 Mb/s with an associated 10 or 20-bit data word.

The chipset performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The S2046 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S2047 on-chip PLL synchronizes directly to incoming digital signals, to receive the data stream. The transmitter and receiver each support differential PECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local loopback allows for system diagnostics. The I/O section can operate from either a +3.3 V or a +5 V power supply. With a 3.3 V power supply the chipset dissipates only 1 W typically.

Figure 1 shows a typical network configuration incorporating the chipset.

Figure 1. System Block Diagram



S2046/S2047 OVERVIEW

The S2046 transmitter and S2047 receiver provide serialization and deserialization functions for block-encoded data to implement a Gigabit interface. Operation of the S2046/S2047 chips is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter
1. 10/20-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10/20-bit parallel output

The 10/20-bit parallel data handled by the S2046 and S2047 devices should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters.

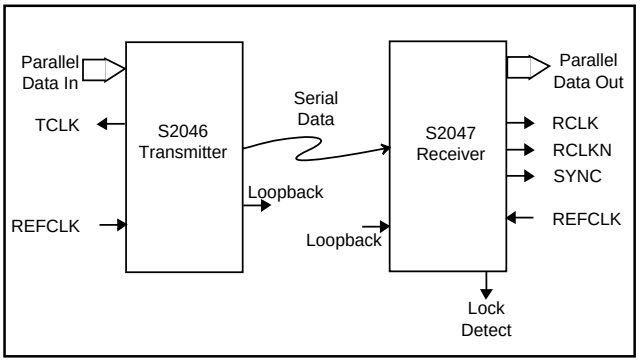
Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 5.

A lock detect feature is provided on the receiver, which indicates that the PLL is locked (synchronized) to the data stream.

Loopback

Local loopback is supported by the chipset, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Interface Diagram



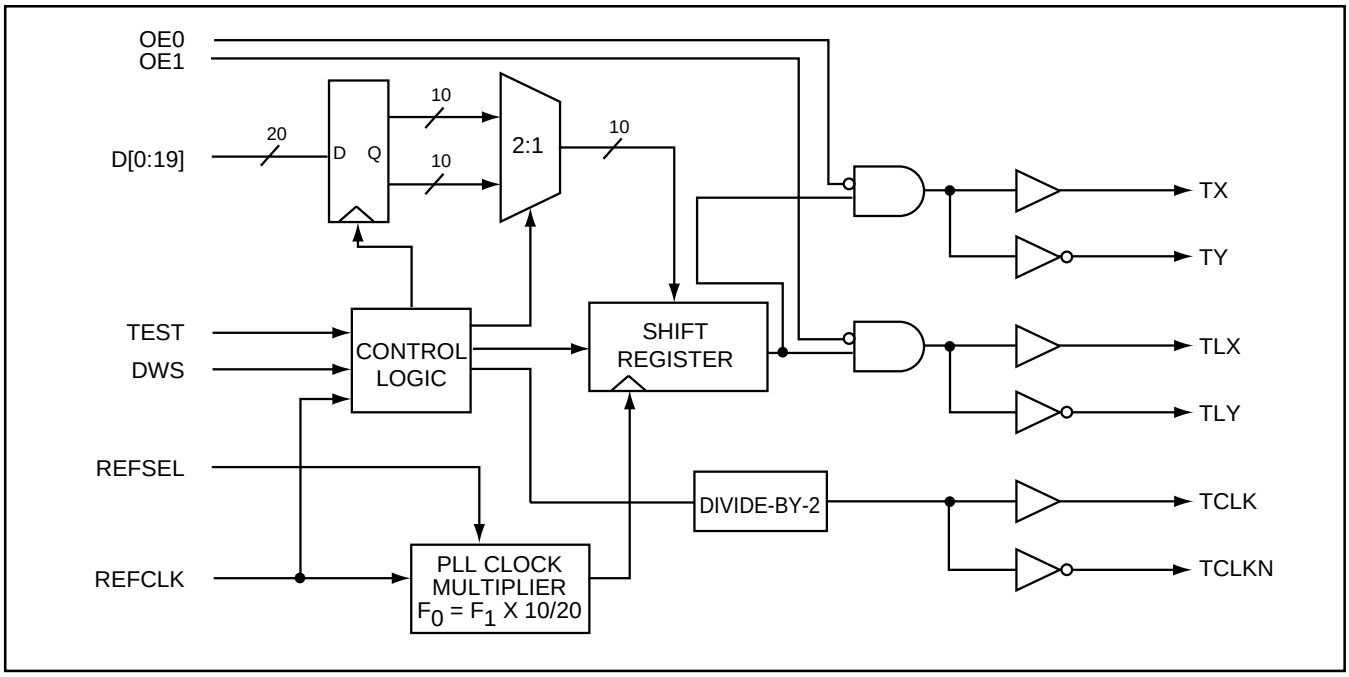
S2046 TRANSMITTER

Architecture/Functional Description

The S2046 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The S2046 is fully compliant with the IEEE 802.3z Specification, and supports the Gigabit Ethernet data rate of 1250 Mbit/sec.

The parallel input data word can be either 10 bits or 20 bits wide, depending upon DWS pin selection. A block diagram showing the basic chip function is shown in Figure 3.

Figure 3. S2046 Functional Block Diagram



Parallel/Serial Conversion

The parallel-to-serial converter takes in 10-bit or 20-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of REFCLK. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10 or 20 times the REFCLK input frequency. The state of the serial outputs is controlled by the output enable pins, OE0 and OE1. D[10] is transmitted first in 10-bit mode. D[0] is transmitted first in 20-bit mode. Table 2 shows the mapping of the parallel data to the 8B/10B codes.

10-Bit/20-Bit Mode

The S2046 operates with either 10-bit or 20-bit parallel data inputs. Word width is selectable via the DWS pin. In 10-bit mode, D[10:19] are used and D[0:9] are ignored.

Reference Clock Input

The reference clock input (REFCLK) must be supplied with a PECL single-ended AC coupled crystal clock source with 100 PPM tolerance to assure that the transmitted data meets the Fibre Channel and IEEE 802.3z Specification frequency limits. The internal serial clock is frequency locked to the reference clock. Refer to Table 1 for reference clock frequencies.

Table 1. Transmitter Operating Modes

DWS	REFSEL	Data Rate (Mbps)	Word Width (Bits)	Reference Clock Frequency (MHz)	TCLK/TCLKN Frequency (MHz)
0	0	1250.0	20	62.50	62.50
1	1	1250.0	10	125.0	62.5

Table 2. Data Mapping to 8B/10B Alphabetic Representation

	First Data Byte										Second Data Byte									
TX[0:19] or RX[0:19]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
8B/10B alphabetic representation	a	b	c	d	e	i	f	g	h	j	a	b	c	d	e	i	f	g	h	j

↑ First bit transmitted in 20-bit mode ↑ First bit transmitted in 10-bit mode

Figure 4. S2047 Functional Block Diagram

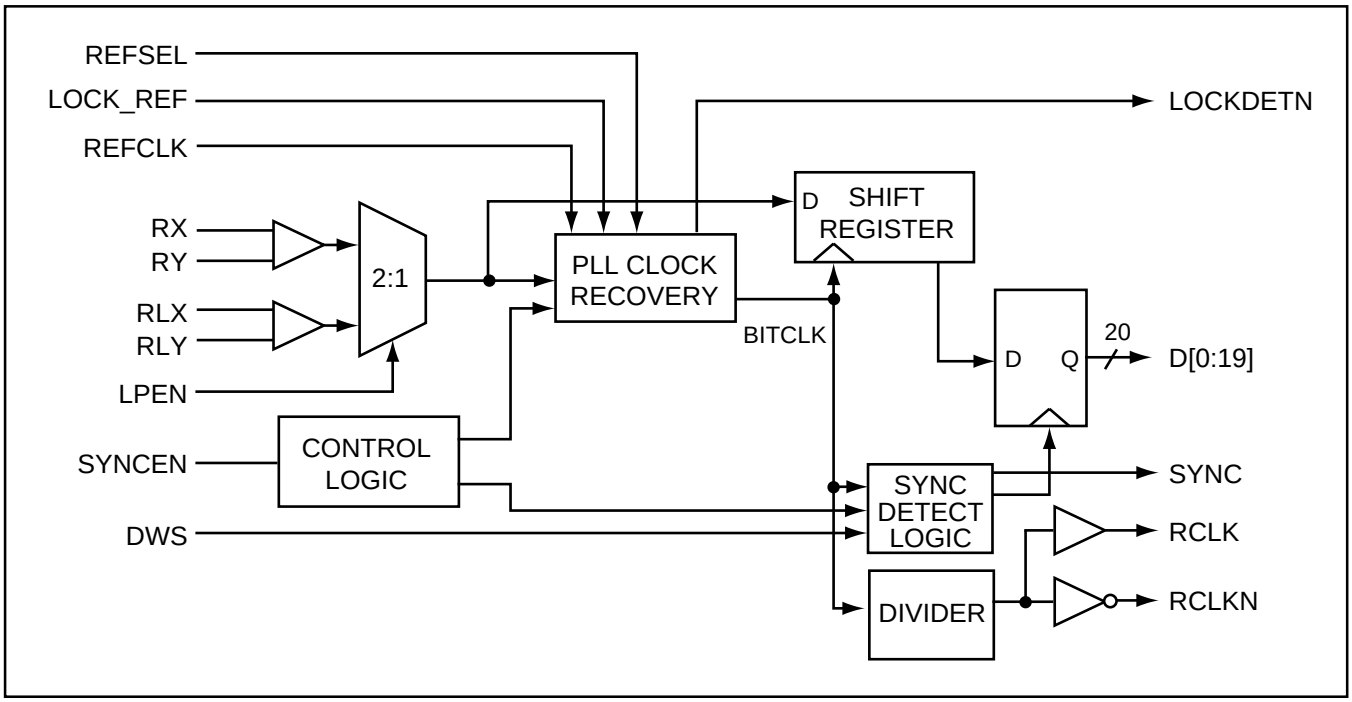
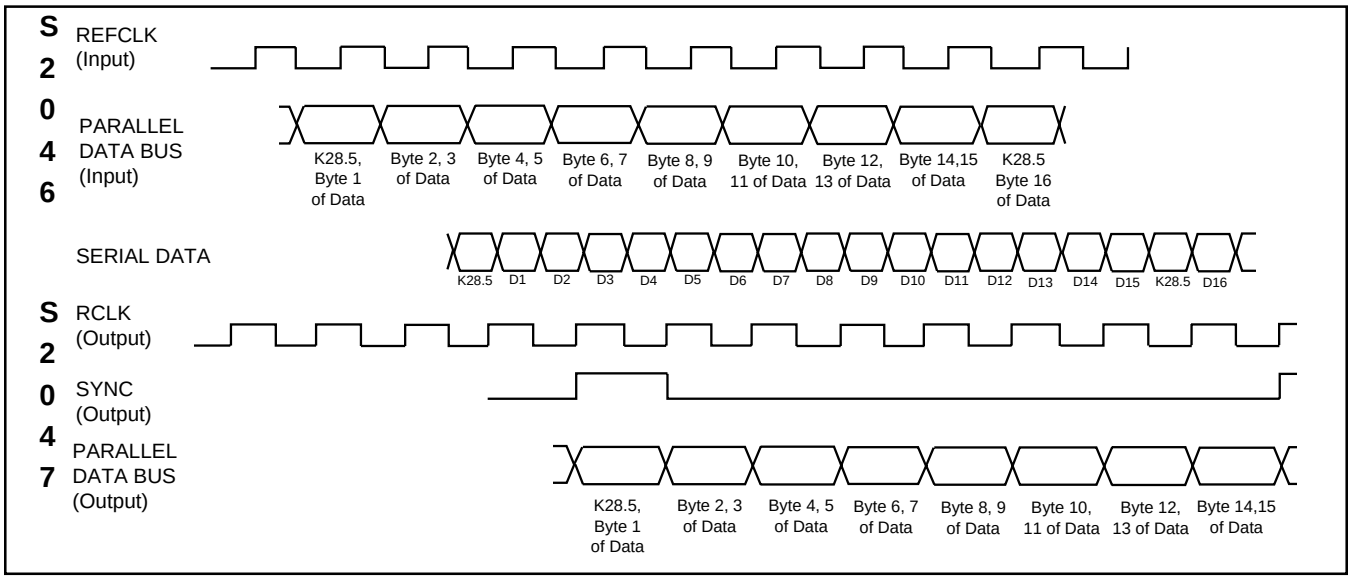


Figure 5. Functional Waveform



1. A.X. Widmer and P.A. Franaszek, “A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code,” IBM Research Report RC 9391, May 1982.

S2047 RECEIVER

Architecture/Functional Description

The S2047 receiver is designed to implement the IEEE 802.3z Specification receiver functions. A block diagram showing the basic chip function is provided in Figure 4.

Whenever a signal is present, the S2047 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. Received data from the incoming bit stream is provided on the device’s parallel data outputs.

The S2047 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of 8B/10B encoded data by a compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the transmission layer as 10-bit or 20-bit parallel data. The chip operates at the Gigabit Ethernet frequency of 1250 Mbit/s.

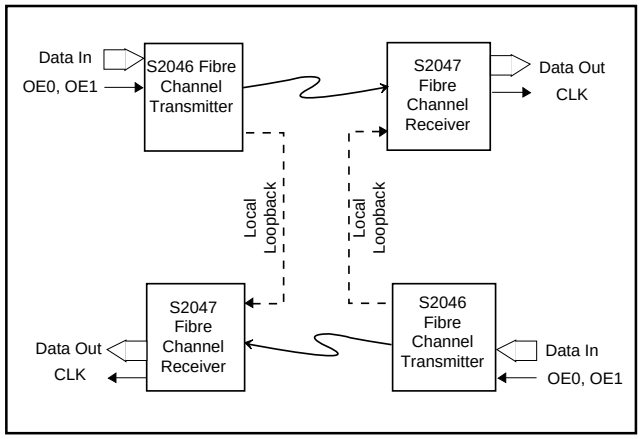
Serial/Parallel Conversion

Serial data is received on the RX, RY pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The data is then clocked into the serial to parallel output registers. The parallel data out can be either 10 or 20 bits wide determined by the state of the DWS pin. The word clock (RCLKN) is synchronized to the incoming data stream word boundary by the detection of the K28.5 synchronization pattern (0011111010, positive running disparity).

10-Bit/20-Bit Mode

The S2047 will operate with either 10-bit or 20-bit parallel data outputs. This option is selectable via the DWS pin. See Table 3. In 10-bit mode, the 10-bit data word is output on both D[10:19] and D[0:9] simultaneously.

Figure 6. Interface Diagram



Reference Clock Input

The reference clock input must be supplied with a PECL single-ended AC coupled crystal clock source at ±100 PPM tolerance. See Table 3 for reference clock frequencies.

Framing

The S2047 provides SYNC character recognition and data word alignment of the TTL level compatible output data bus. During the data realignment process, the RCLKN phase will be adjusted. No glitches will occur in the RCLKN signal due to the realignment. In systems where the SYNC detect function is undesired, a LOW on the SYNCEN input disables the SYNC function and the data will be "un-framed."

When framing is disabled by low SYNCEN, the S2047 simply achieves bit synchronization and begins to deliver parallel output data words whenever it has received full transmission words. No attempt is made to synchronize on any particular incoming character.

The SYNC output signal will go high whenever a K28.5 character (positive disparity) is present on the parallel data outputs. The SYNC output signal will be low at all other times. This is true whether the S2047 is operating in 10-bit mode or in 20-bit mode.

Table 3. Receiver Operating Modes

DWS	REFSEL	Data Rate (Mbps)	Word Width (Bits)	Reference Clock Frequency (MHz)	RCLK/RCLKN Frequency (MHz)
0	0	1250.0	20	62.50	62.50
1	1	1250.0	10	125.0	62.5

Lock Detect

The S2047 lock detect function indicates the state of the phase-locked loop (PLL) clock recovery unit. The PLL will indicate lock after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment within 250 bit times. If a run length of 64 bits is exceeded, or if the transition density is less than 12%, the loop will be declared out of lock and will attempt to re-acquire bit synchronization. When lock is lost, the PLL will shift from the serial input data to the reference clock, so that correct frequency downstream clocking will be maintained.

In any transfer of PLL control from the serial data to the reference clock, the RCLK/RCLKN output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

Start-Up Procedure

The clock recovery PLL requires an initilization procedure to correctly achieve lock on the serial data inputs. At power-up or loss of lock, the PLL must first acquire frequency lock to the local reference clock. This can be accomplished connecting the LOCK_REF pin to a 10 ms reset signal. If this is not possible, the PLL can also be initialized by guaranteeing that no data is seen at the serial data inputs for a minimum of 10 ms upon power-up. If the serial data inputs cannot be controlled, then the S2047 can be put into the loopback mode and the loopback outputs of the S2046 must be quiescent for a minimum of 10 ms after power-up.

OTHER OPERATING MODES

Loopback

Local loopback requires a S2046 and a S2047 as shown in Figure 6. When enabled, serial data from the S2046 transmitter is sent to the S2047 receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

Operating Frequency Range

The S2046 and S2047 are optimized for operation at the Gigabit Ethernet rate of 1250.0 Mbit/s. REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

Test Modes

The TEST pin on the S2046 and the SYNCEN pin on the S2047 provide a PLL bypass mode that can be used for operating the digital area of the chip. In this mode, clock signals are input through the reference clock pins. This can be used for testing the device during the manufacturing process or during an offline self-test. Sync detection is always enabled in test mode.

Table 4. S2046 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	I	50 49 48 47 44 43 42 41 38 37 36 35 31 30 29 28 25 24 23 22	Accepts parallel input data. Data is clocked in on the rising edge of REFCLK. In 20-bit mode, D[0] is transmitted first. In 10-bit mode, D[10:19] are used, D[0:9] are ignored, and D[10] is transmitted first.
TEST	Static TTL	I	20	Multilevel input used for factory testing. When not connected, REFCLK replaces the internal bit clock to facilitate factory testing. In normal use, this input is wired to ground.
DWS	Static TTL	I	19	The level on this pin selects the parallel data bus width. Active High. When inactive, a 20-bit parallel bus width is selected, and D[0:19] are active. When active, a 10-bit parallel data bus is selected, D[10:19] are active and D[0:9] are not used. (See Table 1.) A rising edge will reset the part (used for test).
OE1	Static TTL	I	1	Active low output enable control for TLX/TLY outputs. TLX/TLY will go to the logic low state when disabled.
OE0	Static TTL	I	2	Active low output enable control for TX/TY outputs. TX/TY will go to the logic low state when disabled.
REFCLK	PECL	I	16	(Externally capacitively coupled.) A crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 1.)
TCLK TCLKN	Diff. TTL	O	12 11	Differential TTL word rate clock true and complement. See Table 1 for frequency.
TLX TLY	Diff. PECL	O	5 4	Differential PECL outputs that are functionally equivalent to TX and TY. They are intended to be used for loopback testing. Enabled by OE1. TLX is the positive output, TLY is the negative output.
TY TX	Diff. PECL	O	9 8	Differential PECL outputs that transmit the serial data and drive 75 Ω or 50 Ω termination to VCC-2 V. Enabled by OE0. TX is the positive output, and TY is the negative output.

Table 4. S2046 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
REFSEL	Static TTL	I	18	Multilevel input used to select the reference clock frequency. (See Table 1.)
ECLVCC	+3.3 V	–	21, 39	Core +3.3 V
TTLGND	GND	–	14, 15, 34	TTL Ground
TTLVCC	+3.3 V or +5 V	–	17	TTL Power Supply (+5 V if TTL)
ECLIOVCC	+3.3 V	–	3, 10	PECL I/O Power Supply
ECLIOVEE	GND	–	6, 7	PECL I/O GND
AVCC	+3.3 V	–	27, 32	Analog Power Supply
AVEE	GND	–	26, 33	Analog Ground
ECLVEE	GND	–	13, 40, 51, 52	Core Ground

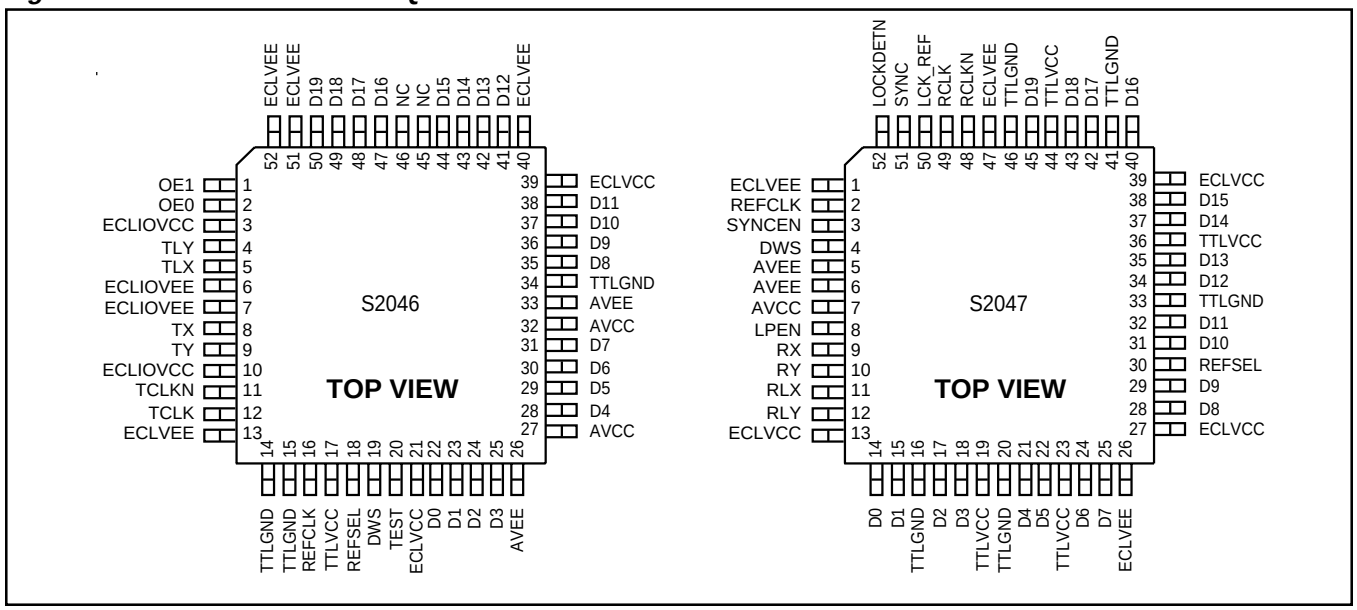
Table 5. S2047 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	TTL	O	45 43 42 40 38 37 35 34 32 31 29 28 25 24 22 21 18 17 15 14	Outputs parallel data. The width of the parallel data bus is selected by the state of the DWS pin. Parallel data on this bus is clocked out on the falling edge of RCLK. In 20-bit mode, D[0] is the first bit received. In 10-bit mode, D[10:19] are used and D[0:9] are driven to the high state. In 10-bit mode, D[10] is the first bit received.
LOCKDETN	TTL	O	52	Lock Detect. Active Low. When active, LOCKDETN indicates that the PLL is locked to the incoming data stream. When inactive, it provides a system flag indicating that the PLL is locked to the local reference clock.
LPEN	TTL	I	8	Loop Enable. Active High. When Active, LPEN selects the loopback differential serial input pins (RLX, RLY). When inactive, LPEN selects RX and RY (normal operation).
DWS	Static TTL	I	4	Data Width Select. Active High. The level on this pin selects the parallel data bus width. When inactive, a 20-bit parallel bus width is selected, and D[0:19] are active. When active, a 10-bit parallel data bus is selected, D[10:19] are active and D[0:9] will go active. (See Table 3.) A rising edge will reset the internal counters (used for test).
RCLK RCLKN	Diff. TTL	O	49 48	Parallel data is clocked out on the falling edge of RCLK/RCLKN. After a sync word is detected, the period of the current RCLK and RCLKN is stretched to align with the word boundary. (See Table 3 for frequency.)
REFCLK	PECL	I	2	(Externally capacitively coupled.) A free-running crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLK is set by the REFSEL pin. (See Table 3.)
SYNC	TTL	O	51	Synchronization (frame). Active High. Upon detection of a valid sync symbol, this output goes active for one RCLK period. When sync is active, the sync symbol is present on the parallel data bus bits D[0:9] in 20-bit mode or D[0:9] and D[10:19] in 10-bit mode.
RLX RLY	Diff. PECL	I	11 12	(Externally capacitively coupled.) The serial loopback data inputs. RLX is the positive input, and RLY is the negative input.

Table 5. S2047 Pin Assignment and Descriptions (Continued)

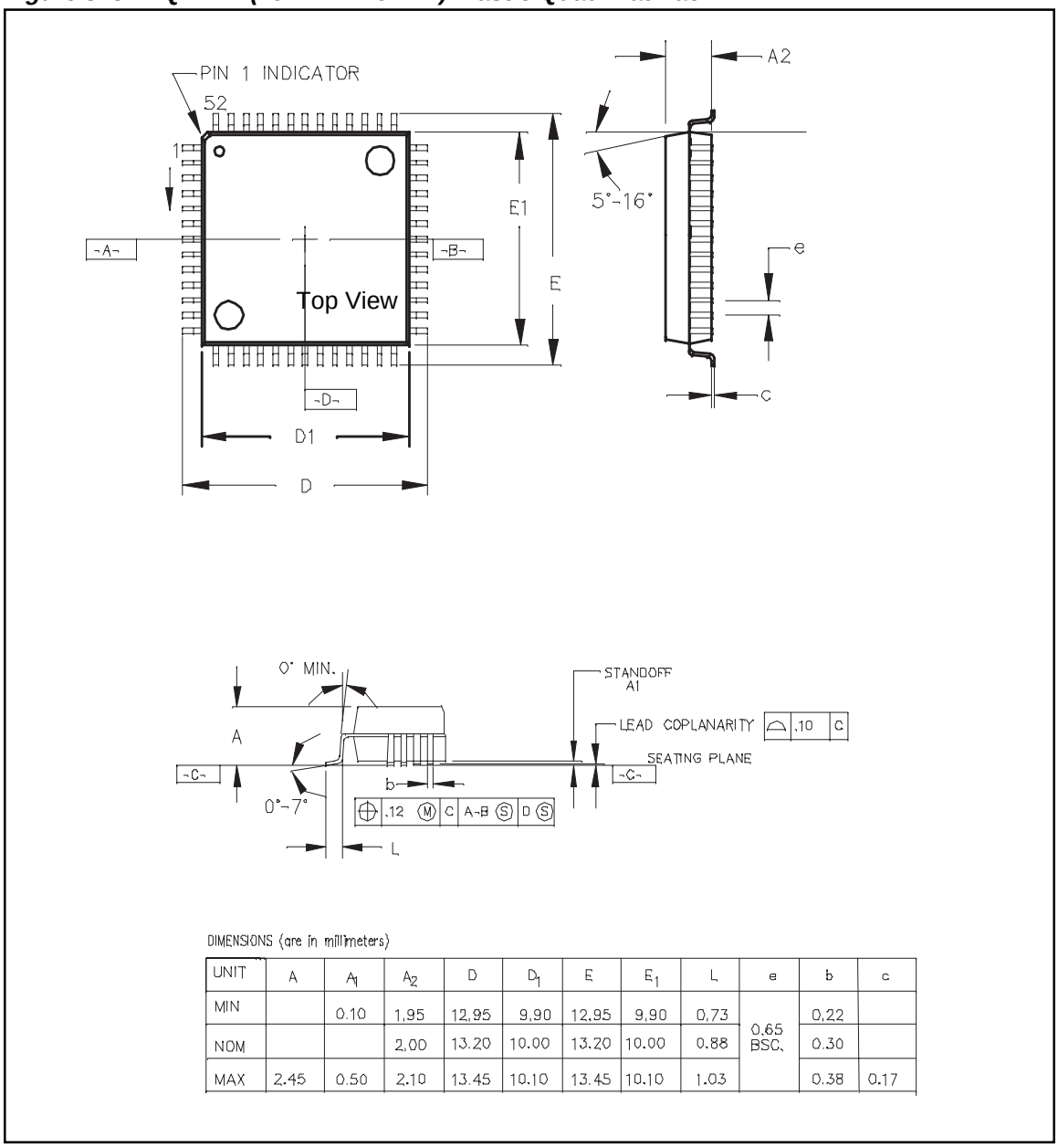
Pin Name	Level	I/O	Pin #	Description
RX RY	Diff. PECL	I	9 10	(Externally capacitively coupled.) The received serial data inputs. RX is the positive input, and RY is the negative input.
SYNCEN	Static TTL	I	3	Sync Enable. Active High. (Multilevel.) When active, enables sync detection. Detection of the sync pattern (K28.5:0011111010, positive running disparity) will enable the word boundary for the data to follow. When open (not connected), REFCLK replaces internal bit clock to facilitate factory testing. In this mode of operation, sync detection is always enabled. When inactive, data is treated as unframed data.
REFSEL	Static TTL	I	30	Reference Select. (Multilevel.) Input used to select the reference clock frequency. (See Table 3.)
LOCK_REF	TTL	I	50	Lock to Reference. Active Low. When active, forces the PLL to lock to the REFCLK input and ignore the serial data inputs.
TTLVCC	+3.3 V or +5 V	–	19, 23, 36, 44	TTL Power Supply (+5 V if TTL)
TTLGND	GND	–	16, 20, 33, 41, 46	TTL Ground
ECLVCC	+3.3 V	–	13, 27, 39	Core Power Supply
ECLVEE	GND	–	1, 26, 47	Core Ground
AVCC	+3.3 V	–	7	Analog Power Supply
AVEE	GND	–	5, 6	Analog Ground

Figure 7. S2046 and S2047 52 PQFP Pinouts



TTLVCC = +5 V or +3.3 V
AVCC = +3.3 V
ECLVCC = +3.3 V
ECLIOVCC = +3.3 V
ECLIOVEE = 0 V
TTLGND = 0 V
ECLVEE = 0 V
AVEE = 0 V

Figure 8. 52 PQFP — (10 mm x 10 mm) Plastic Quad Flat Pack



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.10	1.95	12.95	9.90	12.95	9.90	0.73	0.65 BSC.	0.22	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.30	
MAX	2.45	0.50	2.10	13.45	10.10	13.45	10.10	1.03		0.38	0.17

Table 6. Thermal Management

Device	Θja (Still AM)
S2046	52 ° C/W
S2047	52 ° C/W

Table 7. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S2046/S2047 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only and operation of the device at the maximums stated or any other conditions beyond those indicated in the “Recomended Operating Conditions” of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Typ	Max	Units
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on V_{CC} with respect to GND	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.7		V_{CC} +0.6	V
Voltage on any PECL Input Pin	0		ECL/V_{CC}	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

Table 8. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias			130	°C
Voltage on V_{CC} with respect to GND 5 V Operation 3.3 V Operation	 4.75 3.13	 5.0 3.3	 5.25 3.47	 V V
Voltage on any LVTTL Input Pin	0		5.25	V
Voltage on ECLVCC with respect to GND	3.13	3.3	3.47	V
Voltage on any PECL Input Pin	$ECLV_{CC}$ -2.0		$ECLV_{CC}$	V

Table 9. S2046 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL) + 3.3 V Power Supply + 3.3 V Power Supply + 5 V Power Supply	 2.1 2.2 2.7			 V V V	 V_{CC} = min, I_{OH} = -2.4 mA V_{CC} = min, I_{OH} = -.1 mA V_{CC} = min, I_{OH} = -1 mA
V_{OL}	Output Low Voltage (TTL) + 3.3 V Power Supply + 5 V Power Supply			0.5 0.5	V V	V_{CC} = min, I_{OL} = 2.4 mA V_{CC} = min, I_{OL} = 4 mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input High Voltage (TTL)	0		0.8	V	
I_{IH}	Input High Current (TTL)			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current (TTL)	-500		-50	µA	V_{IN} = 0.5 V
I_{CC}	Supply Current		123	160	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		0.406	0.554	W	Outputs open, V_{CC} = V_{CC} max
ΔV_{INCLK}	Single-ended REFCLK input swing	440		1300	mV	AC coupled
ΔV_{OUT}	Serial Output Voltage Swing	600		1300	mV	50 W to V_{CC} -2.0 V

Table 10. S2047 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL) + 3.3 V Power Supply + 3.3 V Power Supply + 5 V Power Supply	 2.1 2.2 2.7			 V V V	 V_{CC} = min, I_{OH} = -2.4 mA V_{CC} = min, I_{OH} = -.1 mA V_{CC} = min, I_{OH} = -1 mA
V_{OL}	Output Low Voltage (TTL) + 3.3 V Power Supply + 5 V Power Supply			 0.5 0.5	 V V	 V_{CC} = min, I_{OL} = 2.4 mA V_{CC} = min, I_{OL} = 6 mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input High Voltage (TTL)	0		0.8	V	
I_{IH}	Input High Current (TTL)			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current (TTL)	-500		-50	µA	V_{IN} = 0.5 V
I_{CC}	Supply Current – 10-Bit Mode – 20-Bit Mode		 187 194	 256 267	 mA mA	 Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation + 3.3 V Supply, 10-Bit Mode + 3.3 V Supply, 20-Bit Mode + 5 V Supply, 10-Bit Mode + 5 V Supply, 20-Bit Mode		 0.617 0.640 0.728 0.778	 0.887 0.925 1.08 1.142	 W W W W	 Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max Outputs open, V_{CC} = V_{CC} max
ΔVI_{NCLK}	Single-ended REFCLK input swing	440		1300	mV	AC coupled
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		1300	mV	

Timing

The data on the TX[00:09] (TX[00:19]) data bus will be sampled on every rising edge of REFCLK. The data will be serialized and transmitted onto the serial link. The figure below illustrates the timing requirements of REFCLK with respect to the TX[10:19] (TX[0:9]) signals, minimum high and low durations, and the rising and falling slew rate magnitudes. In addition, this system supplied clock must not have more jitter than ±20% of a baud interval.

Figure 9. REFCLK Timing Diagram

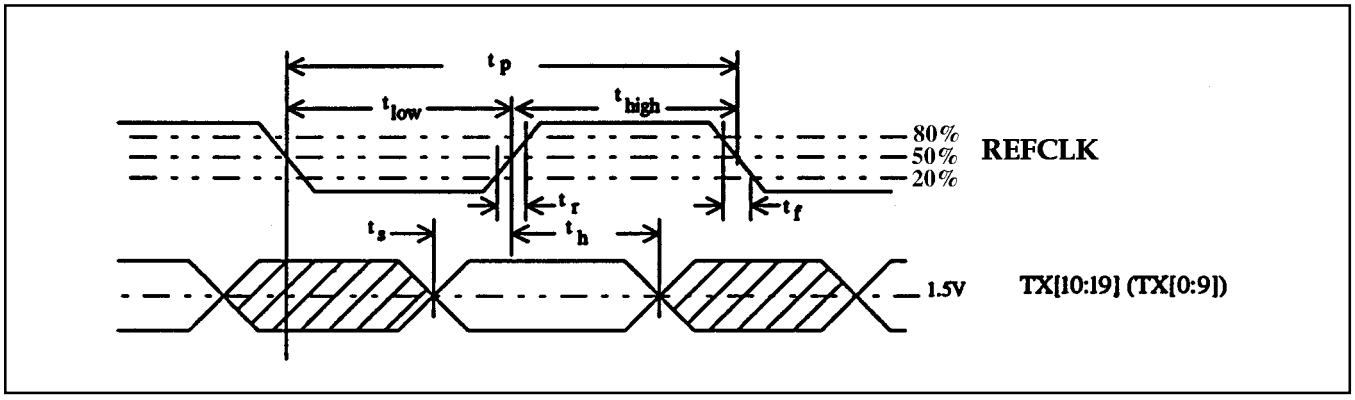


Table 11. REFCLK Timing Table

Parameter	Symbol	Min	Max	Units	Conditions[1]
Frequency 62.50 MHz 125.00 MHz	f	 62.49375 124.9875	 62.50625 125.0125	MHz	This is dependent on the data path width.
Jitter 1250.0 MBaud			160	ps pk-pk	
Period (f=62.5 MHz)	t_p	15.9984	16.0016	ns	
Period (f=125.0 MHz)	t_p	7.9992	8.0008	ns	
REFCLK Low Time	t_{low}	3.2		ns	
REFCLK High Time	t_{high}	3.2		ns	
TX Setup to REFCLK	t_s	2		ns	
TX Hold From REFCLK	t_h	2		ns	
REFCLK Rise Time	t_r	0.5	3.2	ns	This applies to the REFCLK input.
REFCLK Fall Time	t_f	0.5	3.2	ns	This applies to the REFCLK input.

1. All parameters are for outputs driven into a 35pF lumped capacitive load.

Table 12. Serial Data Timing Table (TLX, TLY, TX, TY)

Parameters	Description	Min	Max	Units	Conditions
T_{JRMS}	Serial data output random jitter (RMS)		20	ps	RMS, tested on a sample basis. Measured with 1010 pattern.
T_{DJ}	Serial data output deterministic jitter (p-p)		100	ps	Peak-to-peak, tested on a sample basis. Measured with IDLE pattern.
$T_{SDR,}$ T_{SDF}	Serial data rise and fall		300	ps	20% to 80%, tested on a sample basis.

Tested per Figure 10.

Timing

This section will detail the timing requirements of all of the signals on the interface. All timing is measured into a lumped 35 pf capacitive load.

RBC[N] Timing

When LOCK_REF is pulled low, RCLKN should be in local phase lock with TBC within 500 µs. LOCK_REF, when activated, shall stay low for a duration of at least 500 µs if receiver frequency lock is to be expected. After local phase lock has been acquired, and when EWRAP is high, 2500 baud times after LOCK_REF is driven high, RCLKN shall be in phase lock with REFCLK. After local phase lock has been acquired, and when EWRAP is low, 250 baud times after LOCK_REF is driven high, RCLKN shall be in phase lock with the incoming serial data stream.

When a 62.5 MHz module is in frequency lock (either with REFCLK or a serial data stream) RCLKN shall never have a high level duration (>2.0 v) which is less than 6.0 ns, nor a low level duration (<0.8 v) which is less than 5.5 ns (no clock shivering shall occur). At byte realignment, RCLKN clock states are to be extended rather than truncated). When the S2047 is in frequency lock (either with REFCLK or a serial data stream) and LOCK_REF has been inactive for at least 2500 baud times the minimum instantaneous period shall always be greater that 16.0 ns. When the PLL is adjusting to a new phase or a new frequency, where both the old and new frequencies are valid Gigabit Ethernet frequencies, RCLKN shall never have a period less than 16.0 ns.

Figure 10. RCLKN Timing Diagram

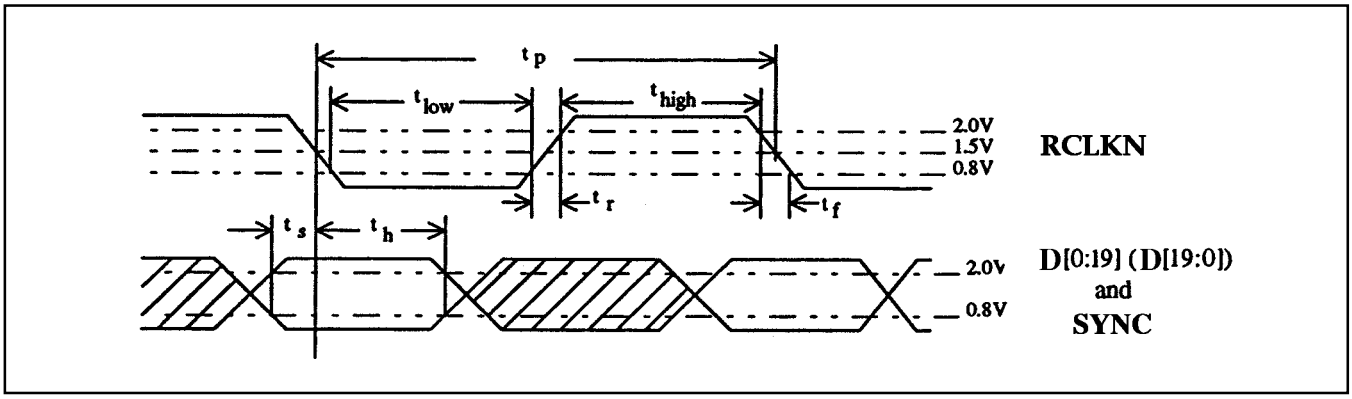


Table 13. Serial Data Input Timing Table (RLX, RLY; RX, RY)

Parameters	Description	Min	Max	Units	Conditions
R_{SDR} , R_{SDF}	Serial data input rise and fall	—	300	ps	20% to 80%.
T_{LOCK}	Data acquisition lock time @ <1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern sample basis
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤1E–12	30%	—	bit time	As specified in Fibre Channel FC–PH standard eye diagram jitter mask. (See Figure 12.) For BER ≤ IE-9 see Figure 14.

Table 14. RCLKN Timing Table

Parameter	Symbol	Min.	Max.	Units	Comments[2]
Frequency 62.50 MHz 125.0 MHz	f	62.49375 124.9875	62.50625 125.0125	MHz	This is dependent on the data path width.
Period in Lock	t_p	TBD		ns	In frequency lock[2].
Out of Lock Period (f=62.50 MHz)	t_{oolp}	TBD		ns	Not in frequency lock.
RCLKN Low Time	t_{low}	3.2		ns	
RCLKN High Time	t_{high}	3.2		ns	
RCLKN Duty Cycle		40%	60%	period	In frequency lock.
RX Setup to RCLKN	t_s	2.1		ns	
RX Hold from RCLKN	t_h	6.3		ns	
RCLK/RCLKN Rise Time	t_r	0.75	2.4	ns	This applies to the RCLKN output.
RCLKN Fall Time	t_f	0.7	3.0	ns	This applies to the RCLKN output.

1. All parameters are for outputs driven into a 35 pf lumped capacitive load.
2. This is the absolute minimum RCLKN period while in frequency lock and must account for any adjustments to the clock to allow for a change in phase or frequency on the received serial link.

Figure 11. Transmitter Timing Diagram

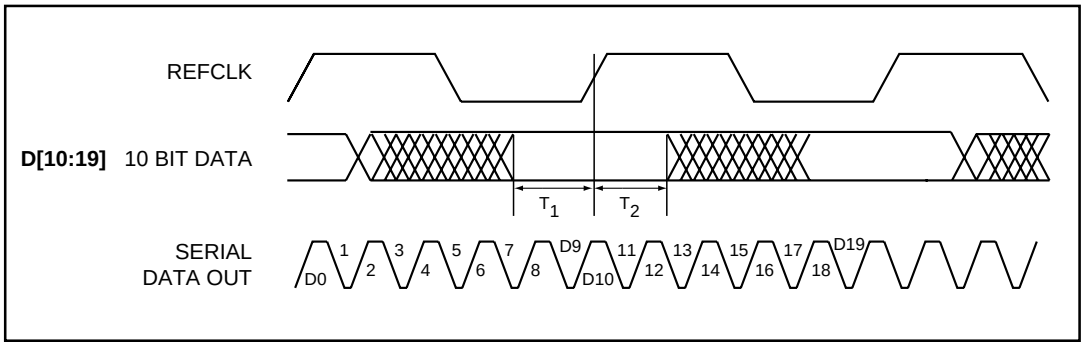


Figure 12. Receiver Timing Diagram

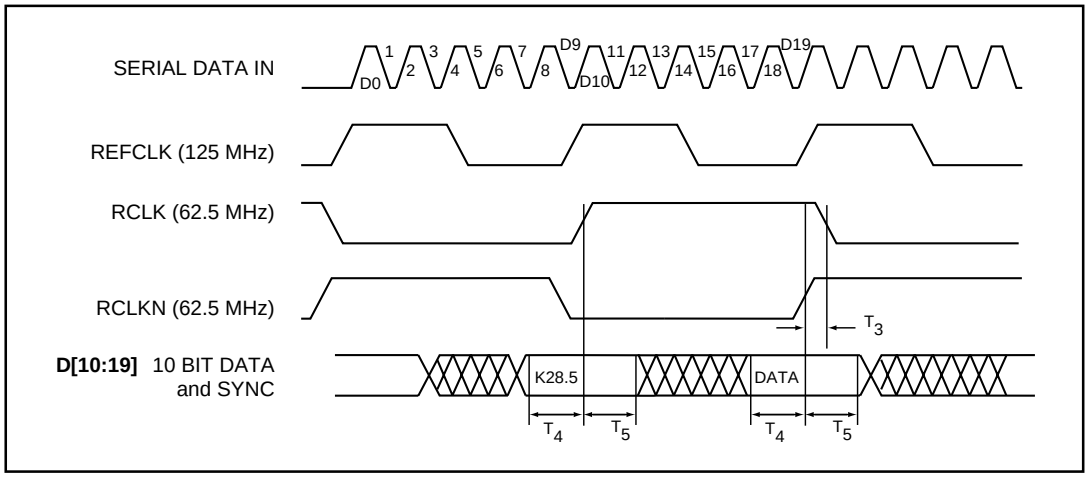


Table 15. S2046 Transmitter Timing

Parameters	Description	Min	Max	Units	Conditions
T_1	Data setup w.r.t. ↑REFCLK	2	—	ns	See note.
T_2	Data hold w.r.t. ↑REFCLK	1.5	—	ns	—

Note: All AC measurements are made from the reference voltage level of the clock (1.4 V) to the valid input or output data levels (0.8 V or 2.0 V).

Table 16. S2047 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T_3	RCLK to RCLKN skew	—	1	ns	Tested on a sample basis.
T_4	Data setup w.r.t. RCLK, RCLKN	3.0		ns	1.0625 GHz Mode
T_5	Data hold w.r.t. RCLK, RCLKN	1.5		ns	1.0625 GHz Mode

Max. Load = 15 pF.

ACQUISITION TIME

With the input eye diagram shown in Figure 11, the S2047 will recover data with a 10^{-9} BER within 50 bit times after an instantaneous phase shift of the incoming data. Note: This is only valid after a 10 ms initial reset has been applied on power up.

Figure 13. Serial Output Load

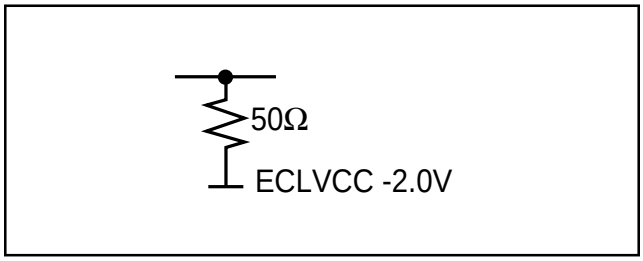


Figure 14. Receiver Input Eye Diagram Jitter Mask

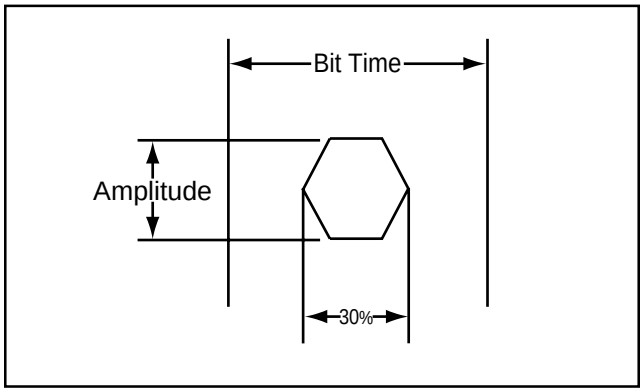
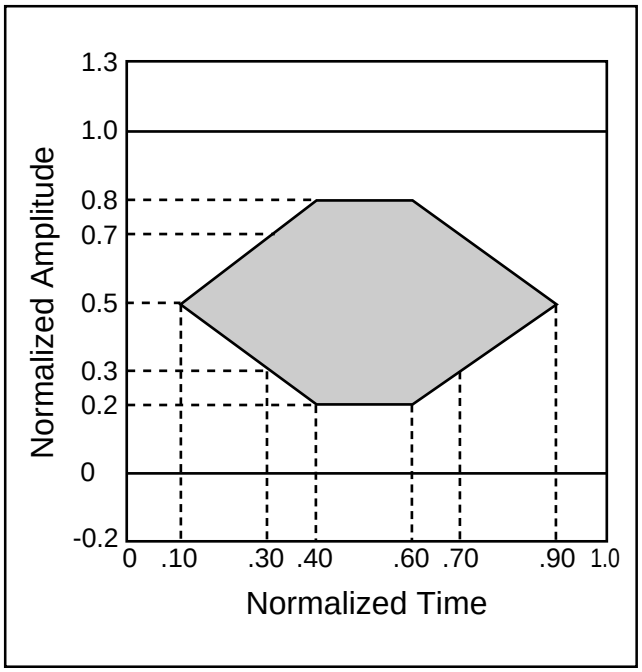


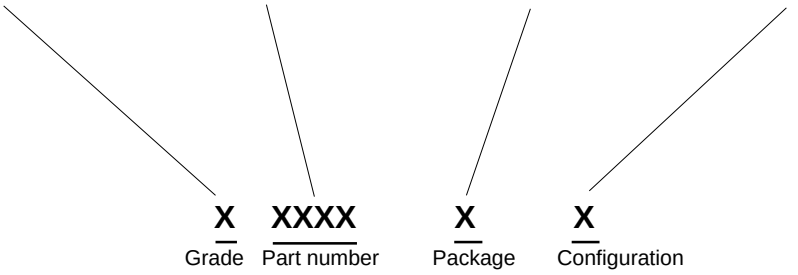
Figure 15. Acquisition Time Eye Diagram



Ordering Information

GRADE	TRANSMITTER	PACKAGE	SHIPPING CONFIGURATION
S – commercial	2046	B – 52 PQFP	Blank = trays /D = dry pack /TD = tape, reel, and dry pack

GRADE	RECEIVER	PACKAGE	SHIPPING CONFIGURATION
S – commercial	2047	B – 52 PQFP	Blank = trays /D = dry pack /TD = tape, reel, and dry pack



Example: S2046B-5—S2046 in a 52 PQFP package shipped in trays.

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