MTC-20125

Asymmetrical Digital Subscriber Loop (ADSL) Modem

Datasheet

Preliminary Information

Rev. 1.6 - Sept 1996

- Complies with ANSI T1E1.413 ADSL

Features

- Full digital modem chip for ADSL transmission.

The MTC-20125 performs the following functions in Receive Direction:

- Simplified Echo Cancelling on received input signals, sampled at 4.4 MHz;
- Decimation of the RX signal to sampling rate half the input rate, at 2.2 MHz;
- Time domain Equalizing and DMT symbol alignment;
- Time domain to Frequency conversion with FFT;
- Rotor and Frequency domain Equalizing;
- Demapping of the DMT carriers to a digital bit stream, at maximally 10 Mbit/s;
- Error and noise monitoring on individual carriers and pilot tones;
- Reed Solomon decoding and deinterleaving;
- DPLL function for tracking the received signal frequency deviations;
- 4 or 8 kbit/s extra monitor channel via pilot tone;
- Extra monitor channel via 16 bit word during the sync symbol (add-on to T1.E1 standard).

The MTC-20125 performs the following functions in Transmit Direction:

- Reed Solomon encoding and monitoring;
- Mapping a digital bit stream on DMT carriers, maximally 10 Mbit/s;
- Rotor and Frequency domain gain correction;
- Frequency to Time domain conversion with IFFT, sampling at 2.2 MHz, maximally 4.4 MHz;
- Time domain DMT symbol composing and filtering;
- Simplified Echo signal calculation;
- Interpolation of the TX signal to double the sampling rate from 2.2 MHz to 4.4 MHz;
- Simple 4 or 8 kbit/s extra monitor channel via pilot tone (add-on to T1.E1 standard);
- Extra monitor channel via 16 bit word during the sync symbol (add-on to T1.E1 standard).

General Description

System Overview

The MTC-20125 is used in both central office and remote applications, and is designed for sampling rates up to 4.4 MHz, with DMT symbols at 4 kHz and 2.2 MHz sampling. The clock frequency used by the MTC-20125 for internal digital signal processing is a maximum of 36 MHz.

Inside the MTC-20125 the Receive (RX) and the transmit (TX) parts are fully separated. There is a common part which deals with the DMT symbol alignment and frequency tracking.

At the front-end side the data enter digitally at a rate which is twice the sampling rate of the ADSL DMT symbols. The DMT symbol format is flexible and the symbol rate is variable, up to 4.3125 kHz.

The MTC-20125 is controlled and configured by an external microcontroller. All programmable coefficients and parameters are loaded by the controller. The ADSL initialization procedure is also under external control. Most of the control functions are slow, e.g. the updates of adaptive filters (TEQ, FEQ) are partially executed in the MTC-20125, but the final calculation and application of new filter values is under the control of the microcontroller, which can decimate the speed of the updates. The only fast control function in the system is the tracking of the pilot tone, and the DMT symbol time alignment. These functions are done by dedicated hardware, which include a DPLL with programmable filters and gains.

ALCATEL

Main Block Description

The main functional blocks used to realize the ADSL modem chip is shown in Figure 1. The following sections describe these in greater detail.

Mapper, Demapper, Monitor

Mapper and Demapper are two separate functions in the TX and RX direction. Each machine is a dedicated ALU that can perform the complete processing of a DMT symbol in less than 150 µs. The demapper includes a monitor function.

The mapper creates for a maximum of 256 carriers the bit constellation of the DMT symbol. The constellation of points are defined in the ADSL standard. The bits ordering with frequency carrier is not monotonic, in order to randomize the spectrum of signal sent to the line. The mapper uses 2 mapping tables in order to perform bitswapping when the SNR deteriorates. The mapper is activated by the DTSU unit which controls the real time operation. The data is received from the Reed Solomon encoder.

The demapper is a fixed point operator. For received carriers, the demapper projects the constellation received on a square grid representing the transmitted constellation. The demapper is able to extract constellation from 1 to 14 bits with a maximum number of 256 carriers. It uses 2 mapping tables for bitswapping. The demapper delivers the data to the Reed Solomon blocks with a constant number of bits, except when synchronization signals are received.

The monitor block performs the measurement of the signal characteristics of a DMT tone. The noise, carrier to noise and distortion are measured. The result of the measurement is used to adjust the coefficient of the adaptive filter, the equalizer and the Echo canceller.

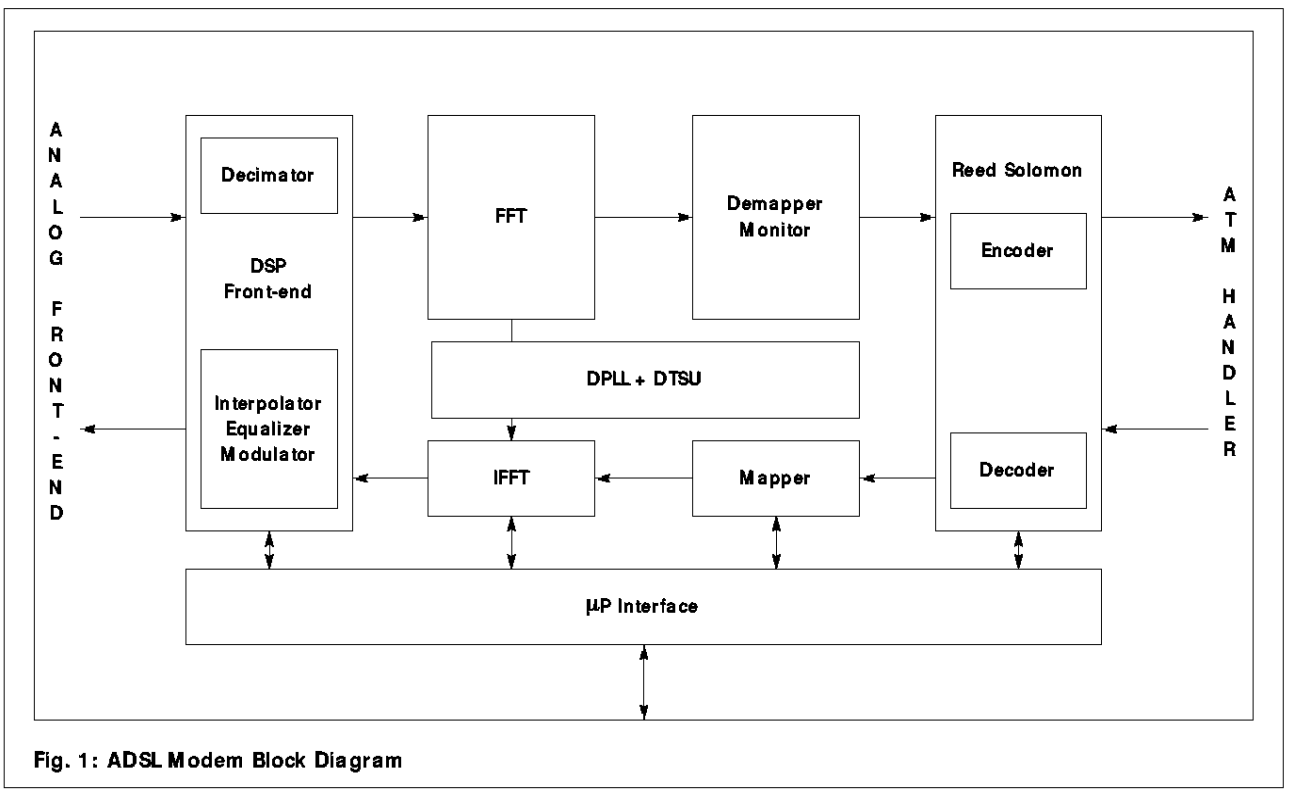

Fig. 1: ADSL Modem Block Diagram

DMT Symbol Timing Unit (DTSU) & Digital Phase Locked Loop (DPLL)

The DTSU activates the slave peripherals for the RX and TX and controls the real time operation of them. The DTSU block is composed of two coupled programmable state machines, one for the TX, one for the RX. The state machines are configured by the microcontroller. The DTSU performs 2 types of function: the time keeper to maintain the real time operation and a scheduler to control the different operation to perform by the modem. The time keeper is based on the 2.2 MHz or 4.4 MHz clock generated from the DSP front-end.

The DPLL controls all clock tuning and trimming. In RX, it controls and tracks the clock of the incoming symbols by monitoring and filtering the symbols. For the definition of the master there are 3 possible configurations. RX or TX is the master of the clock and respectively TX or RX is slave. These are the loop timing situations on the ADSL specification. There is a 3rd mode where both directions are using an independent clock, provided the frequency difference is less than 5 ppm.

Fast Fourier Transform (FFT), Inverse FFT (IFFT)

The FFT block is used for the DMT carrier demodulation in the RX and for the modulation in the TX direction. There is a machine for the RX FFT machine and one for the TX (IFFT). It is a dedicated programmable machine capable of processing one DMT symbol in less than 250 µs. It is based on a dedicated pipeline multiplier accumulator ALU performing 70 million Multiplications per second.

In the RX path, the FFT transforms the time domain DMT symbol into a frequency domain. The FFT is preceded by a Frequency Equalizer (FEQ) to fine tune the gain of different carrier and correct the phase as well as a Rotor block to adjust the frequency error between the received signal and the local clock system.

In the TX path, the IFFT transforms the DMT symbol generated in the frequency domain into the time domain equivalent. The IFFT block is followed by a fine gain tuning block and a Rotor function to adjust the frequency error between local clock system. The FFT module is a slave DSP engine controlled by the microcontroller. It is working off line and communicates with the other blocks via buffers controlled by the DTSU block. The FFT executes a program that is stored in the RAM area. Calculation coefficients are also contained within the same RAM area.

DSP Front-end

The DSP front-end contains the interface block with the analog front-end circuit (MTC-20124) as well as the system clock generator. It contains a parallel and serial interface, the clock generation circuit and the echo cancellation filter.

The interface to the analog front-end is configurable into 2 modes: a parallel interface and a serial interface which both are capable of transmitting the data in the TX and RX direction. The parallel interface uses the 2.2 to 4.4 MHz clock to transmit 16 bit wide words. The data are transmitted by 2 separate blocks to the RX and TX on the base on nibble (4 bits) clocked 4 times the data word clock.

In the case of the serial interface, the data transmitted is the oversampled Pulse Density Modulated (PDM) signal resulting from the sigma delta conversion. The sigma delta converters use an oversampling ratio of 1:16 (35.2 to 70.4 MHz). For the TX part, the interpolator equalizer and digital sigma delta modulator are included in this chip. For the RX part, the circuit contains the digital circuitry to combine and decimate down to the 2.2 MHz word clock the 3 PDM signal coming out of the analog sigma delta modulator. This last block is included in the analog front-end chip. More details of the converter architecture can be found in the Analog Front-end circuit (MTC-20124) description.

Reed Solomon (RS) Coder Decoder

The RS section contains a block for the transmit and for the receive path of the circuit. In the TX part, the RS block contains the interleaving and encoding of the data that is then transmitted to the Mapper block. In the RX part, the RS block contains the de-interleaving block and the decoding of the data. The basic time interval in the RS part of the circuit is the DMT symbol time. In each DMT symbol, 3 slots of 1050 cycles are reserved for the RS encoding. One slot is used for the fast encoding and 2 are reserved for the interleaved data encoding. The remainder of the 5500 cycles are allocated to the data. The RS encoding of the interleaved data is only performed when all the previously encoded data has been transmitted from the buffer to the mapper. This can be up to 16 DMT symbols.

In the TX part, the same base of one DMT symbol is used for the decoding. The decoding of interleaved data is performed only when the complete data of one RS code is received (which is up to 16 symbols).

In the same DMT symbol, 3 RS decodes are performed. The depth of interleaving can be programmed up to a maximum of 72. The code word size of it is a maximum 256. A Scrambler descrambler is implemented into the chip in order to randomize the data traffic before being processed by the RS block. This function can be enabled or disabled within the Function enable register.

Interfaces

In this section the different interfaces of the modem are described.

SLAP: interface to the ATM back-bone chip (MTC-20125).

OBC: microcontroller and RAM interface. The specification given in this document is related to the intel i960 microprocessor.

Analog Front-end: interface to the MTC-20124.

VCXO: interface to the VCXO embedded in the MTC-20124.

JTAG: standard IEEE1149.1 JTAG interface for self-test purpose.

SLAP

The modem output interface is based on the SLAP interface. The interface provides a bidirectional link based on the transmission of bytes. Bytes are sent in series on two lines. One is used for the odd bits, the other is used for even bits, with LSB first. The data is exchanged on the base of a common transfer clock. The clock used for this interface is the modem system clock. The maximum clock frequency is 35 MHz.

The transmit part uses separate lines for the fast and the interleaved data. 4 control signals are used for the TX and for the RX parts. Control signals are interleaved and fast data transmit request, DMT symbol start and RS word start.

SLAP Interface

Pins & Functional Description

Table 1:

Name	Pin	Type	Function
SIT_DATA_0_I	4	I	SLAP data input - Interleaved
SIT_DATA_1_I	5	I	SLAP data input - Interleaved
SIT_DATA_0_F	7	I	SLAP data input - Fast
SIT_DATA_1_F	9	I	SLAP data input - Fast
SIT_REQ_I	2	O	RS/encoder Byte Request
SIT_REQ_F	11	O	RS/encoder Byte Request
SIT_RS	13	O	RS/encoder start word, added to be compliant with ANSI requirement
SIT_SYNC	12	O	Superframe sync, added to be compliant with ANSI specifications

Table 2:

Name	Pin	Type	Function
SIR_DATA_0	26	O	SLAP data output
SIR_DATA_1	28	O	SLAP data output
SIR_VAL_I	21	O	RS/decoder data valid indication
SIR_VAL_F	24	O	RS/decoder data valid indication
SIR_RS	19	O	RS/encoder start word, added to be compliant with ANSI specifications
SIR_SYNC	17	O	Superframe sync, added to be compliant with ANSI specifications

Dynamic Characteristics

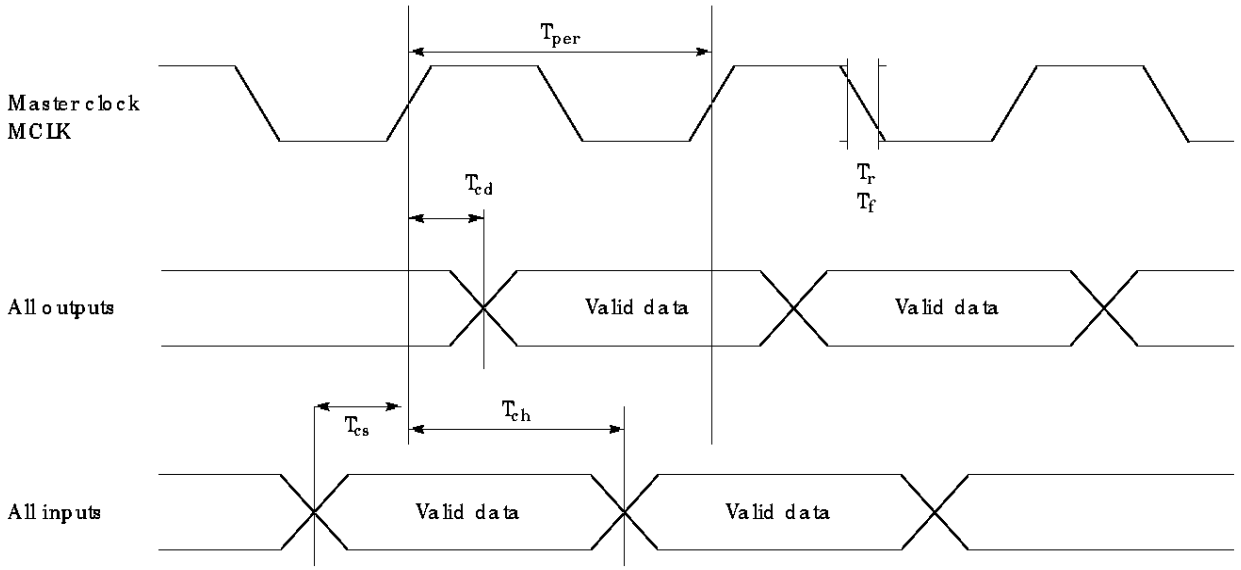

Fig. 2: SLAP intefa ce: timing relation

MCLK

Table 3:Characteristics of the MCLK Clock

Symbol	Parameters	Min	Typ	Max	Unit
T_{per}	Clock period		28.7		nsec
t_r, t_f	Rise, fall time (10% - 90%)			2.5	nsec
t_{clkd}	Internal mclk clock to external MCLK output delay			4	nsec

The timing is specified with a load of 30 pF and the levels are CMOS compatible.

Input & Output Signal Specification

All input & output signals of the SLAP interface are specified with respect to the MCLK output clock.

Table 4: SLAP Intefa ce: Input & Output Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
T_{cd}	MCLK to output delay	0		6	nsec
T_{cs}	Input to MCLK setup time	8			nsec
T_{ch}	Input to MCLK hold time	0			nsec

The timing is specified with a load of 30 pF and the levels are CMOS compatible.

Microprocessor Interface

The modem supports a simple microprocessor interface to communicate with the microprocessor bus. The interface acts as a standard asynchronous multiplexed bus structure. This interface does not support burst mode access.

The RAM access procedure is as follows:

Writing is by writing the contents to the RAM_DATA_i register and accessing the RAM_ADDRESS register.

Reading is by accessing the RAM_ADDRESS register and reading the content to the RAM_DATA_i register.

The word width is not constant.

All RAM locations can be accessed except the coefficient for the front-end part.

Table 5: Pins & Functional Description

Name	Type	Function
AD[15:0]	IO	Multiplexed address - data bus bits 15 to 0
ALE	I	Address latch enable
WNR	I	Write not read indication
CSB	I	Chip select
RDYRCVB	OD	Ready, active low open drain output
INTB or INTRXB or INTTXB	OD	Interrupt

Dynamic Characteristics

Address / Data Bus Specification

Table 6: Address with Respect to ALE

Symbol	Parameters	Min	Typ	Max	Unit
t_r, t_f	Rise, fall time (10% - 90%)			4	ns
T_{alew}	ALE pulse width	0.5 Tc - 3			ns
T_{avs}	Address valid setup time	0.5 Tc - 3			ns
T_{avh}	Address valid hold time	0.5 Tc - 3			ns

Tc = 1 period of the system clock T_{per} (= OBC clock period)

Address and ALE both generated on the rising edge of the system clock, ALE is only high during the 1st half of the period.

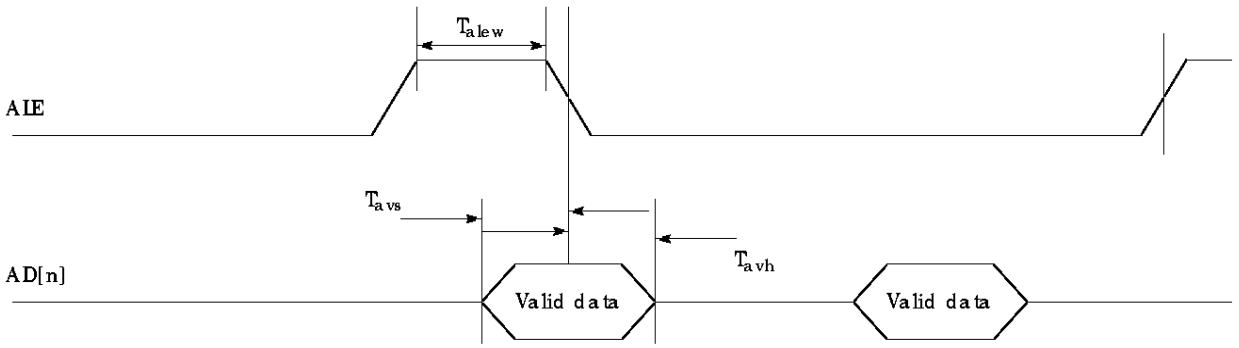

Fig. 3: Address versus ALE timing

The timings are specified with a load of 100 pF and the levels are CMOS compatible.

Table 7: Data Input with Respect to the Clock

Symbol	Parameters	Min	Max	Unit
T_{dh}	Data write hold time (25 MHz i960)	5		ns
T_{ds}	Data write setup time (25 MHz i960)	17		ns
T_{dh}	Data write hold time (33 MHz i960)	5		ns
T_{ds}	Data write setup time (33 MHz i960)	8		ns

Table 8: Data Input with Respect to the Clock

Symbol	Parameters	Min	Max	Unit
T_{zd}	Data active delay from clock, Z to data (25 MHz i960)	3	28	ns
T_{ds}	Data inactive delay from clock, data to Z (25 MHz i960)	3	28	ns
T_{zd}	Data active delay from clock, Z to data (33 MHz i960)	3	18	ns
T_{dz}	Data inactive delay from clock, data to Z (33 MHz i960)	3	18	ns

Table 9: W / RB Input Specification with Respect to the Clock (from µcontroller)

Symbol	Parameters	Min	Max	Unit
T_{wrs}	Setup WRB to system clock (25 MHz i960)	5		ns
T_{wrs}	Setup WRB to system clock (33 MHz i960)	17		ns
T_{wrh}	Hold WRB to system clock (25 MHz i960)	5		ns
T_{wrh}	Hold WRB to system clock (33 MHz i960)	8		ns

Table 10: CSB Input Specification with Respect to the Master Clock (OBC_mclk)

Symbol	Parameters	Min	Max	Unit
T_{css}	Setup CSB to system clock	13		ns
T_{csh}	Hold CSB to system clock	1		ns

Table 11: RDYRVC Output with Respect to the Master Clock (OBC_mclk)

Symbol	Parameters	Min	Max	Unit
T_{zrd}	RDYRCV active delay from clock, Z to 0 (25 MHz i960)	3	26	ns
T_{rdz}	RDYRCV inactive delay from clock, o to Z (25 MHz i960)	3	26	ns
T_{zrd}	RDYRCV active delay from clock, Z to 0 (33 MHz i960)	3	16	ns
T_{rdz}	RDYRCV inactive delay from clock, o to Z (33 MHz i960)	3	16	ns

Table 12: INT, INTRX & INTTX Outputs with Respect to the Master Clock (OBC_clock)

Symbol	Parameters	Min	Max	Unit
T_{dint}	Interrupt output delay from clock (25 MHz i960)	3	28	ns
T_{dint}	Interrupt output delay from clock (25 MHz i960)	3	18	ns

Analog Front-end

Pins & Functional Description

Table 13: MTC-20124 Interface: Pinning

Pin name	Type	Function per mode		
		No PDMP	PDMP @ 3 kHz	PDMP @ 4.4 kHz
RXD[0]	I	RX data nibble input bit 0	Not used	
RXD[1]	I	RX data nibble input bit 1	Receive PDM data, PDM0 signal from the first Σ/Δ section	
RXD[2]	I	RX data nibble input bit 2	Receive PDM data, PDM1 signal from the second Σ/Δ section	
RXD[3]	I	RX data nibble input bit 3	Receive PDM data, PDM3 signal from the last Σ/Δ section	
TXD[0]	O	TX data nibble input bit 0	Transmit PDM data	
TXD[1]	O	TX data nibble input bit 1	Not used	
TXD[2]	O	TX data nibble input bit 1	Not used	
TXD[3]	O	TX data nibble input bit 1	Not used	
CLKM	I	49.152 MHz clk, used in MTC-20125, div. by 2	49.152 MHz clk, used in MTC-20125, div. by 2	35.328 MHz clk, used in MTC-20125, no division
CLKPDM	I	Not used (PDMP module clock)	49.152 MHz clk, (PDMP module clock)	52.992 MHz clk, (PDMP module clock)
CLNIBRX	I	RX nibble clock	Not used	
CLNIBTX	I	TX nibble clock	Not used	
CLWDRX	I	RX word clock	Not used	
CLWDTX	I	TX word clock	Not used	
OFLW	I	MTC-20124 overflow indication	Not used	
ACTI	I	ADSL activation detection		
PDOWN	O	Power down		
AGCOUT	O	AGC coefficient controlling output, synchronous to the word clock		

Dynamic Characteristics

CLWDRX & RXD[n] in relation to CLNIBRX (mode = no internal PDMP filter)

Table 14: MTC-20124 Inteface: Characteristics of the Outputs

Symbol	Parameters	Min	Typ	Max	Unit
T_{nibper}	Clock period		56		nsec
	Clock duty cycle	40		60	%
t_r, t_f	Rise, fall time (10% - 90%)			3	nsec
T_{nibs}	CLW DRX and RXD setup to CLNIBRX falling edge	5			nsec
T_{nibh}	CLW DRX and RXD hold to CLNIBRX falling edge	12			nsec

The timings are specified with a load of 100 pF and the levels are CMOS compatible.

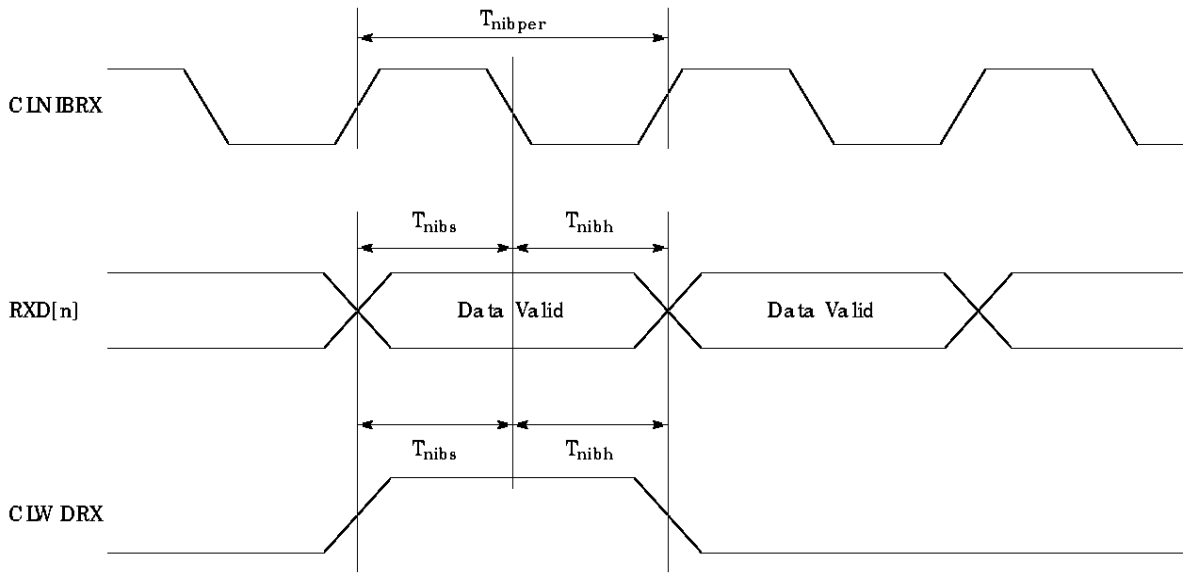

Fig. 4: MTC-20124 Inteface: Timing of the RXD and CLWDRX Inputs

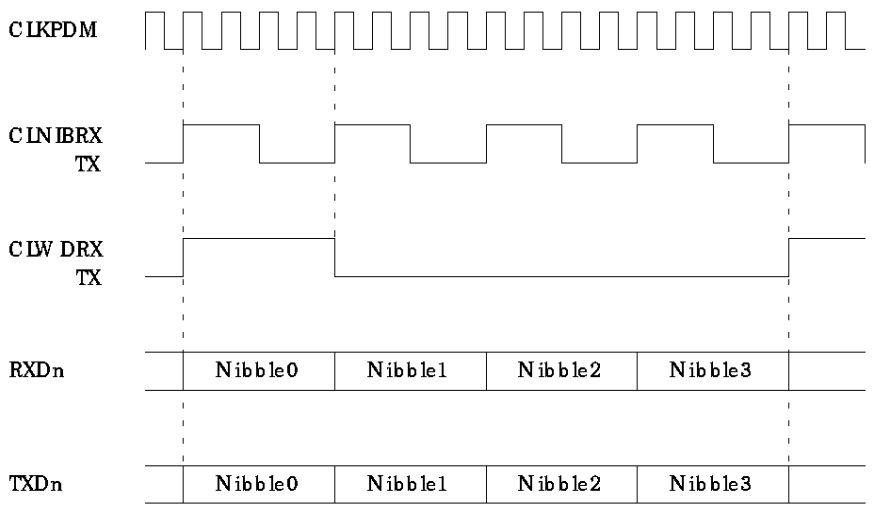

Fig. 5: MTC-20124 Interface: Functional Relationship

CLWDRX & RXD[n] in relation to CLNIBRX (mode = internal PDMP filter used)

Table 15: MTC-20124 Interface: Characteristics of the Outputs

Symbol	Parameters	Min	Typ	Max	Unit
T_{pdmper}	Clock period		18.9		nsec
	Clock duty cycle	40		60	%
t_r, t_f	Rise, fall time (10% - 90%)			3	nsec
T_{pdms}	RXD setup to CLKPDM falling edge	2			nsec
T_{pdmh}	RXD hold to CLKPDM falling edge	3			nsec

The timings are specified with load of 100 pF and the levels are CMOS compatible.

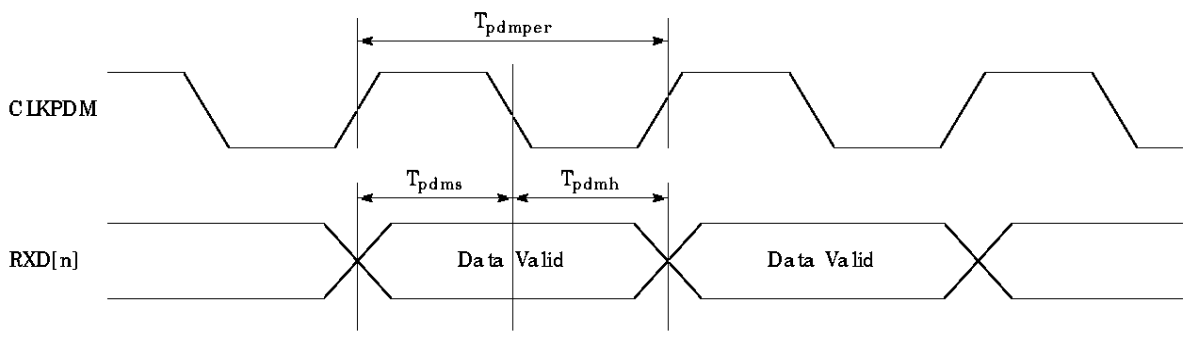

Fig. 6: MTC-20124 Interface: Timing of the RXD

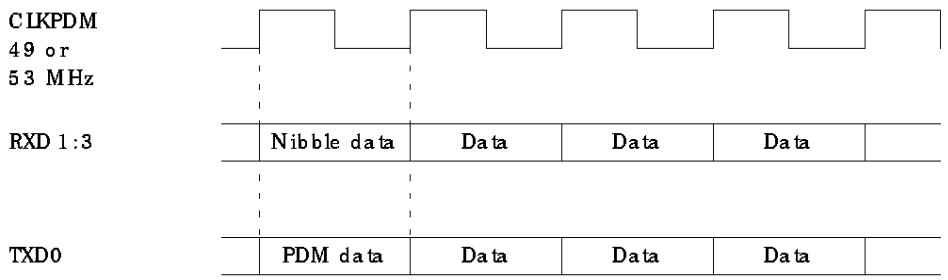

Fig. 7: MTC-20124 Interface: Internal PDMP Filter used

TXD in relation to CLNIBTX
(mode = no internal PDMP filter)

Table 16: MTC-20124 Interface: Output Delay with Respect to CLNIB

Symbol	Parameters	Min	Typ	Max	Unit
T_{nibper}	CLNIBTX clock period		56		nsec
T_{nibd}	Data delay with respect to CLNIBTX rising edge			18	

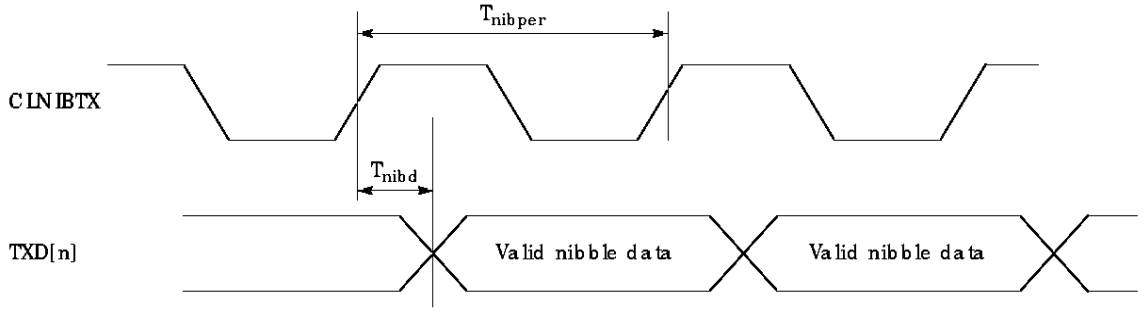

Fig. 8: MTC-20124 Interface: Output Delay with Respect to CLNIBTX

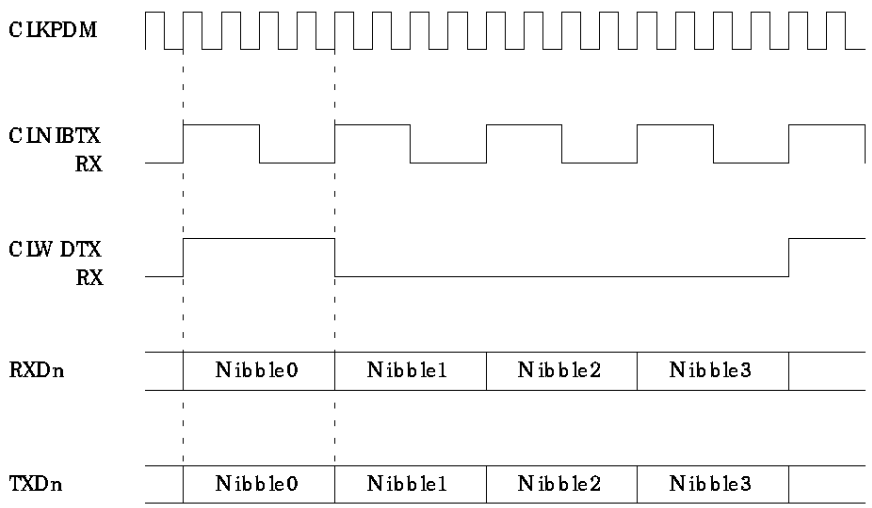

Fig. 9: MTC-20124 Interface: no Internal PDMP Filter

TXD in relation to CLKPDM
(mode = internal PDMP filter used)

Table 17: MTC-20124 Interface: Output Delay with Respect to CLKPDM

Symbol	Parameters	Min	Typ	Max	Unit
T_{pdmper}	CLKPDM clock period		18.9		nsec
T_{pdmd}	Data delay with respect to CLKPDM rising edge			9	

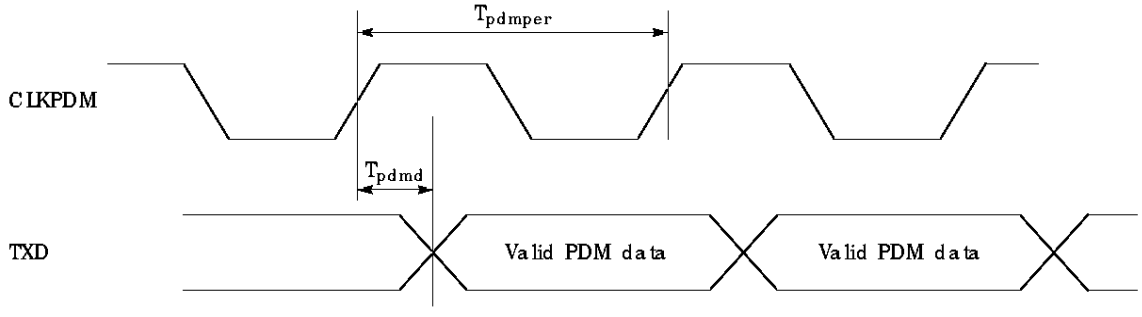

Fig. 10: MTC-20124 Interface: Output Delay with Respect to CLKPDM

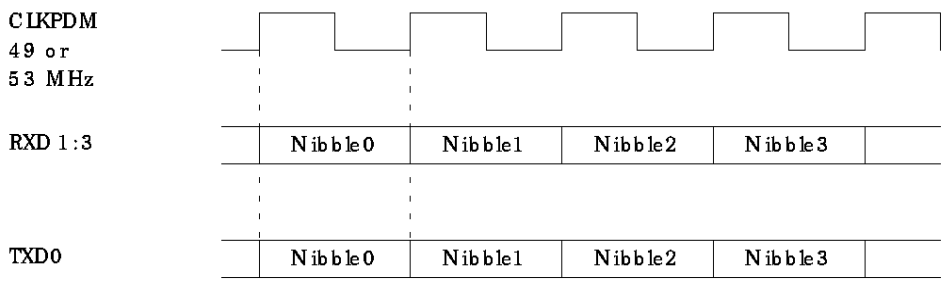

Fig. 11: MTC-20124 Interface: Internal PDMP Filter used

AGCOUT in relation to CLNIB

Table 18: MTC-20124 Interface: Output Delay with Respect to CLNIB

Symbol	Parameters	Min	Typ	Max	Unit
T_{nibper}	CLNIBTX clock period		56		nsec
T_{nibd}	Data delay with respect to CLNIBTX rising edge			18	

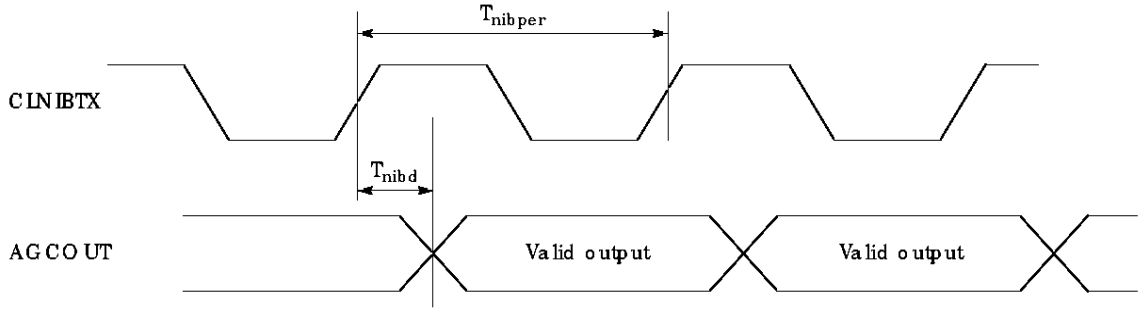

Fig. 12: MTC-20124 Interface: Output Delay with Respect to CLNIBTX

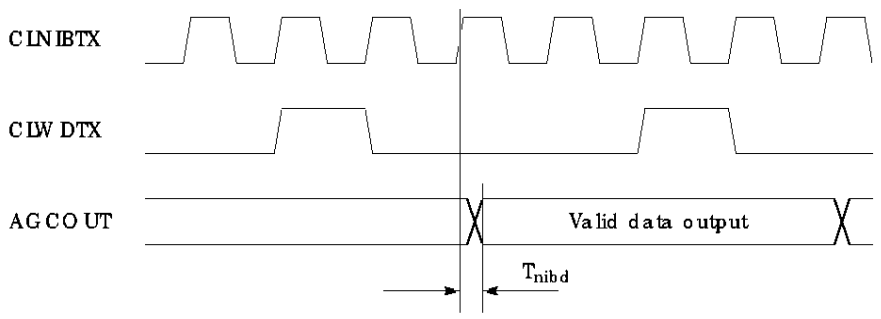

Fig. 13: MTC-20124 Interface: Output Delay with Respect to CLWDTX

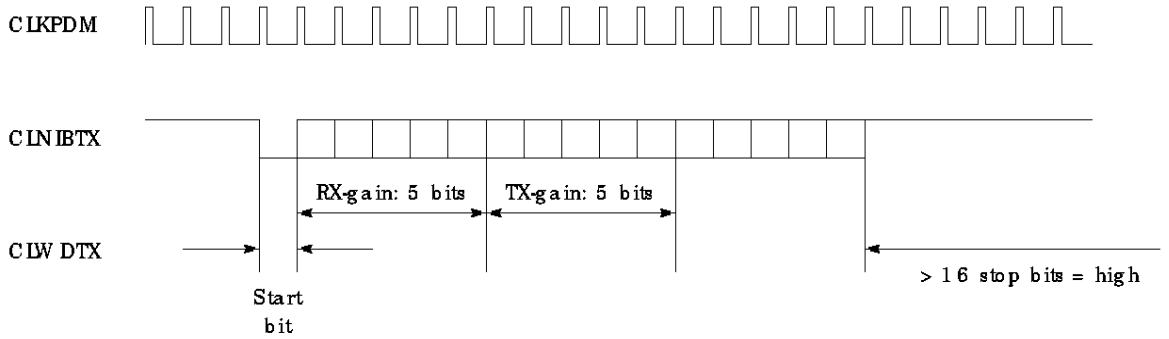

Fig. 14: MTC-20124 Interface: AGCOUT Functional Relation (for all Modes)

Other MTC-20124 signals

The ACTI and PDOWN (activation and power down to MTC-20124) are asynchronous.

VCXO Interface

Pins & Functional Description

Table 19:

Name	Type	Function
VCO_CLK	O	VCO clock, synchronous to mclk_rchap output
VCO_DATA	O	VCO data, synchronous to the mclk_rchap output
VCO_LATCH	O	VCO latch pulse, to be used in the PCM case, synchronous to the mclk_rchap output

Dynamic Characteristics

Output signal specification

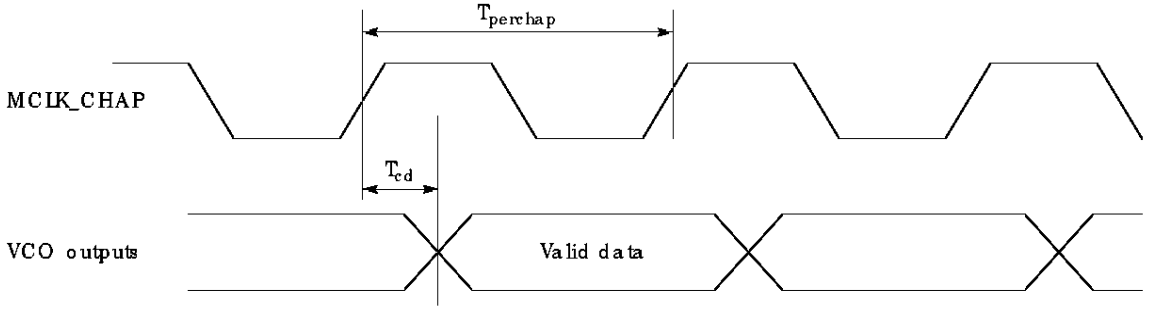

Fig. 15: VCXO Intefa ce: Timing Rela tionship

Table 20:MTC-20125 Intefa ce: Output Cha racteristics

Symbol	Parameters	Min	Typ	Max	Unit
T_{cd}	MCLK_RCHAP to output delay	0		6	nsec

The timing is specified with a load of 30 pF and the levels are CMOS compatible.

JTAG Interface

Description

The MTC-20125 is equipped with a Test Access Port according to IEEE Std. 1149.1 [13]. The intention of boundary scan test support is to enable a test of on-board interconnections and ASIC production tests. Consequently, the TAP interface can be driven only in case of off-line test.

The external interface of the TAP contains the signal TDI, TDO, TCK, TMS and TRST* as defined in the IEEE standard.

The interface from the board to the on-chip Test Access Port is the TAP bus, consisting of five signals:

The standard bus: **TDI, TDO, TCK, TMS** and **TRST**

TRST is explicitly required, since in functional mode TCK will not be active. To guarantee a correct functional operation of the IC, the register that controls the signal in the interface between the TAP controller and the device logic must have an asynchronous reset.

Table 21: Pins & Functional Description

Name	Type	Function	Pin no
HARD_RESETB	I	Master reset active low	88
SIF_TST_RAM	ID	Test pin: ram self test	98
SCAN_EN	ID	Test pin: scan enable	97
TRST	ID	Test pin: tap controller reset	95
TMS	IU	Test pin: test mode selection	93
TDO	OZ	Test pin: test output	92
TDI	IU	Test pin: test input	91
TCK	IU	Test pin: test clock	90
TESTIN0 (RXD0)	I	Scan chain 0 input	107
TESTOUT0 (AGCOUT)	O	Scan chain 0 output	105
TESTIN1 (RXD1)	I	Scan chain 1 input	110
TESTOUT1 (TXD3)	O	Scan chain 1 output	124
TESTIN2 (RXD2)	I	Scan chain 2 input	112
TESTOUT2 (TXD2)	O	Scan chain 2 output	126
TESTIN3 (RXD3)	I	Scan chain 3 input	113
TESTOUT3 (TXD1)	O	Scan chain 3 output	128
TESTIN4 (CLWDTX)	I	Scan chain 4 input	115
TESTOUT4 (TXD0)	O	Scan chain 4 output	131
TESTIN5 (CLNIBTX)	I	Scan chain 5 input	117
TESTOUT5 (VCO_CLK)	O	Scan chain 5 output	133
TESTIN6 (CLWDRX)	I	Scan chain 6 input	119
TESTOUT6 (VCO_DATA)	O	Scan chain 6 output	135
TESTIN7 (CLNIBRX)	I	Scan chain 7 input	120
TESTOUT7 (VCO_LATCH)	O	Scan chain 7 output	138

Dynamic Characteristics

Table 22: JTAG Inteface: Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
T_{TCK}	Clock period		100		ns
t_r, t_f	Rise, fall time (10% - 90%)		5		ns
Tw_H, Tw_L	Clock pulse width		50		ns
Td_D	Data delay	0		20	ns
Ts_D	Data setup	10			ns
Th_D	Data hold	10			ns

The input levels are CMOS compatibles, the output levels are CMOS compatible. The timings are specified with a load of 15 pF.

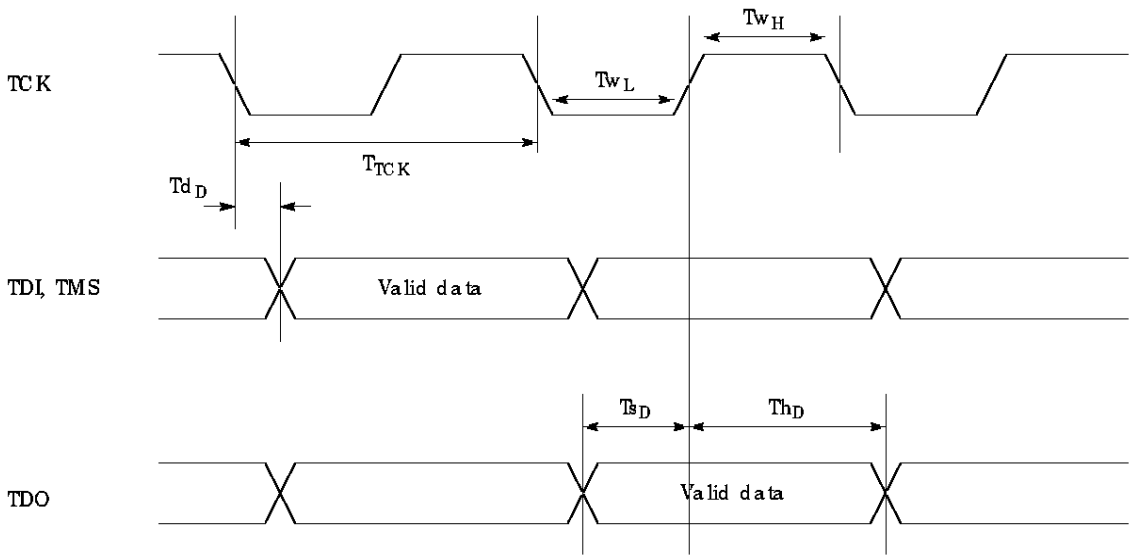

Fig. 16: JTAG Inteface: Timing

MTC-20125 Pinning

VSS = 0 V
VDD = 3.3 V

The power supply can be
double bonded.

Pin no	Function	Pin name	Description
1	VSS		Power connection GND, 0V
2	O	SIT_REQ_I	TX RS/encoder byte request - Interleaved
3		Not connected	
4	I	SIT_DATA_0_I	TX SIAP interface - data in 0 Interleaved
5	I	SIT_DATA_1_I	TX SIAP interface - data in 1 Interleaved
6		Not connected	
7	I	SIT_DATA_0_F	TX SIAP interface - data in 0 Fast
8	VDD		Power connection 3.3 V
9	I	SIT_DATA_1_F	TX SIAP interface - data in 1 Fast
10		Not connected	
11	O	SIT_REQ_F	TX RS/encoder byte request - Fast
12	O	SIT_SYNC	TX Superframe Synchronisation Signal
13	O	SIT_RS	TX RS/encoder Start word indicator
14		Not connected	
15	VSS		Power connection GND, 0V
16		Not connected	
17	O	SIR_SYNC	RX Superframe Synchronisation Signal
18		Not connected	
19	O	SIR_RS	RX RS/encoder Start word indicator
20		Not connected	
21	O	SIR_VAL_I	RX RS/encoded data valid indication
22	VDD		Power connection 3.3 V
23		Not connected	
24	O	SIR_VAL_F	RX RS/encoded data valid indication
25		Not connected	
26	O	SIR_DATA_0	RX SIAP interface - data out 0
27		Not connected	
28	O	SIR_DATA_1	RX SIAP interface - data out 1
29	VSS		Power connection GND, 0V
30		Not connected	
31	O	MCLK_CHAP	Clock output to the CHAP device
32		Not connected	
33	IO	AD_0	Address data bus - bit 0
34		Not connected	
35	IO	AD_1	Address data bus - bit 1
36	VDD		Power connection 3.3 V

Pin no	Function	Pin name	Description
37	VSS		Power connection GND, OV
38		NC	
39	IO	AD_2	Address data bus - bit2
40		NC	
41	IO	AD_3	Address data bus - bit3
42		NC	
43	IO	AD_4	Address data bus - bit4
44	VDD		Power connection 3.3 V
45		NC	
46	IO	AD_5	Address data bus - bit5
47		NC	
48	IO	AD_6	Address data bus - bit6
49		NC	
50	IO	AD_7	Address data bus - bit7
51	VSS		Power connection GND, OV
52		NC	
53	IO	AD_8	Address data bus - bit8
54		NC	
55	IO	AD_9	Address data bus - bit9
56		NC	
57	IO	AD_10	Address data bus - bit10
58	VDD		Power connection 3.3 V
59		NC	
60	IO	AD_11	Address data bus - bit11
61		NC	
62	IO	AD_12	Address data bus - bit12
63		NC	
64	IO	AD_13	Address data bus - bit13
65	VSS		Power connection GND, OV
66		NC	
67	IO	AD_14	Address data bus - bit14
68		NC	
69	IO	AD_15	Address data bus - bit15
70		NC	
71	I	AIE	Address latch enable
72	VDD		Power connection 3.3 V

Pin no	Function	Pin name	Description
73	VSS		Power connection GND, 0V
74	I	CSB	Chip select
75	I	WNR	Write not read
76		NC	
77	OD	RDYRCVB	Ready / receiver busy
78	OD	INTTXB	Interrupt (TXB)
79		NC	
80	VDD		Power connection 3.3 V
81	OD	INTRXB	Interrupt (RXB)
82		NC	
83	OD	INT	Interrupt
84		NC	
85	I	OBC_MCLK	Microprocessor interface Master clock
86		NC	
87	VSS		Power connection GND, 0V
88	I	HARD_RESETB	Master Reset to device (active low)
89		NC	
90	ID	TCK	JTAG IEEE1149.1 clock
91	IU	TDI	JTAG IEEE1149.1 Data in
92	O	TDO	JTAG IEEE1149.1 Data out
93	IU	TMS	JTAG IEEE1149.1 mode select
94	VDD		Power connection 3.3 V
95	ID	TRST	JTAG Tap controller Reset
96		NC	
97	ID	SCAN_EN	Scan enable test pin
98	ID	SLF_TST_RAM	RAM Self-test pin
99		NC	
100	O	PDOWN	Analog front-end power down signal
101	VSS		Power connection GND, 0V
102	I	ACTI	ADSL activation indication
103		NC	
104	I	CLKM	AFE master clock
105	O	AGCOUT	AFE - AGC coefficient control
106		NC	
107	I	RXD0	Receive data nibble 0
108	VDD		Power connection 3.3 V

Pin no	Function	Pin name	Description
109	VSS		Power connection GND, 0V
110	I	RXD1	Receive data nibble1 or PDM1 data
111		NC	
112	I	RXD2	RX data nibble2 or PDM2 data
113	I	RXD3	RX data nibble3 or PDM3 data
114	I	OFLW	Overflow indication from MTC-20124
115	I	CLWDTX	Transmit word clock
116	VDD		Power connection 3.3 V
117	I	CLNIBTX	Transmit nibble clock
118		NC	
119	I	CLWDRX	Receive word clock
120	I	CLNIBRX	Receive nibble clock
121		NC	
122	I	CLKPDM	PDM module clock
123	VSS		Power connection GND, 0V
124	O	TXD3	Transmit data nibble3 or PDM3 data
125		NC	
126	O	TXD2	Transmit data nibble2 or PDM2 data
127		NC	
128	O	TXD1	Transmit data nibble1 or PDM1 data
129		NC	
130	VDD		Power connection 3.3 V
131	O	TXD0	Transmit data nibble0
132		NC	
133	O	VCO_CLK	VCXO clock
134		NC	
135	O	VCO_DATA	VCXO data
136		NC	
137	VSS		Power connection GND, 0V
138	O	VCO_LATCH	VCXO latched output data
139		NC	
140	ID	NC	
141		NC	
142	ID	TESTCLK1	Test clock input 1
143	ID	TESTCLK2	Test clock input 2
144	VDD		Power connection 3.3 V

Chip Package

The chip is packaged into a 144 pin PQFP package. Pin names can be found in the pinning section.

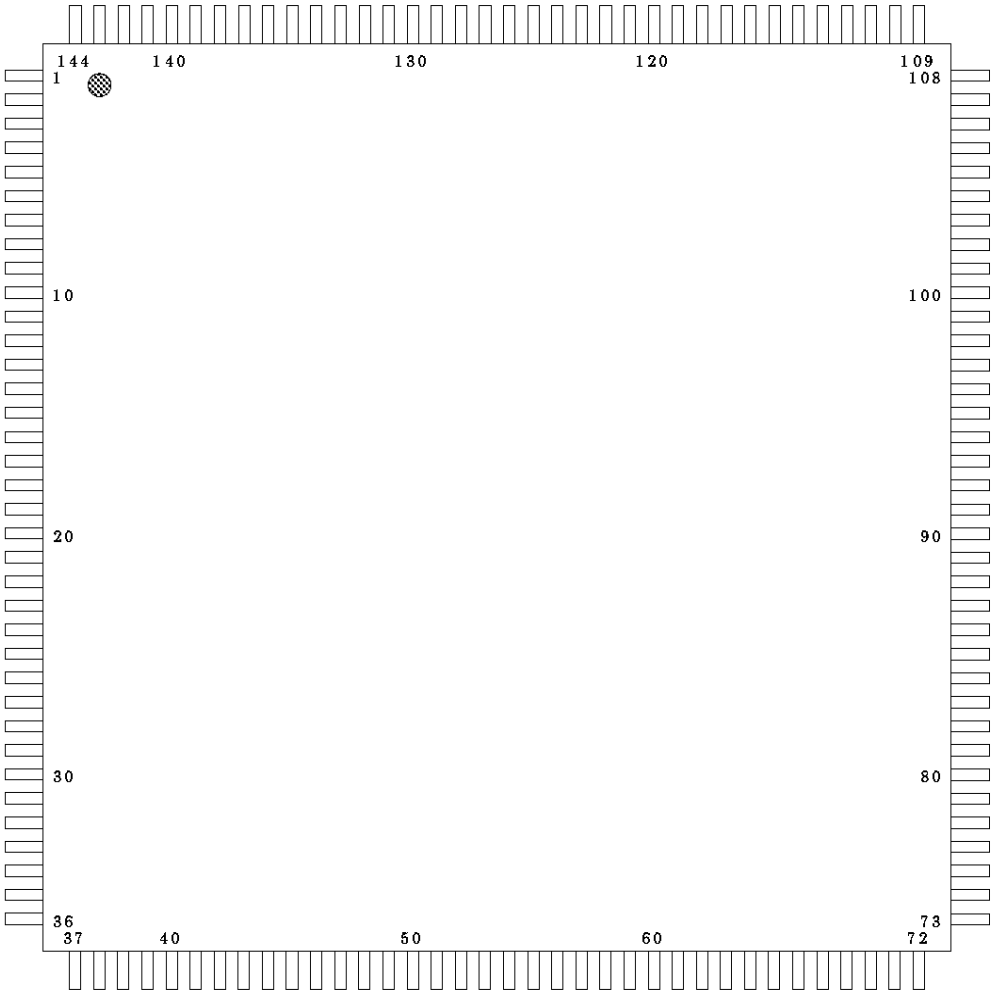

Fig. 17: Chip Package: 144 Pin PQFP

Reference to Alcatel Mietec Package Handbook PB 026a 3/96

Clock Sampling and Data Rate

	ADSL standard				MTC chip set			
Basic data rate	4 kbit/s				4 kbit/s *			
Basic data rate at Reed-Solomon en/decoder	4 8 kbit/s = 32 kbit/s				4 8 kbit/s = 32 kbit/s			
Guardtime overhead	17/16				17/16 (programmable)			
Sync cell overhead	69/68				69/68 (programmable)			
Carrier spacing	4.3125 kHz				4.3125 kHz			
Max num. downlnk carriers	255				255 **			
Act. num. downlnk carriers	Depends on filters and FDM or EC				T.b.d. (flexible filters)			
Max. num. uplnk carriers	31				128			
Act. num. uplnk carriers	Depends on filters and FDM or EC				T.b.d. (flexible filters)			
SAMPLING RATES	IFFT (TX)	MTC-20124 (TX)	MTC-20124 (RX)	FFT (RX)	IFFT (TX)	MTC-20124 (TX)	MTC-20124 (RX)	FFT (RX)
Min. downlnk sampl rate	2208 kHz				2208 kHz			
Act. downlnk sampl rate	-	-	-	-	4416	4416	4416	2208
Min. uplnk sampling rate	276 kHz				276 kHz			
Act. uplnk sampling rate	-	-	-	-	2208	4416	2208	1104
MTC-20124 master clock rate	-				52992 kHz			
MTC-20125 master clock rate	-				35328 kHz			

* Early version MTC-20124 limited to 3 kHz.

15 carriers, when a passive POTS Splitter, with higher edge of the ADSL high-pass, is used.

* Highest 10 carriers are influenced by the decimation filter.

Electrical, Physical and Environmental Characteristics

Electrical Ratings and Characteristics

Absolute Maximum Ratings

Limiting capabilities are those parameter limits above which damage to the integrated circuit may occur. It is not implied that more than one of these conditions can be applied simultaneously.

Transient Energy Capability

ESD

a) During power-on or power-off surges, the device withstands -7 V on the VDD line for up to one second.

b) During testing, output pins withstand being shorted to either VDD or GND, for up to one second (min. 1 minute between events).

c) The MTC-20125 is compliant with the ALCATEL standard 1AB 00000 0043 QTZZA, with a limit voltage of 1500 V, and with the ALCATEL standard 1AB 00000 0044 QTZZA, with a limit voltage of 250 V.

Latch-up

The MTC-20125 is compliant with the ALCATEL standard 1AB 00000 0046 QTZZA, with a limit current of 100 V.

Thermal Data

The junction to ambient thermal resistance RthA when mounted on a horizontal printed board in still air is 25-26°C/W without a heat spreader, and less than 22°C/W with heat spreader.

Table 23: Maximum Ratings

Symbol	Parameters	Min	Max	Unit
VDD	VDD supply voltage, related to GND	-0.4	5	V
Vin	Voltage at any input pin	VSS -0.5	VDD +0.5	V
Vout	Voltage at any output pin	VSS -0.5	VDD +0.5	V
Tstg	Storage temperature	-65	150	°C
TL	Lead temperature (10 second soldering)		300	°C
ILU	Latch-up current	100		mA
I	DC current drain per I/O pin		50	mA
I	DC current drain per VDD/VSS pin		75	mA

Operating Conditions

Unless specified, the characteristic limits of Static characteristics in this document and Dynamic characteristics apply over an operating temperature range of 0° C to 110° C and for VDD within the range: +4.50 V to +5.50 V ref. to GND.

Table 24: Operating Conditions

Symbol	Parameter description	Min	Typ	Max	Unit
VDD	VDD supply voltage, related to GND	3.15	3.30	3.45	V
Vin, Vout	Voltage at any input and output pin	0		VDD	V
Pd	Power dissipation			1.6	W
Ta	Ambient temperature	-25	85	110	°C
T_j	Junction temperature	-25		110	°C

The ambient temperature when testing the device on ATE equipment shall be raised in function of the test time as to guarantee the same chip temperature as on board level at 70° C ambient.

To guarantee the lifetime of the component, the junction temperature must be below the typical value for 95% of the time.

Static characteristics

Power Supply

Table 25: Static Power Consumptions

Symbol	Parameter	Test conditions		Typ	Max	Unit
IVDD	Supply * current	Clock and frame applied	VDD = 3.3 V	1 mA	-	mA
			VDD = 3.45 V	TBD	-	mA
IVDDF		Clock not applied VDD = 3.45 V		TBD	-	mA

Digital inputs

- CMOS compatible

Table 26: DC Characteristics Digital Inputs

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
VIL	Low level input voltage				0.3*VDD	V
VIH	High level input voltage		0.7*VDD			V
IIH	Input leakage current	Vin = VSS, VDD	-10		10	µA
OIZ	Tri-state leakage current	Vin = VSS, VDD	-10		10	µA
C_{inp}	Input capacitance				5	pF

Digital outputs

- Hard driven outputs

Table 27: DC Characteristics - Digital Outputs

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
VOL	Low level output voltage	I_{out} = -4 mA			0.5	V
VOH	High level output voltage	I_{out} = 4 mA	VDD-0.5			V
C_{out}	Output capacitance				7	pF

- TRI-STATE outputs

Table 28: DC Characteristics-iTstate Digital Outputs

Symbol	Parameters	Test conditions	Min	Max	Note	Unit
VOL	Low level output voltage			0.5		V
IOLD	Low level output current	VOL= 1 V	80			mA
IOHD	High level output current	VOH = 2.3 V	-80			mA
CO	Output capacitance			7		pF
VOH	High level output voltage		Vdd-0.5			V
IOZ	3-state output current			10		µA

MTC-20125

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