PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MJ1472

PCM RECEIVING CIRCUIT

The MJ1471 1742 1473 circuits have been designed specifically for use in 30 channel PCM systems. All circuits conform to the appropriate CCITT recommendations. The range of circuits is realised in N-channel MOS technology. They all operate from a single 5V supply and all inputs and outputs are TTL compatible. Operating speed of 2.048MHz is guaranteed over 0°C to 70°C temperature range.

The MJ1472 block diagram is shown in Figure 2.

FEATURES

- Line Time Generation (From 9 Stage Clock Driven Counter)
- Line Timing, Frame Alignment
- Alarm Signals FAT + MIR, ATL, AW, EPAT
- Test Points TP1, TP2, TP3, MR
- Inputs and Outputs LSTTL Compatible

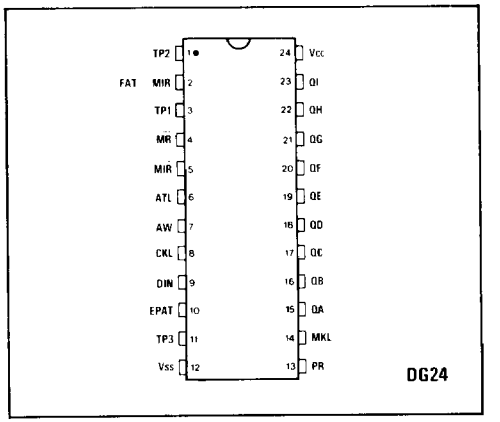

Fig.1 Pin connections (top view)

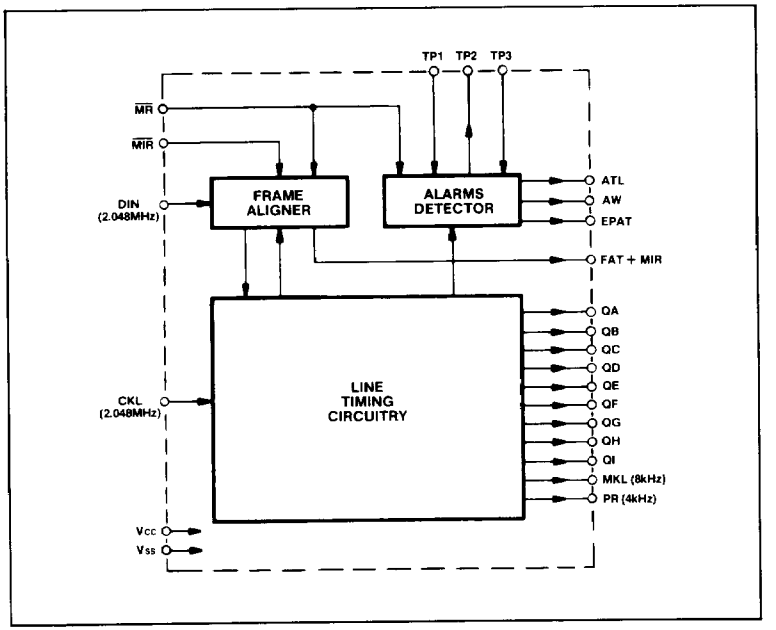

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0° C to +70° C
Package thermal resistance 60° C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	All inputs	2.7			V	I_{OH} -60μA
Low-level output voltage	V_{OL}	All inputs			0.5	V	I_{OL} = 0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25° C
High-level output current	I_{OH}	All outputs	-60			μA	V_{OH} = 2.7V
Low-level output current	I_{OL}	All outputs	0.8			mA	V_{OL} = 0.5V
Input capacitance	C_{IN}	All inputs			10	pF	1MHz 100mV
Supply current	I_{CC}			40	60	mA	V_{CC} = 5.25V

AC CHARACTERISTICS

Propagation delays	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Q_A to Q_I	t_{pd1}			50	ns	Fig 5 for loading Measure from CKL LE
MKL & PR	t_{pd2}			100	ns	As above
ATL & FAT + MIR	t_{pd3}			100	ns	As above
AW	t_{pd4}			300	ns	As above
EPAT	t_{pd5}			100	ns	Fig 5 for loading Measure from TP3 LE
TP2	t_{pd6}			150	ns	Fig 5 for loading Measure from TP1 TE
TP2	t_{pd7}			250	ns	Fig 5 for loading Measure from CKL LE
Required delay from DIN transition to CKE TE	t_1	50		430	ns	

FRAME ALIGNMENT

Frame alignment is described by the flow chart of Figure 3 where the A and B words are defined.

Position	1	2	3	4	5	6	7	8
Word A	X	0	0	1	1	0	1	1
Word B	X	1	X	X	X	X	X	X

Table 1

A(TA) represents the presence of word A in TSO of frame TA. B(TB) likewise represents the presence of word B in TSO of frame TB. $\bar{A}$(TA) and $\bar{B}$(TB) represent the absence of the words in TSO of the respective frame.

Frame alignment is assumed lost when 3 consecutive words A(TA) or B(TB) have been received with error. Frame alignment is recovered when the following sequence is detected in successive frames. Word A → word B (TB) and finally A(TA). To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of an imitative frame alignment signal, the following procedure is followed. Should A(TA) be followed by absence of word B(TB) a new search for A is started a frame later.

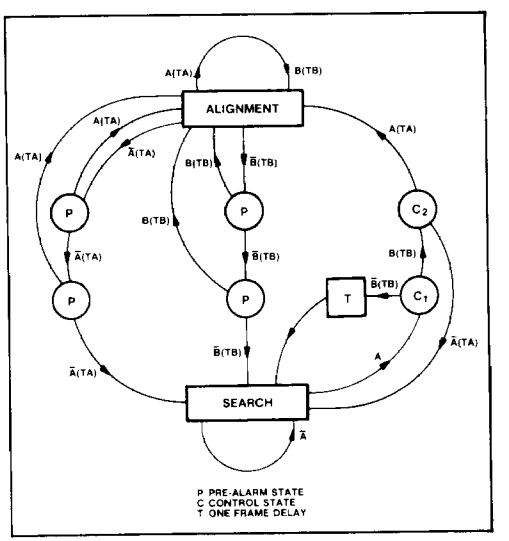

Fig.3 Frame alignment procedure

LINE TIMING

Nine stage clock (CKL) driven counter. All outputs (QA to QI) available externally.

MKL One bit positive pulse corresponding to 8th bit of TS15.

PR One bit positive pulse corresponding to position 8 of TS30 of frame A.

TRANSMISSION ALARM DETECTION

As already outlined in Fig.3. Three consecutive words A(TA) or B(TB) set an R-S flip-flop. This condition can also be forced by the external signal MIR.

MIR Input to R-S flip-flop.

FAT + MIR Output indication of state of R-S flip-flop.

ATL Output high when logic '1' is detected in position 3 of TS0, TB for two consecutive TB frames. Output low when logic '0' is detected in position 3 of TS0, TB. ATL output inhibited by the presence of output FAT + MIR.

AW Output high whenever $\bar{A}$(TA) is detected. Output is removed only when word $\bar{A}$(TA) is detected.

EPAT The output is high when for eight consecutive times at least 15 words A(TA) are detected in 512ms. EPAT alarm is removed (EPAT = 0) when less than 15 $\bar{A}$(TA) words are detected in (512 x 8)ms. The 512ms timer interval is obtained by an 11 bit binary counter clocked every double frame.

TEST POINTS

TP1, TP2, TP3 and Master Reset MR are test points.

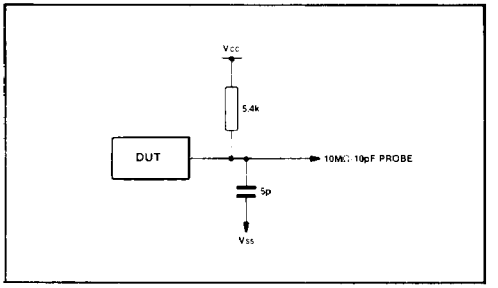

Fig.4 Propagation delay test circuit

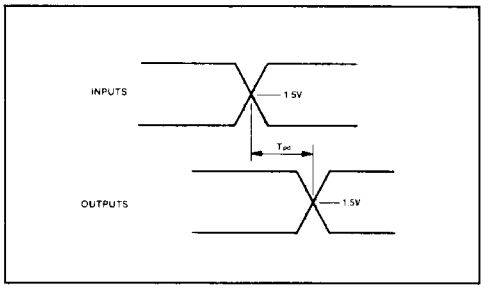

Fig.5 Waveforms for tpd