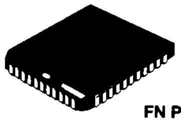
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MCM62950A

32K x 9 Bit Synchronous Static RAM



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62950A is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, high-speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). Asynchronous controls consist of asynchronous write enable ($\overline{AW}$) and output enable ($\overline{G}$). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

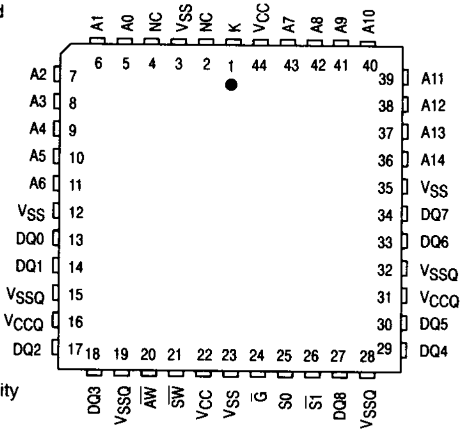
Addresses (A0 – A14) and control signals, except output enable ($\overline{G}$) and asynchronous write enable ($\overline{AW}$), are sampled through positive-edge-triggered noninverting registers. Data outputs are asynchronously controlled by $\overline{G}$.

Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of K. Write cycles are completed only if $\overline{AW}$ is asserted within the specified setup time to the following rising edge of K. Write cycles may be aborted by negating the $\overline{AW}$ signal prior to the low going edge of K. Data for the write may be delayed until the latter half of the write cycle.

The MCM62950A is packaged in a 44-pin plastic-leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output switching. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 15/20/25 ns Max and Cycle Times: 15/20/25 ns Min
- Internal Input Registers (Address, Control)
- Late Write Abort Feature
- Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

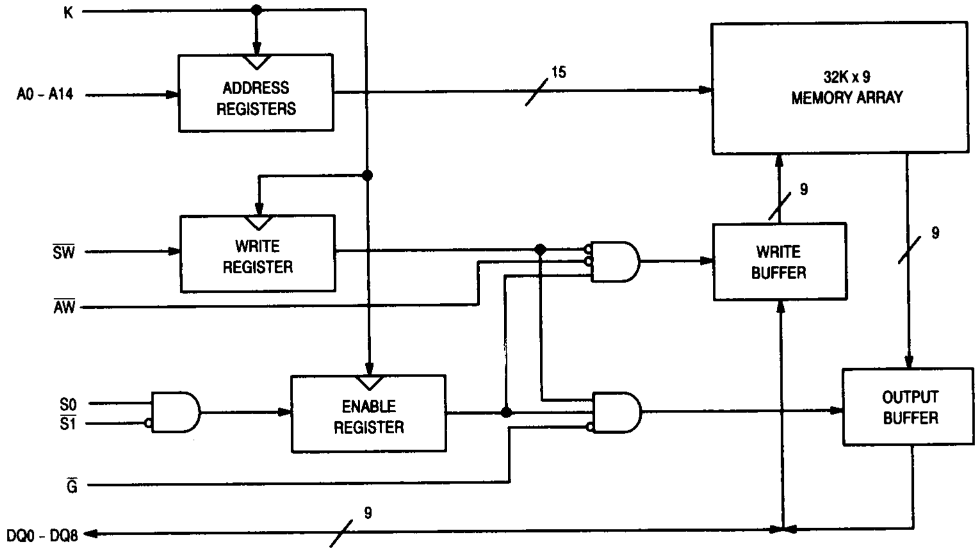
PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{SW}$	Synchronous Write
$\overline{AW}$	Asynchronous Write
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BLOCK DIAGRAM



SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{SW}$	$\overline{AW}$	$\overline{G}$	K	Operation	I/O Status
F	X	X	X	L-H	Deselected	High-Z
T	L	X	X	L-H	Write	High-Z
(T)	(L)	L	X	L	Write	Data-In
(T)	(L)	H	X	L	Aborted Write (No Action)	High-Z
T	H	X	—	L-H	Read Initiated	—
(T)	(H)	X	H	X	Read	High-Z
(T)	(H)	X	L	X	Read	Data Out

NOTES:

1. X means Don't Care.
2. S0, $\overline{S1}$, and $\overline{W}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. $\overline{W}$ = (L) implies $\overline{W}$ = L for the last clock transition from low to high. Similarly for S = (T).

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	− 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V, t_{KHKH} = 15 ns)	P_D	1.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	− 0.5*	0.0	0.8	V

* V_{IL} (min) = − 3.0 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G}$, S0 = V_{IH}, $\overline{S1}$ = V_{IL}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) t_{KHKH} = 15 ns	I_{CCA}	—	—	170	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH})	I_{SB1}	—	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} − 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} − 0.2 V or ≤ 0.2 V, Cycle Time ≥ t_{KHKH} min)	I_{SB2}	—	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	0.1	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	—	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, $T_A = 0$ to $+ 70$°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level .... 1.5 V
Input Pulse Levels .... 0 to 3.0 V
Input Rise/Fall Time .... 3 ns
Output Timing Reference Level .... 1.5 V
Output Load .... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM62950A-15		MCM62950A-20		MCM62950A-25		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Control:								ns	
Cycle Time	t_{KHKH}	15	—	20	—	25	—		
Clock High Pulse Width	t_{KHKL}	6	—	8	—	11	—		
Clock Low Pulse Width	t_{KLKH}	6	—	8	—	11	—		
Read Access Times:								ns	
Clock Access Time	t_{KHQV}	—	15	—	20	—	25		
Output Enable to Output Valid	t_{GLQV}	—	6	—	8	—	9		
Aborted Write Cycles:								ns	
Clock Low to Asynchronous Write High	t_{KLAWH}	—	0	—	0	—	0		
Clock High to Asynchronous Write Invalid	t_{KHAWX}	2	—	2	—	2	—		
Write Cycles:								ns	
Asynchronous Write Low to Clock High	t_{AWLKH}	5	—	6	—	6	—		
Clock High to Asynchronous Write Invalid	t_{KHAWX}	2	—	2	—	2	—		
Data-In Valid to Clock High (Transparent Data)	t_{DVKH}	5	—	6	—	6	—		
Clock High to Data Invalid (Transparent Data)	t_{KHDX}	2	—	2	—	2	—		
Output Buffer Control:								ns	
Clock High to Output Low-Z after Write	t_{KHQX1}	6	—	6	—	6	—		
Clock High to Output Change	t_{KHQX2}	5	—	5	—	5	—		
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—		
Output Disable to Q High-Z	t_{GHQZ}	—	6	—	8	—	9		4
Clock High to Q High-Z	t_{KHQZ}	—	6	—	6	—	6		4
Register Setup Times for: Address	t_{AVKH}	2	—	2	—	2	—	ns	5
Synchronous Write	t_{WVKH}								
Chip Select	t_{S0VKH} t_{S1VKH}								
Register Hold Times for: Address	t_{KHAX}	2	—	2	—	2	—	ns	5
Synchronous Write	t_{KHWX}								
Chip Select	t_{KHS0X} t_{KHS1X}								

NOTES:

1. A read cycle is defined by $\overline{SW}$ high for the setup and hold times. A write cycle is defined by $\overline{SW}$ low for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{SW}$ is sampled low.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.
5. This is a synchronous device. All address inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) when the device is selected. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) when the device is selected. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

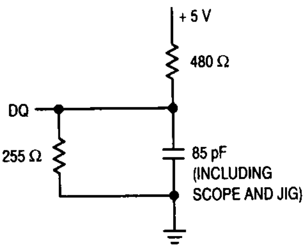


Figure 1A

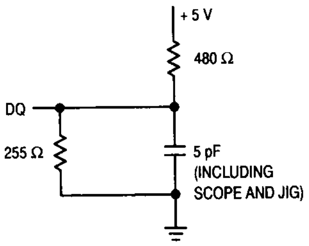
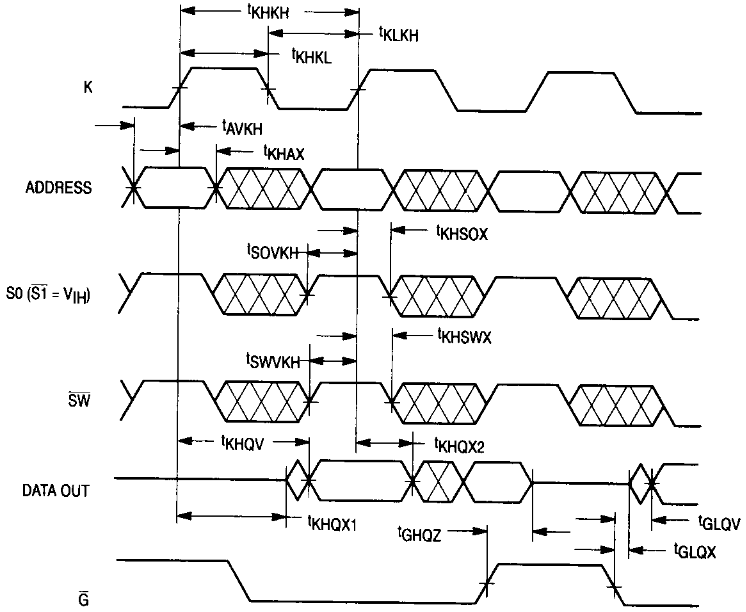
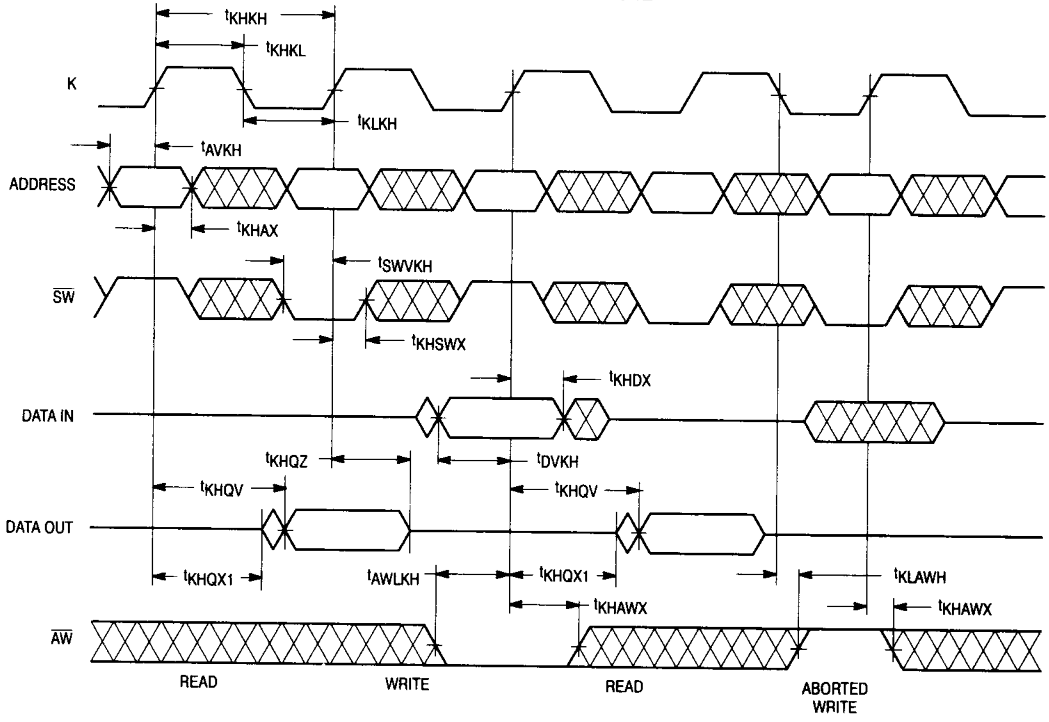


Figure 1B

READ CYCLE

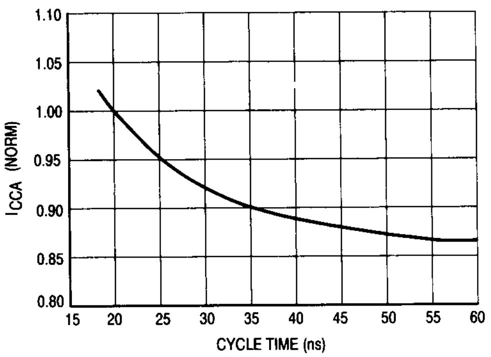


READ-WRITE-READ CYCLE

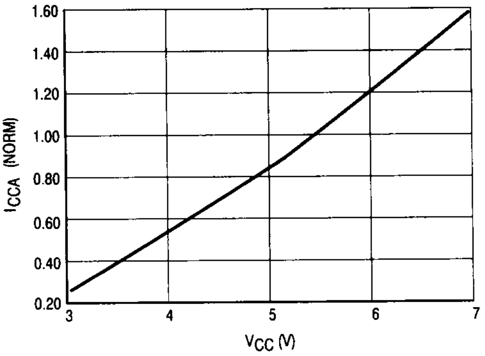


DERATING CURVES

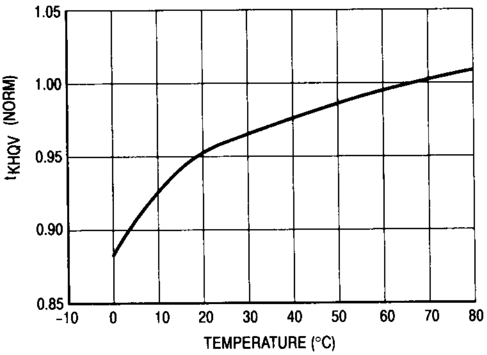
(Derating Curves Are Based On Component Typical Values)



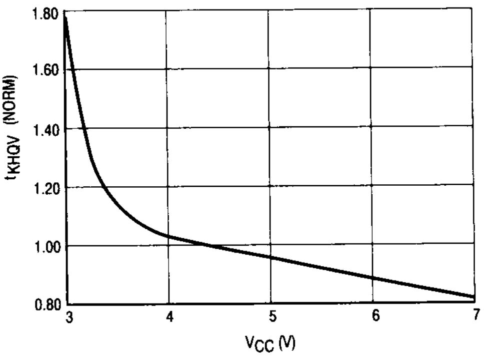
I_{CCA} vs Cycle Time



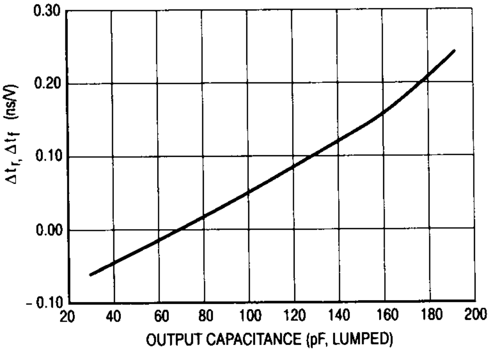
I_{CCA} vs V_{CC}



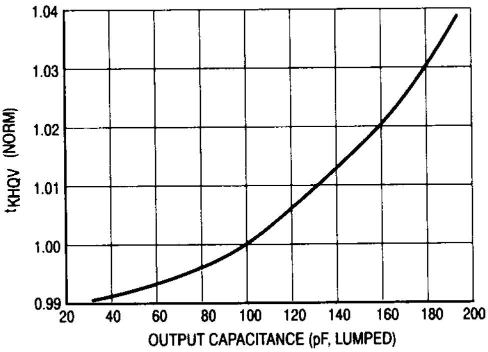
KHQV vs Temperature



KHQV vs V_{CC}



Change in Output Rise/Fall Times vs Output Capacitance



KHQV vs Output Capacitance

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62950A X XX

Motorola Memory Prefix — MCM
Part Number — 62950A
Package (FN = PLCC) — X
Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns) — XX

Full Part Numbers — MCM62950AFN15 MCM62950AFN20 MCM62950AFN25