High Performance SRAM Modules

Features

- 256K and 512K secondary cache module family using Synchronous and Asynchronous SRAM for PowerPC applications
- Organized as a 32K or 64K x 72 package on a 4.05" x 1.0", 136-lead, Dual Read-out DIMM for SSRAM and as 32K x 64 package for ASRAM
- Available in linear (PowerPC™) burst modes
- Operation fro 50 MHZ to 66 MHZ supported
- Fast access times: 9 and 11ns using SSRAM; 12ns using ASRAM
- Byte Parity
- Individual Byte Write control
- Low capacitive address, control, clock, and data bus loading
- Single +3.3V or +5V, +/- 5% power supply
- 5V-tolerant common data I/O
- Uses AMP Connector P/N 5-382617-8

Description

The IBM family of 512KB synchronous SRAM modules use IBM's burstable, high performance 0.5 micron, CMOS Static RAMs that are versatile and can achieve up to 9ns access. The 512KB modules integrate four 64K x 18 burst SRAMs. The burst mode operation of these modules support PowerPC-based systems and is available for either +3.3V or +5V applications. The 256KB ASRAM module offers a cost/performance optimization for +5V applications.

These IBM family of Cache modules support operation upto 66MHZ. Outputs are 5V tolerant and LVTTL compatible. The Cache family is presently designed to support PowerPC controllers, however, Cache family of modules for Pentium controllers are also available on request

50H4644
SA14-4701-02
Revised 3/96

Connector Pin Assignment

PD0	1	69	GND
PD1	2	70	PD2
DQ0	3	71	VCC
DQ1	4	72	DQ2
VCC	5	73	DQ3
DQ4	6	74	DQ5
DQ6	7	75	DQ7
DQP0	8	76	GND
DQ8	9	77	DQ9
DQ10	10	78	DQ11
GND	11	79	DQ12
CLK0	12	80	GND
GND	13	81	DQ13
DQ14	14	82	DQ15
VCC	15	83	DQP1
DQ16	16	84	GND
DQ17	17	85	DQ18
DQ19	18	86	DQ20
DQ21	19	87	DQ22
VCC	20	88	DQ23
DQP2	21	89	GND
DQ24	22	90	DQ25
DQ26	23	91	DQ27
DQ28	24	92	DQ29
GND	25	93	DQ30
DQ31	26	94	GND
DQP3	27	95	$\overline{CE0}$
GND	28	96	$\overline{WE1}$
$\overline{WE0}$	29	97	$\overline{WE3}$
$\overline{WE2}$	30	98	$\overline{OE0}$
$\overline{ADSP}$	31	99	$\overline{ADSC}$
$\overline{ADV}$	32	100	GND
VCC	33	101	$\overline{OE1}$
$\overline{WE4}$	34	102	$\overline{WE5}$
$\overline{WE6}$	35	103	$\overline{WE7}$
DQ32	36	104	$\overline{CE1}$
DQ33	37	105	DQ34
GND	38	106	DQ35
DQ36	39	107	DQ37
DQ38	40	108	VCC
DQ39	41	109	DQP4
DQ40	42	110	DQ41
VCC	43	111	DQ42
DQ43	44	112	DQ44
DQ45	45	113	GND
DQ46	46	114	DQ47
DQP5	47	115	DQ48
GND	48	116	DQ49
CLK1	49	117	GND
GND	50	118	DQ50
DQ52	51	119	DQ51
DQ53	52	120	DQ54
DQ55	53	121	DQ56
DQP6	54	122	GND
VCC	55	123	DQ57
DQ58	56	124	DQ59
DQ60	57	125	DQ61
DQ62	58	126	DQ63
DQP7	59	127	VCC
A0	60	128	A1
A2	61	129	A3
A4	62	130	A5
A6	63	131	A7
A8	64	132	NC
A10	65	133	A9
A12	66	134	A11
A14	67	135	A13
GND	68	136	A15

Pins 8,12,21,27,31,32,47,49,54,59,83,99 and 109 are NC for P/N14M32724BAA

Vcc = 3.3V for P/d 14M64724DPA

Vcc = 5.0V for P/Ns 14M64724DAA and 14M32724BAA

50H4644
SA14-4701-02
Revised 3/96

Pin Definition and Description

Signal	I/O	Number of pins	Description
A0-A15	I	16	Address inputs. These inputs are registered at the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
DQ0-DQ63	I/O	64	Data I/O. The 64 bit data bus is divided into 8 bytes: D(0:7), D(8:15), D(16:23), D(24:31), D(32:39), D(40:47), D(48:55), D(56:63). D(0:7) is the least significant byte and D(56:63) is the most significant byte. The direction of the data pins is controlled by $\overline{OE}$.
DQP0-DQP7	I/O	8	Data Parity I/O. These are the data parity bits for the data bus. DQP0 applies to D(0:7) and DQP7 applies to D(56:63). Applies to P/Ns 14M64724DPA and 14M64724DAA.. P/N 14M32646BAA does not have parity bits and are NC at interface.
$\overline{CE0}$-$\overline{CE1}$	I	2	Chip enable. These lines are used to enable or disable the module. They can also be used to block $\overline{ADSP}$. LOW Active.
$\overline{WE0}$-$\overline{WE7}$	I	8	Byte write enables. These lines allow individual bytes to be written to the module. $\overline{WE0}$ controls DQ0-DQ7 and DQP0, $\overline{WE1}$ controls DQ8-DQ15 and DQP1, etc. LOW Active.
$\overline{OE0}$-$\overline{OE1}$	I	2	Output enable. These are asynchronous inputs which enable the data I/O drivers when active. LOW Active.
$\overline{ADSP}$	I	1	Address Status Processor. When this input and/or $\overline{ADSC}$ is active, a new external address will be latched thus interrupting any ongoing burst. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at the same time (at the rising edge of CLK), only $\overline{ADSP}$ will be recognized. $\overline{ADSP}$ is ignored when $\overline{CE}$ is HIGH. LOW Active.
$\overline{ADSC}$	I	1	Address Status Controller. When this input and/or $\overline{ADSP}$ is active, a new external address will be latched thus interrupting any ongoing burst. A read or write is performed using the new address if all chip enables are active. LOW Active.
$\overline{ADV}$	I	1	Address Advance. The input is used to automatically increment the internal burst address counter. Depending on the module type, the burst sequence can be either linear (Power-PC based) or interleaved (Pentium/486) based. LOW Active.
CLK(0:1)	I	2	Clock. This signal is used to latch the address, data (store), $\overline{ADSP}$, $\overline{ADSC}$, $\overline{CE}$, $\overline{WE}$, and $\overline{ADV}$. All synchronous inputs must meet setup and hold times around the clock's rising edge.
PD0-PD2	O	3	Presence Detect Bits
NC	-		No Connect (Pin count varies with the design; See Connector Pin Assignment Page 4)
GND	I	18	Ground.
VCC	I	9	Power Supply. +3.3V (For P/N 14M64724DPA) or +5V (For P/N 14M64724DAA & 14M32724BAA)

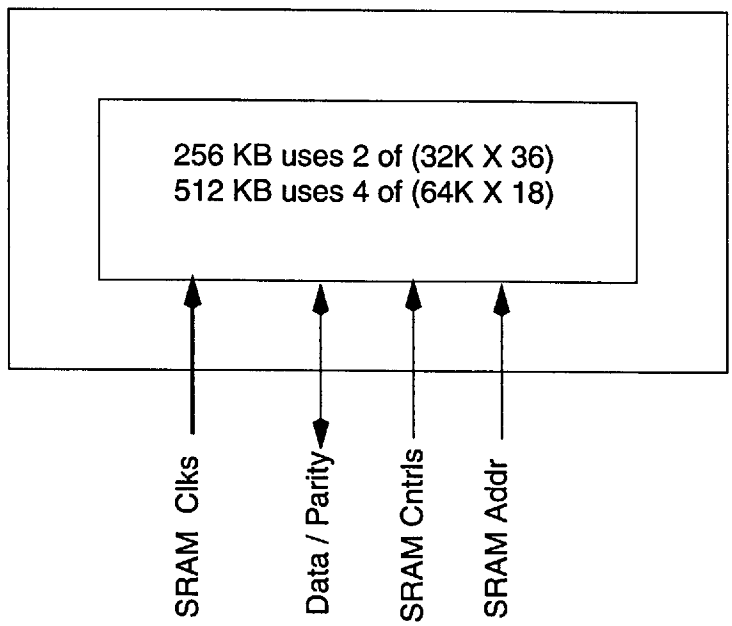
Ordering Information

Part Number	Organization	Power Supply	Access/Cycle	Leads	Type
IBM14M32724FPA-9	32K x 72	+3.3V	9 ns / 15 ns	136	PowerPC
IBM14M32724FPA-11	32K x 72	+3.3V	11 ns / 15 ns	136	PowerPC
IBM14M64724DPA-9	64K x 72	+3.3V	9 ns / 15 ns	136	PowerPC
IBM14M64724DPA-11	64K x 72	+3.3V	11 ns / 15 ns	136	PowerPC
IBM14M64724DAA-9	64K x 72	+5V	9 ns / 15 ns	136	PowerPC
IBM14M32646BAA-12	32K x 64	+5V	12 ns / 15 ns	136	PowerPC Asynch

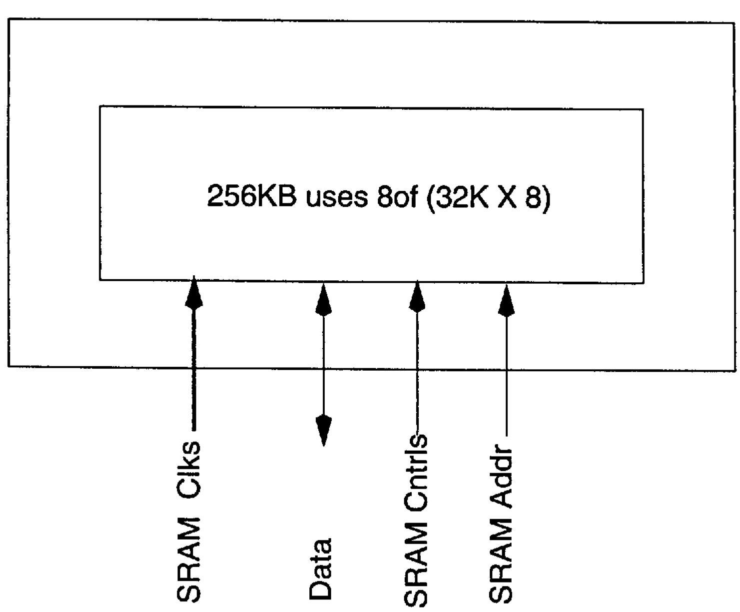
50H4644
SA14-4701-02
Revised 3/96

Block Diagram

Synchronous module (256 and 512KB)



Asynchronous module (256 KB)



Burst Sequence Truth Table (linear burst) (for 14M32724FPA, 14M64724DPA & 14M64724DAA)

External Address	A15-A2	(A1,A0)			
		(0,0)	(0,1)	(1,0)	(1,1)
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)
2nd Access	A15-A2	(0,1)	(1,0)	(1,1)	(0,0)
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)
4th Access	A15-A2	(1,1)	(0,0)	(0,1)	(1,0)

Presence Detect Table

Part Number	Module Burst Type	Module Size	Vcc	PD0	PD1	PD2
IBM14M32724FPA	Linear	256KB	+3.3V	TBD	TBD	TBD
IBM14M64724DPA	Linear	512KB	+3.3V	NC	NC	GND
IBM14M64724DAA	Linear	512KB	+5V	GND	GND	NC
IBM14M32646BAA	Asynch	256KB	+5V	NC	GND	NC

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage (3.3V)	V_{CC3}	-0.5 to 4.6	V	1, 2
Power Supply Voltage (5V)	V_{CC5}	-0.5 to 7	V	1, 3
Input Voltage	V_{IN}	-0.5 to 6.0	V	1
Output Voltage	V_{OUT}	-0.5 to V_{CC3}+0.5	V	1
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P/Ns 14M64724DPA and 14M32724FPA useV_{CC3}.
3. P/Ns 14M64724DAA and 14M64646 BAA use V_{CC5} .

Recommended DC Operating Conditions (T_A=0 to 70°C)

P/N 14M32724FPA, 14M64724DPA & 14M64724DAA						
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{CC3}	3.135	3.3	3.465	V	1, 4, 5
Supply Voltage	V_{CC5}	4.75	5.0	5.25	V	1, 4, 5
Input High Voltage	V_{IH}	2.2	—	5.5	V	1, 2, 4
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3, 4
Output Current	I_{OUT}	—	5	8	mA	4

1. All voltages referenced to V_{SS}. All V_{DD} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)
4. Input Voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 nanosecond set-up and hold times.
5. P/N 14M32724FPA & 14M64724DPA use Vcc3 only; P/N 14M64724DAA uses Vcc5 only

Capacitance (T_A=0 to +70°C, V_{CC}=3.3V ± 5%, f=1MHz) Maximum values

P/N 14M32724FPA, 14M64724DPA & 14M64724DAA					
Parameter	Symbol	Test Condition	256KB	512KB	Units
Input Capacitance (Address)	C_{IN1}	V_{IN} = 0V	25	25	pF
Input Capacitance (Control, $\overline{CE}$, $\overline{OE}$)	C_{IN2}	V_{IN} = 0V	15	15	pF
Input Capacitance ($\overline{WE}$, CLK)	C_{IN3}	V_{IN} = 0V	10	10	pF
Data I/O Capacitance (DQ0-DQ71)	C_{OUT}	V_{OUT} = 0V	7	7	pF

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC}=3.3V ± 5%)

P/N 14M32724FPA, 14M64724DPA & 14M64724DAA					
Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	Icc15		900 950	mA	1, 2
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH}, CS2 = V_{IL}All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0, CLK at 100MHz)	I_{SB}		100	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}		4	µA	
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}		4	µA	
Output High Level Output "H" Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output "L" Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current
2. P/N 14M64724DAA operating current is 950mA.

Recommended DC Operating Conditions (T_A=0 to 70°C)

IBM14N32646BAA						
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage (5.0V)	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.2	—	Vcc+0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.5	—	0.8	V	1, 3
Output Current	I_{OUT}	—	-5	5	mA	

1. All voltages referenced to GND. All V_{CC} and GND pins must be connected.
2. V_{IH}(Max)= Vcc + 0.5
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -2.0V (pulse width ≤ 20.0 ns.)

Capacitance (T_A=0 to +70°C, V_{CC5}=5V ± 5%, f=1MHz) Maximum values

IBM14N32646BAA					
Parameter		Symbol	Test Condition	256KB	Units
Input Capacitance (Address)	A3, A4	C_{IN1}	V_{IN} = 0V	35	pF
	All others			10	
Input Capacitance ($\overline{CE}$, $\overline{OE}$)		C_{IN2}	V_{IN} = 0V	64	pF
Input Capacitance ($\overline{WE}$)		C_{IN3}	V_{IN} = 0V	10	pF
Data I/O Capacitance (DQ0-DQ71)		C_{OUT}	V_{OUT} = 0V	10	pF

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC5}=5V ± 5%)

IBM14N32646BAA					
Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current @ 5.0V Maximum Power Supply Operating Current (Maximum V_{CC5}, I_{out} = 0)	I_{CC12}		1430	mA	1
Standby Current @ 5.0V Power Supply Standby Current (Maximum V_{CC5}, $V_{IH} \le \overline{CS}$; All other inputs = V_{IH} or V_{IL}; I_{out}= 0)	I_{SB}		340	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{CC})	I_{LI}		40	µA	
Output Leakage Current (V_{OUT} =0 &V_{CC}, $\overline{OE}$ = V_{IH})	I_{LO}		40	µA	
Output High Level Output "H" Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output "L" Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current

AC Characteristics (T_A=0 to +70°C, Units in nsec)

P/N 14M32724FPA, 14M64724DPA & 14M64724DAA						
Parameter	Symbol	-9		-11		Notes
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYCLE}	15.0	—	15.0	—	
Clock Pulse High	t_{CH}	3.0	—	3.0	—	
Clock Pulse Low	t_{CL}	3.0	—	3.0	—	
Clock to Output Valid	t_{CQ}	—	9.0	—	11.0	3
Address Status Controller Setup Time	t_{ADSCS}	2.5	—	2.5	—	
Address Status Controller Hold Time	t_{ADSCH}	0.5	—	0.5	—	
Advance Setup Time	t_{ADVS}	2.5	—	2.5	—	
Advance Hold Time	t_{ADVH}	0.5	—	0.5	—	
Address Setup Time	t_{AS}	2.5	—	2.5	—	
Address Hold Time	t_{AH}	0.5	—	0.5	—	
Chip Selects Setup Time	t_{CSS}	2.5	—	2.5	—	
Chip Selects Hold Time	t_{CSH}	0.5	—	0.5	—	
Write Enables Setup Time	t_{WES}	2.5	—	2.5	—	
Write Enables Hold Time	t_{WEH}	0.5	—	0.5	—	
Data In Setup Time	t_{DS}	2.5	—	2.5	—	
Data In Hold Time	t_{DH}	0.5	—	0.5	—	
Data Out Hold Time	t_{CQX}	3.0	—	3.0	—	3
Clock High to Output High Z	t_{CHZ}	—	5.0	—	5.5	1, 2, 3
Clock High to Output Active	t_{CLZ}	2.5	—	2.5	—	1, 2, 3
Output Enable to High Z	t_{OHZ}	2.0	5.5	2.0	6.5	1, 3
Output Enable to Low Z	t_{OLZ}	0.25	—	0.25	—	1, 3
Output Enable to Output Valid	t_{OQ}	—	5.0	—	6.0	3

1. Transitions are measured ± 200 mV from steady state voltage.
2. At any given voltage and temperature, T_{CHZ} max is always less than T_{CLZ} min for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from HIZ to new RAM data.
3. See AC test loading figure on Page 12.

AC Test Loading

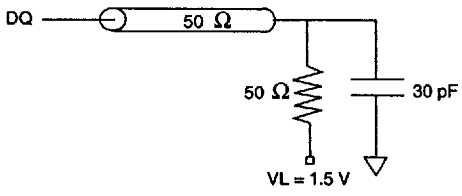


Fig. 1 Test Equivalent Load

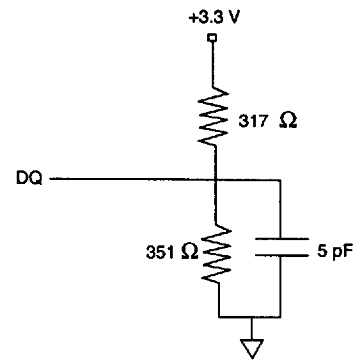
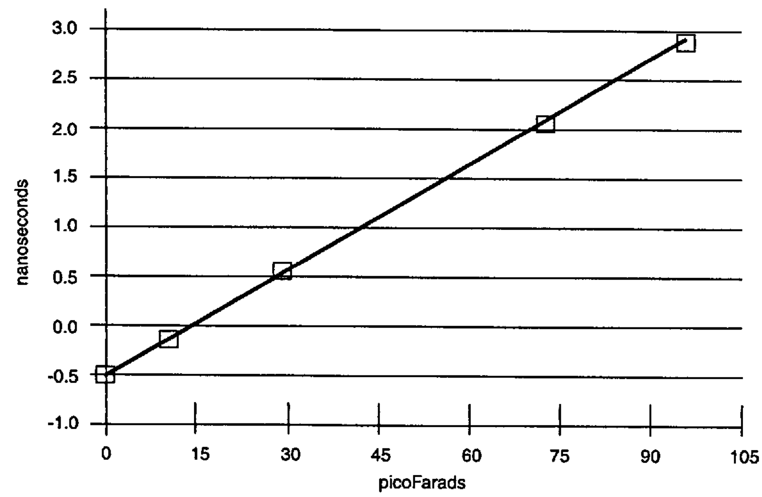


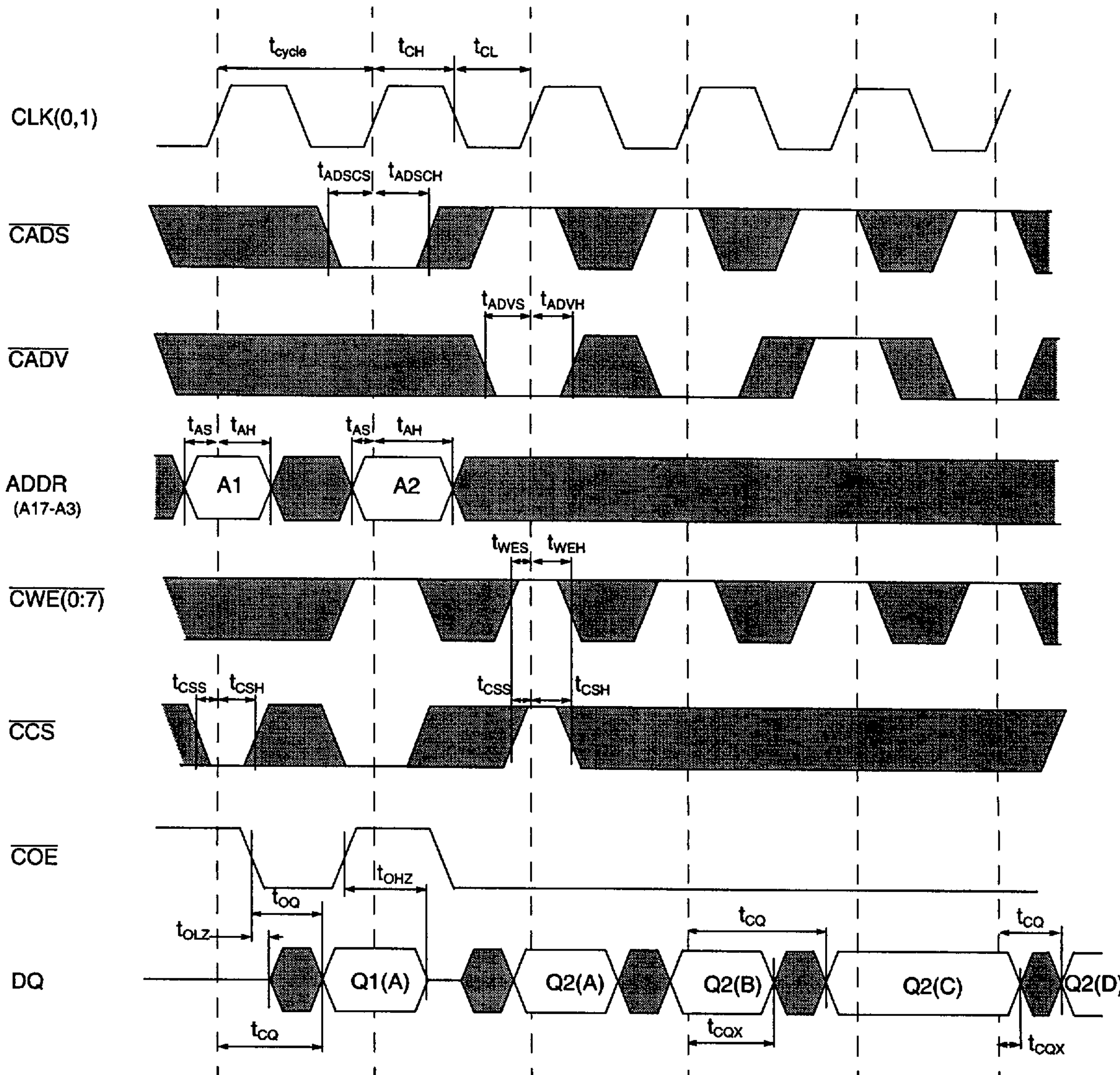
Fig. 2 Test Equivalent Load

Output Capacitive Load Derating Curve



The derating curve above is for a purely capacitive load on the output driver. For example, a part specified at 8ns access time will behave as though it has an 8.5 ns access time if a 30 pF load with no DC component was attached to the output driver. The access time guaranteed in the datasheets are based on a 50 ohm terminated test load. For unterminated loads the derating curve should be used. This curve is based on nominal process conditions with worst case parameters $V_{CC} = 3.14$ V, $T_a = 70$ °C.

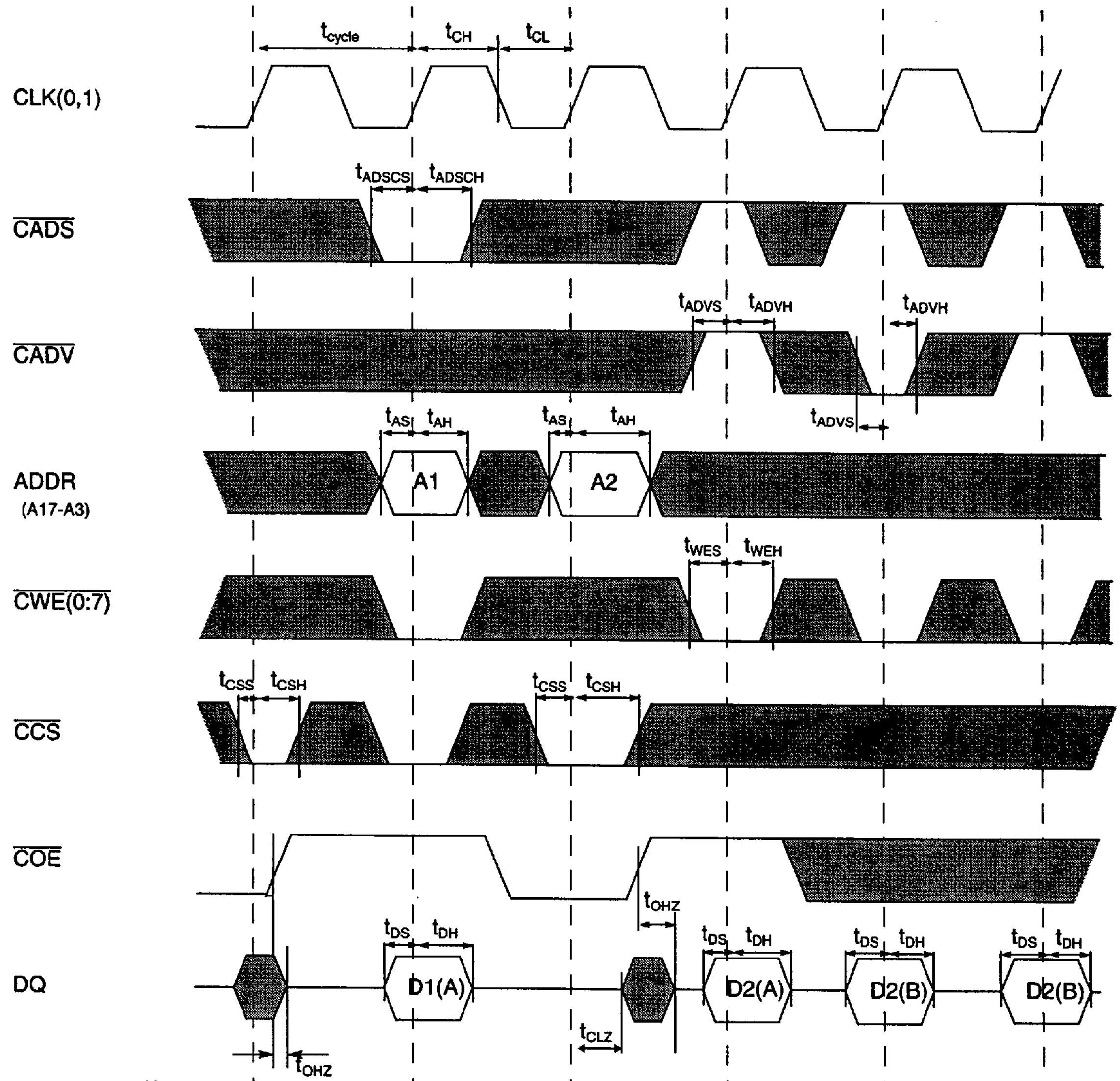
Synchronous SRAM Timing Diagram (Burst Read)



Notes:

1. Q1(A) and Q2(A) refer to output for Address A1 and A2 respectively.
2. Q2(B),Q2(C) and Q2(D) refer to output from subsequent internal burst counter addresses.

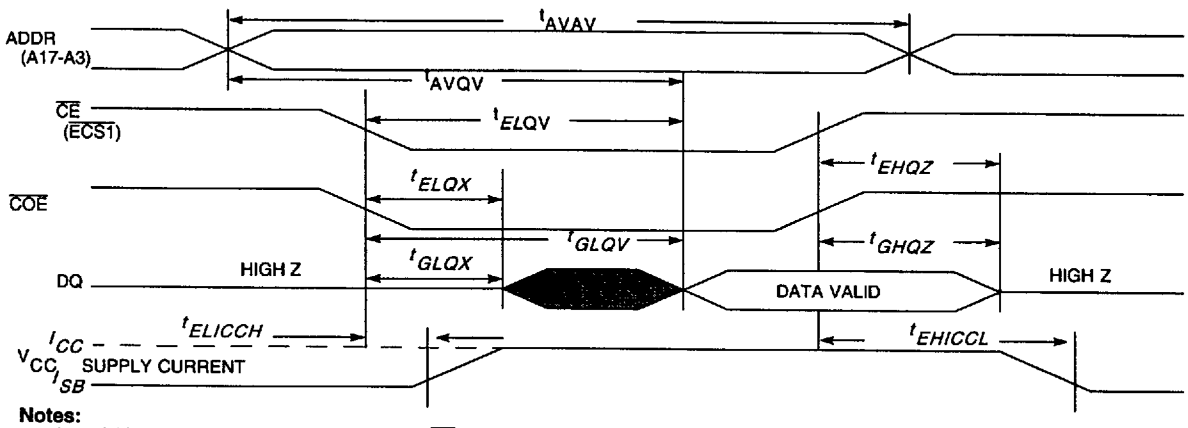
Synchronous SRAM Timing Diagram (Burst Write)



Notes:

1. D1(A) and D2(A) refer to data written to addresses A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.

Asynchronous SRAM Timing Diagram (Read)



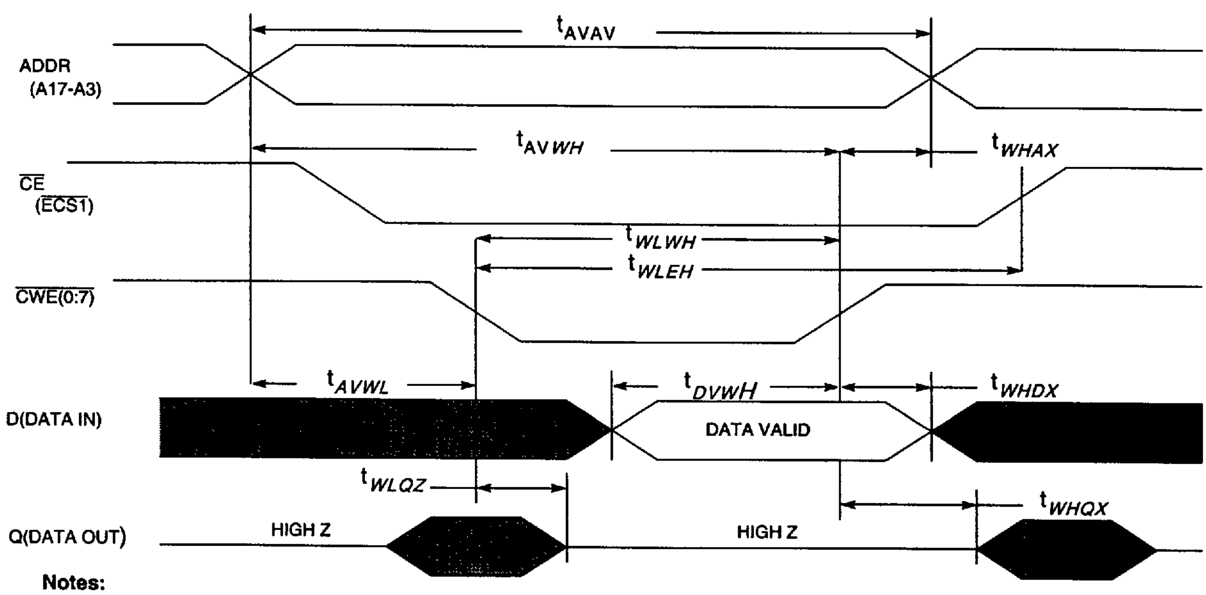
Notes:
1. Addresses valid prior to or coincident with $\overline{CE}$ going low.

Read Cycle

Parameter	Symbol	Data		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{AVAV}	12		ns	2
Address Cycle Time	t_{AVQV}		12	ns	
Enable Access Time	t_{ELQV}		12	ns	3
Output Enable Access Time	t_{GLQV}		6	ns	
Output Hold from Address Change	t_{AXQX}	3		ns	4, 5, 6
Enable Low to Output Active	t_{ELQX}	4		ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	0	7	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0		ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	0	6	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0		ns	
Power Down Time	t_{EHICCL}		12	ns	

1. $\overline{CWE(0:7)}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{CE}$ going low
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mv from steady-state voltage.
6. This parameter is sampled and not 100% tested.

Asynchronous SRAM Timing Diagram (Write Cycle 1)



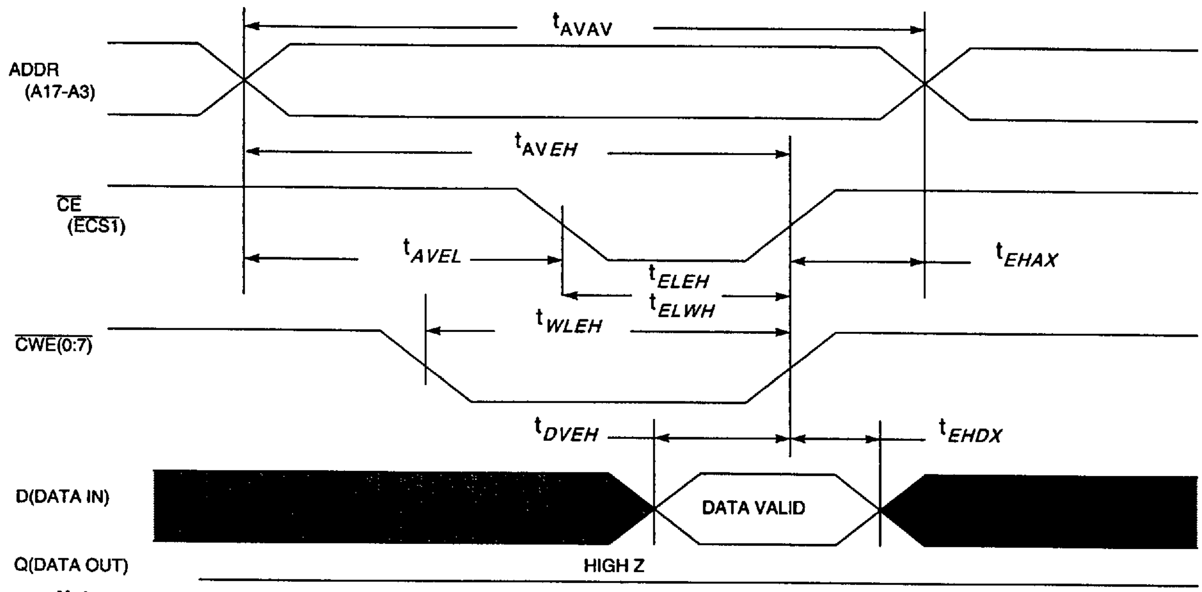
Notes:
1. A write occurs during the overlap of $\overline{COE}$ low and $\overline{CWE}$ low..
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.

Write Cycle 1 ($\overline{WE}$ Controlled)

Parameter	Symbol	Data		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	1
Address Setup Time	t_{AVWL}	0		ns	
Address Valid to End of Write	t_{AVWH}	10		ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	10		ns	
Write Pulse Width $\overline{G}$ High	t_{WLWH} t_{WLEH}	9		ns	2
Data Valid to End of Write	t_{DVWH}	6		ns	
Data Hold Time	t_{WHDX}	0		ns	
Write Low to Output High-Z	t_{WLQZ}	0	6	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	2		ns	3, 4, 5
Write Recovery Time	t_{WHAX}	0		ns	

1. All timings are referenced from the last valid address to the first transitioning address.
2. If $V_{IH} \leq \overline{COE}$, the output will remain in a high impedance state
3. At any given voltage and temperature , t_{WLQZ} (max) < t_{WHQX} (min), both for a given device and from device to device.
4. Transition is measured ±500 mv from steady state voltage.
5. This parameter is sampled and not 100% tested.

Asynchronous SRAM Timing Diagram (Write Cycle 2)



Notes:
1. A write occurs during the overlap of $\overline{COE}$ low and $\overline{CWE}$ low.

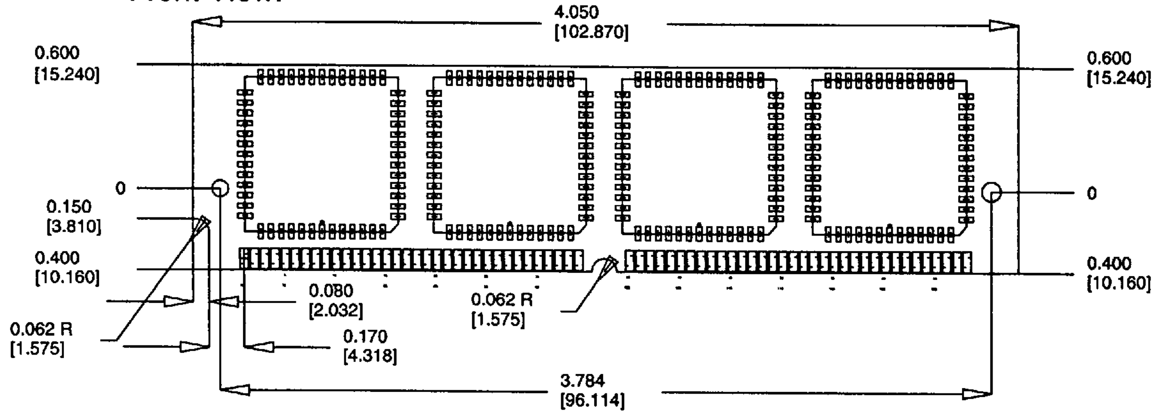
Write Cycle 2 ($\overline{OE}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	
Address Setup Time	t_{AVEL}	0		ns	
Address Valid to End of Write	t_{AVEH}	10		ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	9		ns	3, 4
Data Valid to End of Write	t_{DVEH}	6		ns	
Data Hold Time	t_{EHDX}	0		ns	
Write Recovery Time	t_{EHAX}	0		ns	

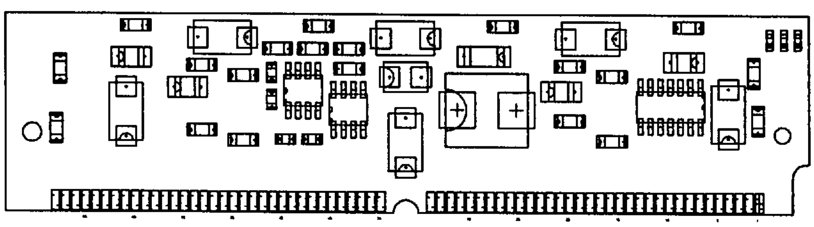
1. A write occurs during the overlap of $\overline{COE}$ low and $\overline{CWE}$ low
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
4. If $\overline{COE}$ goes high coincident with or before $\overline{CWE}$ goes high, the output will remain in a high impedance state.

Layout Drawing of 512KB (64K x 72), 5V, 136-pin Synchronous module

Front View:

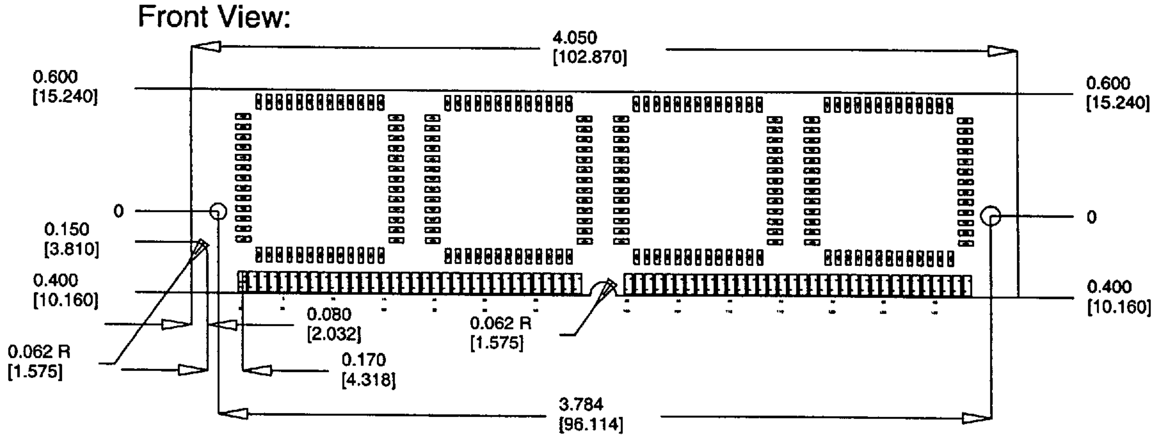


Back View:

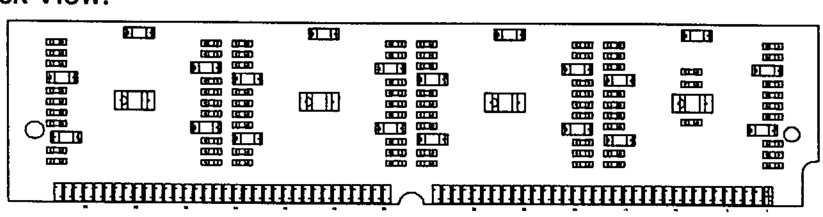


Layout Drawing of 512KB (64K x 72), 3.3V, 136 -pin Synchronous module

Front View:

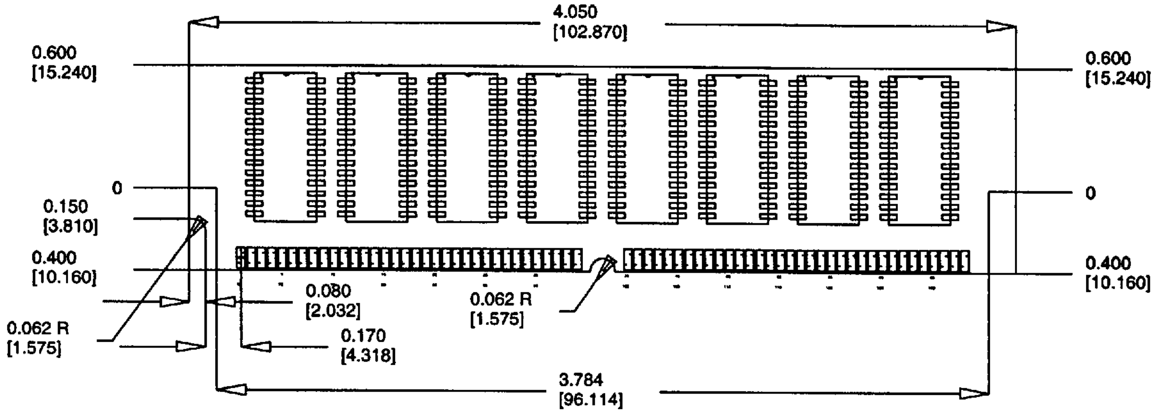


Back View:

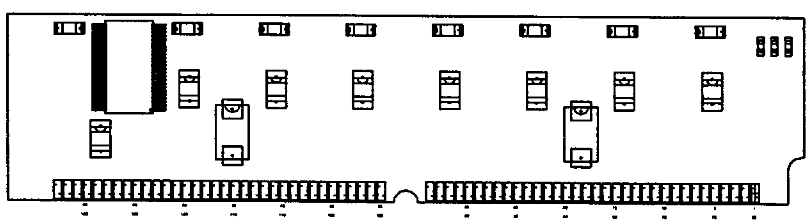


Layout Drawing of 256KB (32K x64), 5V, 136pin Asynchronous module

Front View:



Back View:



Revision Log

Rev	Contents of Modification
10/95	Preliminary Release
12/95	Latest Realease; EC # E21031; Dt 12/05/95
3/96	Added 256KB SSRAM DIMM P/N, 03/07/96

50H4644
SA14-4701-02
Revised 3/96