RS825x

ATM Physical Interface (PHY) Devices

The RS825x is a family of four 155 Mbps (OC-3/STM-1) ATM-SONET Physical Layer (PHY) devices with an integrated, PLL clock and data recovery circuit. These devices have optimized SONET framer functions for mapping ATM cells to SONET payloads for edge switch applications, and optional enhanced feature sets for ATM-WAN access applications. They provide ATM Forum-compliant service termination, and map the 53-byte cells from an ATM switch fabric or an adaptation layer processor (SAR) into the SONET payload. Available in single, dual, and quad port packages, LAN and WAN versions, the RS825x devices are tailored to meet a wide variety of ATM OC-3 applications. These include WAN terminals, ATM LAN and WAN switches, ATM OC-3 NICs, and Ethernet-ATM uplink cards.

The RS825x family thus consists of four devices, with two devices in each of two categories, WAN and LAN. All references to the RS825x in this document apply to the entire family of RS825x devices, unless otherwise noted.

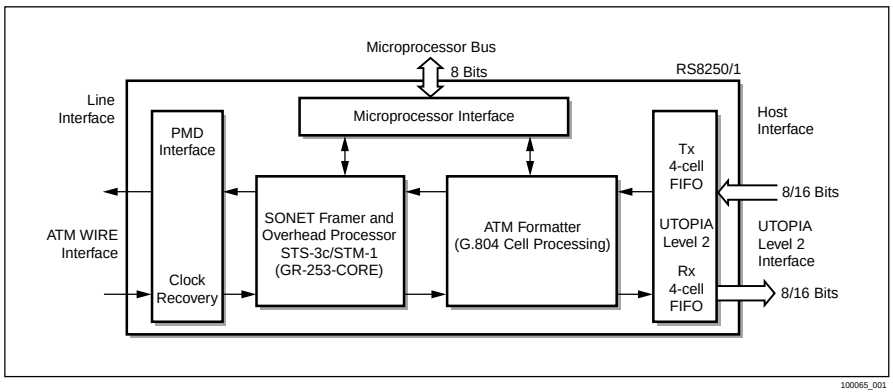
The RS825x uses an ATM Forum UTOPIA Level 2-compliant host interface designed for a multi-PHY environment. The ATM framer provides G.804 cell processing, with HEC generation, checking and alignment operations. Each port provides a 155 Mbps SONET termination with all of the counters needed for capturing both SONET and ATM error events as specified by the ATM Forum. A proprietary protection scheme allows for near-instantaneous switching between active and stand-by PHYs.

The RS825x family uses a Pseudo-Emitter Coupled Logic (PECL) line interface, that is compliant with the ATM Forum's WIRE definition. Thus, designers can connect directly to either fiber optic or Cat 5 Physical Media Dependant (PMD) devices. For diagnostics, three loopback modes are provided: source loopback, line loopback before the ATM processor, and line loopback at the UTOPIA block. In addition, the RS825x can generate BIP-8 errors and insert invalid HECs.

The WAN versions of the device (RS8250/4), support the following:

- Compliance with the jitter requirements of Bellcore's GR-253-CORE when using the 19.44 MHz reference clock.
- Automatic Protection Switching (APS) using the K1/K2 overhead octets and a Bit Error Rate (BER) integrator.
- Access to the S1 octet for system timing.
- Data transmission/reception over the Data Link message channels, D1-D3 and D4-D12.

Functional Block Diagram



Distinguishing Features

- Synthesizes a 155.52 MHz clock from an 8 kHz input
- UTOPIA Level 2 interface
- Meets ITU, ANSI, and ATM Forum standards
- ATM Forum WIRE interface for PMDs using PECL
- D1-D3, D4-D12 external data link (WAN only)
- Supports APS (K1/K2 bytes) (WAN only)
- SRAM-style microprocessor interface for all control and configuration registers
- Glueless interface to the Bt/RS823x segmentation and reassembly devices
- JTAG (IEEE 1149.1a-1993) compliant
- 8 kHz and 19.44 MHz selectable sync inputs and outputs
- SONET overhead processing
- Automatic collection of one-second statistics
- Low power consumption-500 mW/port
- Rapid start after reset
- Reference software provided
- 3.3 V, (–40 °C to 85 °C)
- Packages: 128-pin TQFP (RS8251), 156-pin BGA (RS8250), and 256-pin BGA (RS8254/5)

Applications

- Switches, Hubs, Routers
- LAN NIC cards
- DSLAM uplinks

Line Interface

- ATM Forum WIRE interface specification compliant
- PECL I/O, compatible with PMD optical and UTP interface devices
- Clock recovery from NRZ input data
- Recovery of receive-octet alignment and octet clock from F6/28 framing pattern
- Select transmit clock from input or recovered receive clock

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
RS8250EBGC	28250-16	C	156-pin, 15 mm BGA	-40 °C to 85 °C
RS8251ETFC	28251-16	C	128-pin TQFP	-40 °C to 85 °C
RS8254EBGC	R7173-17	C	256-pin, 35 mm BGA	-40 °C to 85 °C
RS8255EBGC	R7174-17	C	256-pin, 35 mm BGA	-40 °C to 85 °C

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Line Interface (continued)

- PMD (line) and Framer (source) loopbacks for diagnostic testing
- Loss of Signal (LOS) detection
- 8 kHz or 19.44 MHz reference clock

UTOPIA Level 2 Interface

- PHY cell to UTOPIA interface
- 50 MHz maximum data rate
- 8/16-bit data path interface
- Multi-PHY support
- Mode-compatible with UTOPIA level 1
- Configurable cell buffer depth

SONET STS_3c/STM-1 Framer

Section Overhead Octets Supported

	Transmit	Receive
A1/A2	F6/28 hex or disable 00	Monitor out of frame state machine
J0	01 hex or 64-byte trace buffer	Monitor Rx trace buffer, interrupt on change
Z0, Z0	02, 03 hex	Not checked
B1	Calculated, error insertion	Checked, errors counted
D1, D2, D3	00 hex or external data link (WAN only)	External data link (WAN only)

Line Overhead Octets Supported

	Transmit	Receive
H1/H2	620A/93FF hex pointer	Full GR.253 pointer processor
H3	Set to 00	Used in pointer processor
B2	Calculated, error insertion	Checked, errors counted
K1/K2	Insertable via register (WAN only)	Checked, interrupt on change (WAN only)
D4-D12	00 hex or external data link (WAN only)	External data link (WAN only)
S1	Insertable via register (WAN only)	Checked, interrupt on change (WAN only)
M1	Line FEBE inserted	Checked, errors counted

Path Overhead Octets Supported

	Transmit	Receive
J1	00 hex or 64-byte trace buffer	Monitor Rx trace buffer, interrupt on change
B3	Calculated, error insertion	Checked, errors counted
C2	13 hex for ATM mapping	Checked for 01 or 13 hex
G1	Path FEBE, RDI inserted	Checked, errors counted, status

SONET Framer Functions

- Recovers frame location using F6/28 framing pattern
- Processes pointer to locate payload envelope
- Provides OOF, LOP, and AIS status
- Provides frame and payload position information to other blocks
- Generates clocks and frame counters
- Maps cell data into payload envelope
- Generates all section, line, and path overhead and alarms
- Performs cell and frame scrambling before transmission
- Detects and integrates alarms for reporting in status registers
- Detects BIP and FEBE errors for error counters
- Recovers D1-D3 and D4-D12 data link (WAN only)

Cell Alignment Framing Section

- Recovers cell alignment from HEC
- Performs HEC error correction
- Matches idle/desired cell headers and generates write
- Strobes and cell sync for UTOPIA interface
- Generates cell status bits, cell counts, and error counts
- Reads cell data from the UTOPIA FIFO
- Inserts headers and generates HEC
- Inserts idle cells when no traffic is ready

Support for Automatic Protection Switching (APS) (WAN Only)

- Register control allows for support of APS
- K1/K2 Transmit control register allows transmission of any value
- Separate control bits for AIS, line FERF
- K1/K2 receive status register allows observation of incoming octet values
- Maskable interrupt on any change in received value
- Software interrupt routine can easily implement APS protocol
- Signal Fail/Signal Detect BER threshold monitoring

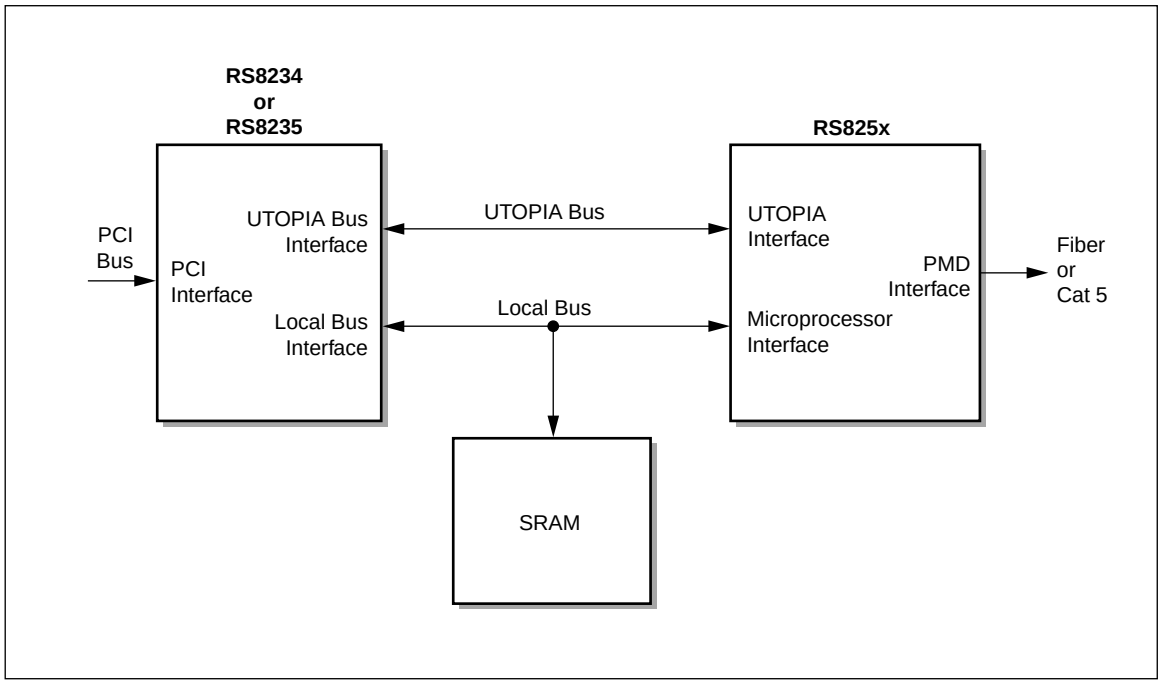
Microprocessor Interface

- SRAM-like interface mode with high-performance or low-power access selection
- Glueless RS823x SAR interface mode
- 8-bit data bus
- Open-drain interrupt output

Counters/Status and Interrupt Registers

- Summary interrupt indications
- Configuration of interrupt enables
- One-second status latching
- One-second counter latching
- Eight general purpose outputs, configurable as status indicator pins

The following diagram is a Network Interface Card (NIC) application of the RS825x



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1.0 Product Description

The RS825x ATM Physical Layer Interface (PHY) device is a transmitter/receiver that performs the Transmission Convergence (TC) sublayer function of converting SONET/SDH frames to ATM cells and vice versa.

The RS825x family consists of four devices in two categories, WAN and LAN:

Table 1-1. RS825x Device Categories

Number of Ports	WAN Device No.	LAN Device No.
1	RS8250	RS8251
4	RS8254	RS8255

The difference between the WAN and LAN versions of the RS825x is that the RS8250/4 WAN version includes an enhanced performance feature set as follows:

1. The integral PLL/clock and data recovery circuit meets the jitter tolerance, jitter transfer, and jitter generation specification of Bellcore *GR.253-CORE*
2. Automatic Protection Switching (APS) is supported through access of the K1 and K2 overhead octets
3. Programmable signal degrade/signal fail BER threshold monitoring with automatic detection and clearing
4. Extended SONET overhead processing with access to data link D1-D3 and D4-D12 octets for messaging to an optional serial communication controller
5. Access to the S1 overhead status byte for transporting synchronization status messages

In this document, RS825x refers to the entire family of RS825x devices. Specific device numbers are used when features do not apply to all of the devices in the family. Appendix A provides information about the RS8254/5 quad PHY devices. Appendix B provides information about the RS8250 single WAN device.

This chapter provides an overview of the RS825x, including its primary features and applications. A logic diagram, package pinouts, and pin descriptions are also presented. A block diagram is included to show the data flow in the device.

1.1 RS825x Features

The RS825x, operating at up to 155 Mbps (duplex), provides a single-access ATM service termination for User-to-Network Interfacing (UNI) and Network-to-Network Interfacing (NNI) in conformance with the *ATM Forum UNI Specification 94/0317, ITU Recommendation I.432,* and other industry standards. This PHY device consists of several functional blocks: the SONET Framer, the ATM Cell Formatter, the UTOPIA Level 2 interface, and the microprocessor interface. Together these blocks and the clock recovery block provide efficient conversion of SONET frames to ATM cells and vice versa.

The RS825x is implemented in 0.35 micron CMOS technology, which runs on 3.3 V. The RS8250 is packaged in a 156-pin Ball Grid Array (BGA), the RS8251 is packaged in a 128-pin Thin Quad Flat Pack (TQFP), and the RS8254/5 devices in a 256-pin BGA. This low-power device processes STS-3c/STM-1 data streams at 155 Mbps (duplex). The device also provides a Pseudo-Emitter Coupled Logic (PECL) interface for serial connection to a Physical Media Dependent (PMD) device. It has a synchronous 16-bit wide, four-cell deep FIFO buffer. An 8-bit microprocessor bus interface is used for configuration, status, and control of the device. Furthermore, the RS825x output control signals can be set up to drive Light Emitting Diodes (LEDs) for monitoring data and alarm activity.

The RS825x descrambles received data, then uses the payload pointer (H1, H2) to locate and retrieve the SONET payload envelope. It also processes section, line, and path overhead. ATM cells are extracted from the payload envelope according to the ATM cell delineation standards. The RS825x optionally performs payload descrambling, Header Error Checking (HEC) error detection and correction, and idle cell filtering. Error counts are kept at all levels for performance monitoring.

The RS825x generates a transmit payload pointer (H1, H2) and framing bytes (A1, A2). The device also performs HEC generation, idle cell insertion, and ATM cell payload scrambling. The RS825x synthesizes the 155.52 MHz transmit clock from a 19.44 MHz, 8 kHz frequency reference, or can use the clock from the internal clock recovery circuit.

When necessary, the RS825x inserts line and path alarm signals and Remote Defect Indications (RDIs). It also inserts path and line BIP-8 codes and Far End Block Error (FEBE) indications to allow performance monitoring at the far end. Additionally, all-0s data can be inserted for diagnostic purposes.

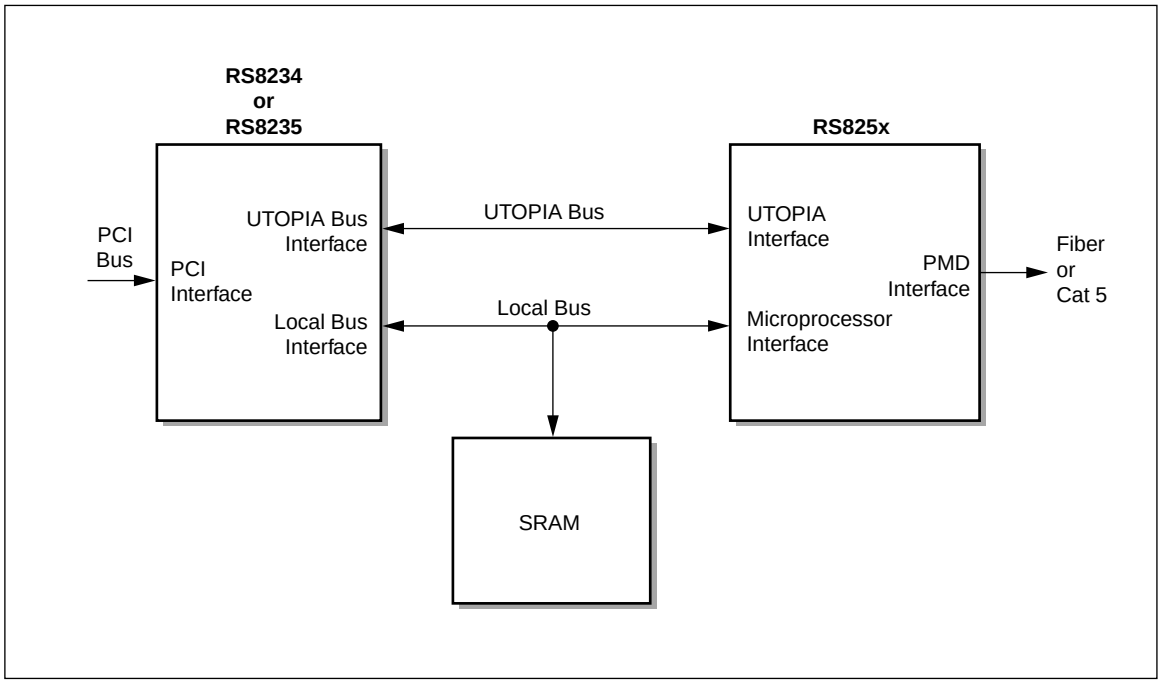
1.2 Applications Overview

The RS825x can be used in a number of applications:

- ATM LANs over optical fibers
- Workstations and PC Network Interface Cards (NICs)
- LAN switches and hubs
- SONET or SDH compliant ATM UNIs

The device is typically used in combination with a Segmentation and Reassembly (SAR) device, such as the RS8234 or RS8235 SAR, to provide framing along with segmentation and reassembly of ATM traffic. The device can be used in switch-to-switch links and switch-to-terminal links. The RS825x connects to the SAR via the UTOPIA and microprocessor interfaces (see Figure 1-1). It can be either loop-timed or source-timed. The device can be configured and controlled through a generic microprocessor interface. For more information on applications for the RS825x, see Chapter 3.0.

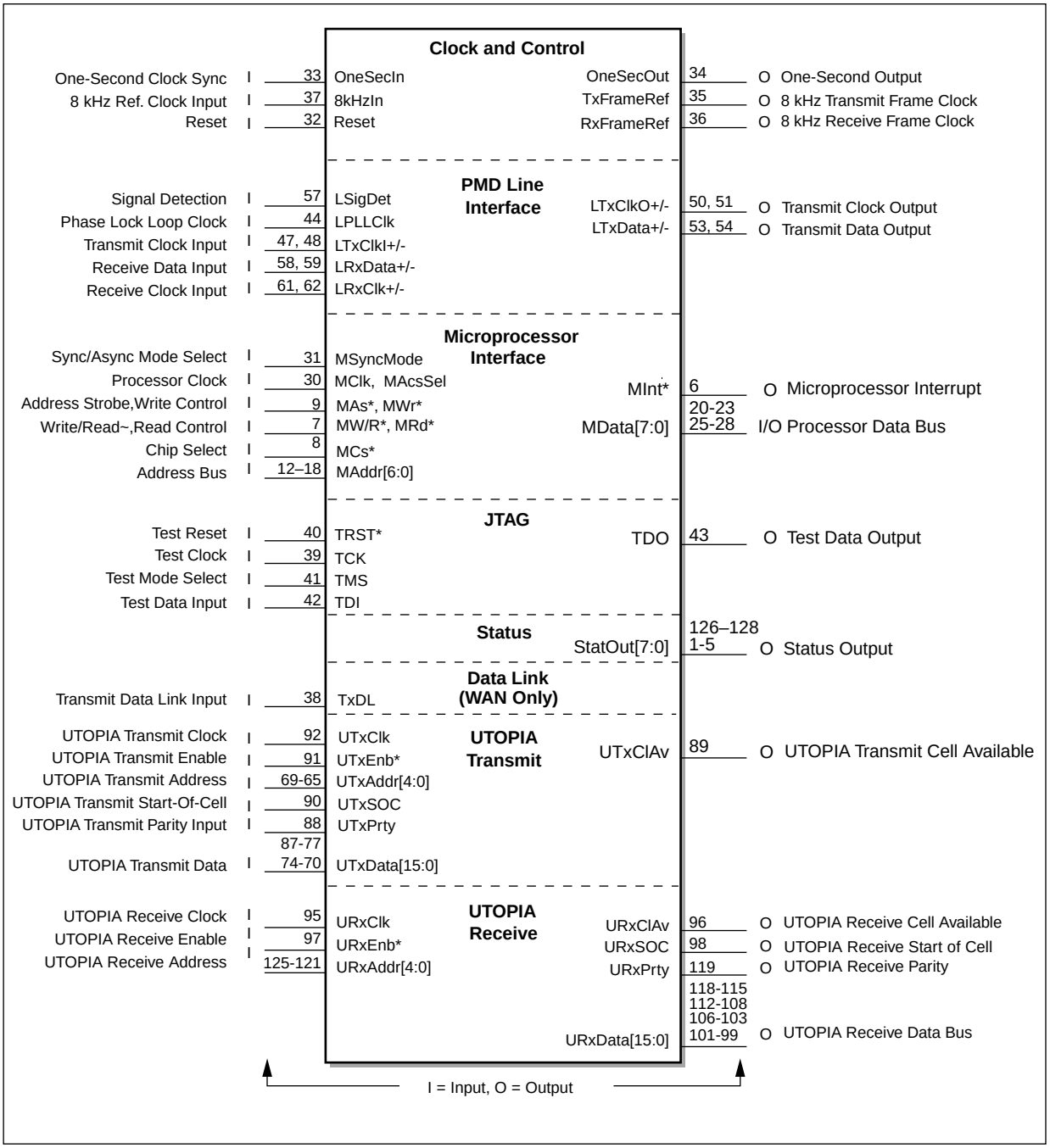
Figure 1-1. RS825x connected to a SAR (RS8234/5)



1.3 Logic Diagram

Figure 1-2 is a logic diagram of the RS825x functional blocks. There are seven general purpose clock and control pins. The PMD interface is comprised of 12 pins. The microprocessor interface consists of six clock and control inputs, an 8-bit data bus, and a 7-bit address bus. There are five JTAG pins and eight status pins. The UTOPIA interface consists of 26 transmit pins and 26 receive pins. There are 10 power pins and 13 ground pins. Pin descriptions are given in Table 1-2.

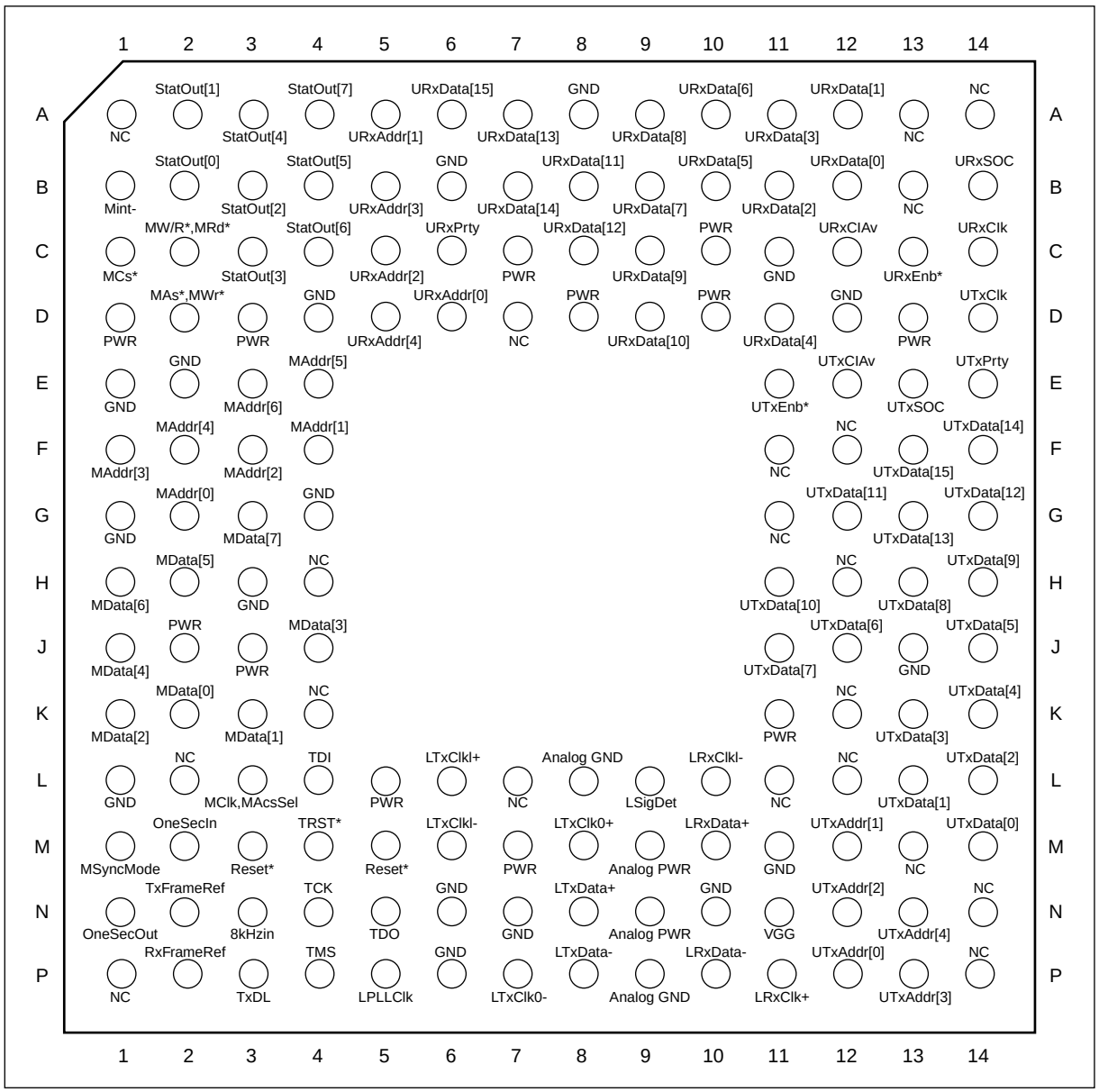
Figure 1-2. RS825x Logic Diagram



1.4 RS8250 Pinout and Pin Descriptions

Figure 1-3 is a pinout diagram for Revision D of the RS8250 ATM Transmitter/Receiver. It is a CMOS integrated circuit packaged in a 156-pin BGA. All unused input pins should be connected to ground. Unused outputs should be left unconnected.

Figure 1-3. RS8250 Pinout Diagram (top view)



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Pin names and numbers are listed in Table 1-2. An asterisk (*) following a pin label indicates that the pin logic level is active low.

Table 1-2. RS8250 Pin Definitions *(1 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Clock and Control	Reset*	Device Reset	M3	TTL	I	This pin is used to reset the device when asserted low.
	OneSecIn	One-Second Strobe	M2	TTL	I	This input is used to latch device status, typically at 1-second intervals.
	OneSecOut	One-Second Output	N1	TTL	O	This pin is a 1-second count derived from the 8khzIn input (pin 37).
	TxFrameRef	Transmit Frame Clock	N2	TTL	O	This pin can be either an 8 kHz output derived from the Transmit SDH frame or a 19.44 MHz output derived from the transmit clock, as selected by bit 1 of the TXSEC (0xOC) register.
	RxFrameRef	Receive Frame Clock	P2	TTL	O	This pin can be either an 8 kHz output derived from the Receive SDH frame or a 19.44 MHz output derived from the recovered (receive) clock as selected by bit 1 of the RXSEC (0x45) register.
	8kHzIn	8 kHz Reference Clock Input	N3	TTL	I	This pin is an 8 kHz clock input used to derive OneSecOut. It can also be used as a transmit clock reference.
PMD Line Interface	LTxClk–	Line Transmit Clock Input Negative Polarity	M6	PECL	I	This pin transmits the timing source directly to the LTxClkO pin if an external source is selected by bits 3 and 4 in the CLKREC register (0x01). This pin is intended to operate at 155.52 MHz. The source must be accurate to 20 PPM.
	LTxClkI+	Line Transmit Clock Input Positive Polarity	L6	PECL	I	This pin transmits the timing source directly to the LTxClkO pin if an external source is selected by bits 3 and 4 in the CLKREC register (0x01). This pin is intended to operate at 155.52 MHz. The source must be accurate to 20 PPM.
	LTxClkO–	Line Transmit Clock Output Negative Polarity	P7	PECL	O	This pin is a 155.52 MHz output derived from one of four clock sources: LPLLClk, 8kHzIn, Loop-timed, or LTxClkI+/-. The clock source is selected in bits 3 and 4 of the CLKREC register (0x01). It is generally used for diagnostic purposes.
	LTxClkO+	Line Transmit Clock Output Positive Polarity	M8	PECL	O	This pin is a 155.52 MHz output derived from one of four clock sources: LPLLClk, 8kHzIn, Loop-timed, or LTxClkI+/-. The clock source is selected in bits 3 and 4 of the CLKREC register (0x01). It is generally used for diagnostic purposes.
	LTxData–	Line Transmit Output Negative Polarity	P8	PECL	O	Transfers SDH-framed data from the RS8251 to the PMD in differential serial NRZ format.
	LTxData+	Line Transmit Output Positive Polarity	N8	PECL	O	Transfers SDH-framed data from the RS8251 to the PMD in differential serial NRZ format.
	LRxClk–	Line Receive Clock Negative	L10	PECL	I	This pin is the receive clock.

Table 1-2. RS8250 Pin Definitions *(2 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
PMD Line Interface (cont.)	LRxClk+	Line Receive Clock Positive	P11	PECL	I	This pin is the receive clock.
	LRxData–	Line Receive Input Negative	P10	PECL	I	This pin receives differential serial NRZ data from the PMD.
	LRxData+	Line Receive Input Positive	M10	PECL	I	Receives differential serial NRZ data from the PMD.
	LSigDet	Line Signal Detection	L9	TTL or PECL	I	This pin is normally connected to the Signal Valid output of the PMD and must be asserted high when the PMD is receiving a valid signal. Designs that do not use a Signal Valid from the PMD must tie this input high. Conexant recommends that a comparator be used (see Figure 2-3).
	LPLLClk	Line Phase Loop Lock Clock	P5	TTL	I	This pin is a 19.44 MHz clock input. The transmit synthesizer (PLL) uses this clock to generate 155.52 MHz LTxClkO output when bits 3 and 4 of the CLKREC register (0x01) are set to 0. ***NOTE(S):*** The transmit synthesizer PLL and clock recovery PLL use this input as a reference clock regardless of the timing source selection.
Microprocessor Interface	MClk, MAcsSel	Microprocessor Clock, Access Time Select	L3	TTL	I	When MSyncMode is set to a logic 1, the MClk pin is a clock signal that samples the microprocessor interface pins (MCs*, MW/R*, MAs*, MAddr[6:0], MData[7:0]) on its rising edge. Additionally, the rising edge of MClk may cause the microprocessor interface output pins (MData[7:0], MInt*) to change states. When MSyncMode is set to a logic 0, the MAcsSel pin selects the asynchronous interface access time. A logic 0 selects a power-saving access mode (130 ns) while a logic 1 selects the high-performance access mode (80 ns).
	MSyncMode	Microprocessor Synchronous/Asynchronous Bus Mode Select	M1	TTL	I	A logic 1 selects the synchronous bus mode compatible with Bt8230 and Bt8233. In this mode, the microprocessor pins are defined as follows: MClk (pin 30), MW/R* (pin 7), MAs* (pin 9), MCs* (pin 8), MInt* (pin 6), MAddr (pins 12-18), and MData (pins 20-28). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MAcsSel (pin 30), MRd* (pin 7), MWr* (pin 9), MCs* (pin 8), MInt* (pin 6), MAddr (pins 12-18), and MData (pins 20-28).
	MCs*	Microprocessor Chip Select	C1	TTL	I	When MCs* is set to a logic 0, the device is enabled for read and write accesses. When MCs* is set to a logic 1, the device does not respond to input signal transitions on MClk, MAcsSel; MW/R*, MRd*; or MAs*, MWr*. Additionally, when MCs* is set to a logic 1, the MData[7:0] pins are in a high-impedance state but the Int* pin remains operational.

Table 1-2. RS8250 Pin Definitions *(3 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Microprocessor Interface (cont.)	MW/R*, MRd*	Microprocessor Write/Read, Read Control	C2	TTL	I	When MSyncMode is set to a logic 1, this pin is a read/write control pin. In this mode, when MW/R* is set to a logic 1, a write access is enabled, and the MData[7:0] pin values are written to the memory location indicated by the MAddr[6:0] pins. Also in this mode, when MW/R* is set to a logic 0, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read and its value placed on the MData[7:0] pins. Both read and write accesses assume the device is chip selected (MCs* = 0), the address is valid (MAs* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is set to a logic 0, this pin is a read control pin. In this mode, when Rd* is set to a logic 0, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read and its value placed on the MData[7:0] pins. The read access assumes the device is chip selected (MCs* = 0), a write access is not being requested (MWr* = 1), and the device is not being reset (Reset* = 1).
	MAs*, MWr*	Microprocessor Address Strobe, Write Control	D2	TTL	I	When MSyncMode is set to a logic 1, this pin is an address strobe pin. When the MAs* pin is set to a logic 0, it indicates a valid address, MAddr[6:0]. This signal is used to qualify read and write accesses. When MSyncMode is set to a logic 0, this pin is a write control pin. When MWr* is set to a logic 0, a write access is enabled and the MData[7:0] pin values are written to the memory location indicated by the MAddr[6:0] pins. The write access assumes the device is chip selected (MCs* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1).
	MAddr[6]	Microprocessor Address Bus	E3	TTL	I	These seven bits are an address input for identifying the register that is accessed.
	MAddr[5]		E4	TTL	I	
	MAddr[4]		F2	TTL	I	
	MAddr[3]		F1	TTL	I	
	MAddr[2]		F3	TTL	I	
	MAddr[1]		F4	TTL	I	
	MAddr[0]		G2	TTL	I	

Table 1-2. RS8250 Pin Definitions *(4 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Microprocessor Interface (cont.)	MData[7]	Microprocessor Data Bus	G3	TTL	I/O	These eight bits are a bidirectional data bus for transferring the read and write data.
	MData[6]		H1	TTL	I/O	
	MData[5]		H2	TTL	I/O	
	MData[4]		J1	TTL	I/O	
	MData[3]		J4	TTL	I/O	
	MData[2]		K1	TTL	I/O	
	MData[1]		K3	TTL	I/O	
	MData[0]		K2	TTL	I/O	
	MInt*	Microprocessor Interrupt	B1	TTL	O	When a logic 0 is read on this pin, the device needs servicing. It remains asserted until the pending interrupt is acknowledged. This pin is an open drain output for an external wired OR logic implementation.
JTAG (See IEEE 1149.1a-1993)	TRST*	Test Reset	M4	TTL	I	When this pin is asserted, the internal boundary-scan logic is reset. This pin has a pullup resistor.
	TCK	Test Clock	N4	TTL	I	This pin samples the value of TMS and TDI on its rising edge in order to control the boundary scan operations.
	TMS	Test Mode Select	P4	TTL	I	This pin controls the boundary-scan Test Access Port (TAP) controller operation.
	TDI	Test Data Input	L4	TTL	I	This pin is the serial test data input.
	TDO	Test Data Output	N5	TTL	O	This pin is the serial test data output.

Table 1-2. RS8250 Pin Definitions *(5 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Status	StatOut[7]	Status Outputs[7:0]	A4	TTL	O	This pin reflects either the value in bit 7 of the OUTSTAT register (0x41) or LOS, as selected by bit 2 of register GEN (0x00). If selected by bit 0 or 1 of RXLIN (0x46), this pin will be the D1-D3 or D4-D12 receive data link serial clock output (WAN only).
	StatOut[6]		C4	TTL	O	This pin reflects either the value in bit 6 of the OUTSTAT register (0x41) or OOF, as selected by bit 2 of register GEN (0x00). If selected by bit 0 or 1 of RXLIN (0x46), this pin will be the D1-D3 or D4-D12 receive data link serial data output (WAN only).
	StatOut[5]		B4	TTL	O	This pin reflects either the value in bit 5 of the OUTSTAT register (0x41) or LOP, as selected by bit 2 of register GEN (0x00). For WAN only: if selected by bit 0 or 1 of RXLIN (0x46), this pin will be the D1-D3 or D4-D12 receive data link indication output. This output is high during the time that clock/data outputs contain pulses for D1-D3 octets. It is low during the time that clock/data outputs contain pulses for D4-D12 octets.
	StatOut[4]		A3	TTL	O	This pin reflects either the value in bit 4 of the OUTSTAT register (0x41) or AIS-L, as selected by bit 2 of register GEN (0x00). If selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin will be the D1-D3 or D4-D12 transmit data link serial clock output (WAN only).
	StatOut[3]		C3	TTL	O	This pin reflects either the value in bit 3 of the OUTSTAT register (0x41) or RDI-L, as selected by bit 2 of register GEN (0x00). For WAN only: if selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin will be the D1-D3 or D4-D12 transmit data link indication output. This output is high during the time that clock/data inputs are expected for D1-D3 octets, and low for D4-D12.
	StatOut[2]		B3	TTL	O	This pin reflects either the value in bit 2 of the OUTSTAT register (0x41) or AIS-P, as selected by bit 2 of register GEN (0x00). For WAN only: if selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin will output a pulse at the beginning of every cell slot time (both idle and data cells), synchronized to the UTOPIA transmit side.
	StatOut[1]		A2	TTL	O	This pin reflects either the value in bit 1 of the OUTSTAT register (0x41) or RDI-P, as selected by bit 2 of register GEN (0x00).
	StatOut[0]		B2	TTL	O	This pin reflects either the value in bit 0 of the OUTSTAT register (0x41) or LOCD, as selected by bit 2 of register GEN (0x00).
Data Link	TxDL	Transmit Data Link Input	P3	TTL	I	This pin is used to serially transmit data over the D1-D3 and D4-D12 data link (WAN only).

Table 1-2. RS8250 Pin Definitions *(6 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Transmit	UTxClk	UTOPIA Transmit Clock	D14	TTL	I	The data transfer/interface byte clock is provided by the ATM layer to the PHY layer for synchronizing transfers on UTxData.
	UTxEnb*	UTOPIA Transmit Enable	E11	TTL	I	The enable data transfers signal is active low. It is asserted by the ATM layer during cycles when UTxData contains valid cell data.
	UTxAddr[0]	LSB	P12	TTL	I	These pins are the address of the PHY device being selected. The address is driven from the ATM to the multi-PHY layer to poll and select the appropriate multi-PHY device. Each multi-PHY device must maintain its address. Address 31 indicates a null PHY port.
	UTxAddr[1]	UTOPIA Transmit Address	M12	TTL	I	
	UTxAddr[2]		N12	TTL	I	
	UTxAddr[3]		P13	TTL	I	
	UTxAddr[4]	MSB	N13	TTL	I	
	UTxData[0]	UTOPIA Transmit Data	M14	TTL	I	The data bus is driven from the ATM layer to the PHY. UTxData[15] is the MSB of the high octet and UTxData[7] is the MSB of the lower octet.
	UTxData[1]		L13	TTL	I	
	UTxData[2]		L14	TTL	I	
	UTxData[3]		K13	TTL	I	
	UTxData[4]		K14	TTL	I	
	UTxData[5]		J14	TTL	I	
	UTxData[6]		J12	TTL	I	
	UTxData[7]		J11	TTL	I	
	UTxData[8]		H13	TTL	I	
	UTxData[9]		H14	TTL	I	
	UTxData[10]		H11	TTL	I	
	UTxData[11]		G12	TTL	I	
	UTxData[12]		G14	TTL	I	
	UTxData[13]		G13	TTL	I	
	UTxData[14]		F14	TTL	I	
	UTxData[15]		F13	TTL	I	
	UTxPrty	UTOPIA Transmit Parity Input	E14	TTL	I	The Transmit Data bus checks for odd parity over UTxData [7:0] coming from the ATM layer. In 16-bit mode, it checks for odd parity over UTxData[15:0].

Table 1-2. RS8250 Pin Definitions *(7 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Transmit (cont.)	UTxSOC	UTOPIA Transmit Start of Cell	E13	TTL	I	The Start of Cell signal is active high. It is asserted by the ATM layer during cycles when UTxData contains the first valid byte of the cell.
	UTxClAv	UTOPIA Transmit Cell Available	E12	TTL	O	This signal indicates FIFO full or Cell Buffer Available. For octet-level flow control, this signal is active low from the PHY layer to the ATM layer. It is asserted to indicate that a maximum of four more transmit data writes will be accepted. For cell-level flow control in an multi-PHY environment, UTxClAv is an active high signal with high impedance potential going from the multi-PHY layer to the ATM layer. A polled multi-PHY device drives this signal only during each cycle following one with its address on the UTxAddr lines. The polled multi-PHY device asserts UTxClAv high to indicate it can accept the transfer of a complete cell, otherwise it deasserts the signal.(1)
UTOPIA Receive	URxClk	UTOPIA Receive Clock	C14	TTL	I	The data transfer/interface byte clock is provided by the ATM layer to the PHY layer for synchronizing transfers on URxData.
	URxEnb*	UTOPIA Receive Enable	C13	TTL	I	The enable receive data signal is active low. It is asserted by the ATM layer to indicate that URxData and URxSOC will be sampled at the end of the next cycle. In support of multiple PHY configurations, when URxEnb* is asserted, the URxData and URxSOC PHY layer outputs change to a high-impedance state. URxData and URxSOC must be enabled only in cycles following those with URxEnb* asserted.
	URxAddr[0]	UTOPIA Receive Address	D6	TTL	I	This is the address of the PHY device being selected. It is driven from the ATM to the multi-PHY layer to poll and select the appropriate multi-PHY device. URxAddr [4] is the MSB. Each multi-PHY device must maintain its address. Address 31 indicates a null PHY port.
	URxAddr[1]		A5	TTL	I	
	URxAddr[2]		C5	TTL	I	
	URxAddr[3]		B5	TTL	I	
	URxAddr[4]		D5	TTL	I	

Table 1-2. RS8250 Pin Definitions *(8 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Receive (cont.)	URxData[0]	UTOPIA Receive Data Bus	B12	TTL	O	The data bus is driven from the ATM layer to the PHY layer. URxData[15] is the MSB of the high octet and URxData[7] is the MSB of the lower octet. To support multiple PHY configurations, URxData can be placed in a high-impedance state which is enabled only when URxEnb* is asserted.
	URxData[1]		A12	TTL	O	
	URxData[2]		B11	TTL	O	
	URxData[3]		A11	TTL	O	
	URxData[4]		D11	TTL	O	
	RxData[5]		B10	TTL	O	
	URxData[6]		A10	TTL	O	
	URxData[7]		B9	TTL	O	
	URxData[8]		A9	TTL	O	
	URxData[9]		C9	TTL	O	
	URxData[10]		D9	TTL	O	
	URxData[11]		B8	TTL	O	
	URxData[12]		C8	TTL	O	
	URxData[13]		A7	TTL	O	
	URxData[14]		B7	TTL	O	
	URxData[15]		A6	TTL	O	
	URxPrty	UTOPIA Receive Parity	C6	TTL	O	The data bus parity is odd parity for URxData[7:0], driven by the PHY layer. In 16-bit mode, this is the odd parity bit over URxData[15:0]. To support multiple PHY configurations, URxPrty can be placed in a high-impedance state which is enabled only in cycles following those with URxEnb* asserted.(1)
	URxSOC	UTOPIA Receive Start of Cell	B14	TTL	O	The Start of Cell signal is active high. It is asserted by the PHY layer when RxData contains the first valid byte of the cell. In support of multiple PHY configurations, when URxEnb* is asserted, the URxData and URxSOC PHY layer outputs change to a high-impedance state. URxData and URxSOC must be enabled only in cycles following those with URxEnb* asserted.(1)

Table 1-2. RS8250 Pin Definitions *(9 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Receive (cont.)	URxClAv	UTOPIA Receive Cell Available	C12	TTL	O	This signal indicates FIFO empty or Cell Buffer Available. For octet-level flow control, this signal is active low from the PHY layer to the ATM layer. It is asserted to indicate that in the current cycle there is no valid data for delivery to the ATM layer. For cell-level flow control in an multi-PHY environment, URxClAv is an active high signal with high impedance potential going from the multi-PHY layer to the ATM layer. A polled multi-PHY device drives this signal only during each cycle following one with its address on the URxAddr lines. The polled multi-PHY device asserts URxClAv high to indicate it has a complete cell available for transfer to the ATM layer, otherwise it deasserts the signal.(1)
Supply Voltage	PWR	Supply Voltage	C7 C10 D1 D3 D8 D10 D13 J2 J3 K11 L5 M5 M7	—	—	These pins are power supply connections.
	Analog PWR	Analog Supply Voltage	M9 N9	—	—	This pin is an analog power supply connection.

Table 1-2. RS8250 Pin Definitions *(10 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Supply Voltage (cont.)	GND	Ground	A8 B6 C11 D4 D12 E1 E2 G1 G4 H3 J13 L1 M11 N6 N7 N10 P6	—	—	These pins are ground connections.
	Analog GND	Analog Ground	L8 P9	—	—	This pin is an analog ground connection.
	V_{GG}	Electrostatic Discharge (ESD) Supply Voltage	N11	—	—	This pin is an ESD supply connection. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using in a 3.3 V system only, leave this pin unconnected.

NOTE(S):
(1) RS8250 defaults to UTOPIA Level 2 when reset causing the TxClAv, RxClAv, RxSOC, and RxPrty signals to be in high-impedance state. This may cause initialization problems for ATM layer UTOPIA Level 1 devices. Therefore, it is recommended that pulldown resistors be used for these devices.

1.5 Block Diagram and Descriptions

Figure 1-4 is a detailed block diagram of the RS825x. When traffic is transmitted from the host system, octet-wide or 16-bit data enters the RS825x via the UTOPIA port. The host data is assembled into ATM cells and then formatted for serial-line transmission by the SONET line framer.

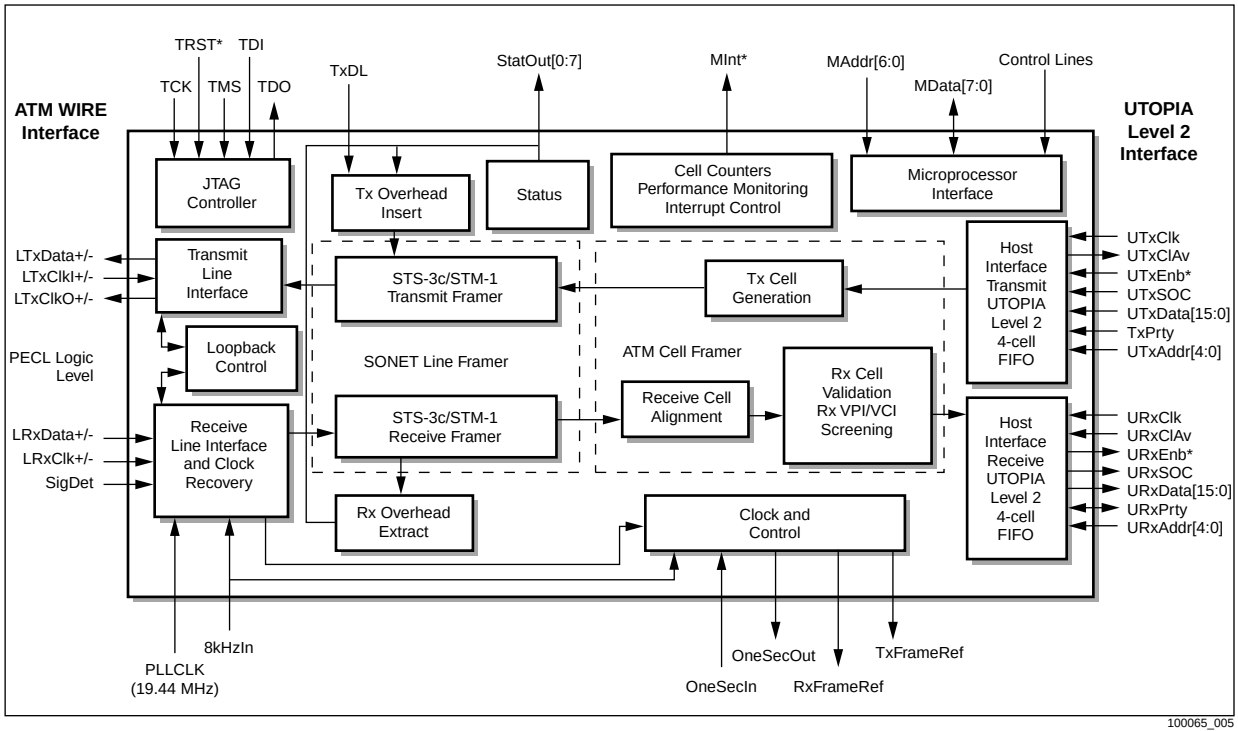
In the receive direction, serial network data is framed to octets by the SONET line framer and passed to the ATM cell processing block. Octet data is then aligned into ATM cells, checked, and sent to the UTOPIA port.

The line framer block connects to external interfaces for line reception and transmission. Also included are overhead interfaces, data links, and event counters.

The HEC ATM cell alignment block accepts octet data from the line framer block. It generates cells for transmission and validates received cells. Included are HEC generators and detectors, data scramblers, and counters.

The UTOPIA interface communicates with the next layer of ATM processing. It controls transmit priority and rate, and has counters for events and errors.

Figure 1-4. RS825x Detailed Block Diagram



2.0 Functional Description

This chapter describes the RS825x architecture and functional blocks. Figure 2-1 shows the RS825x transmit signal path. The RS825x calculates the HEC for incoming ATM cells from the UTOPIA interface and inserts it into the fifth octet of each cell. The result is formatted into SONET frames and converted to serial data. One of four clock sources is used to synchronize the outgoing data stream over the PECL interface.

Figure 2-1. RS825x Transmitter Block Diagram

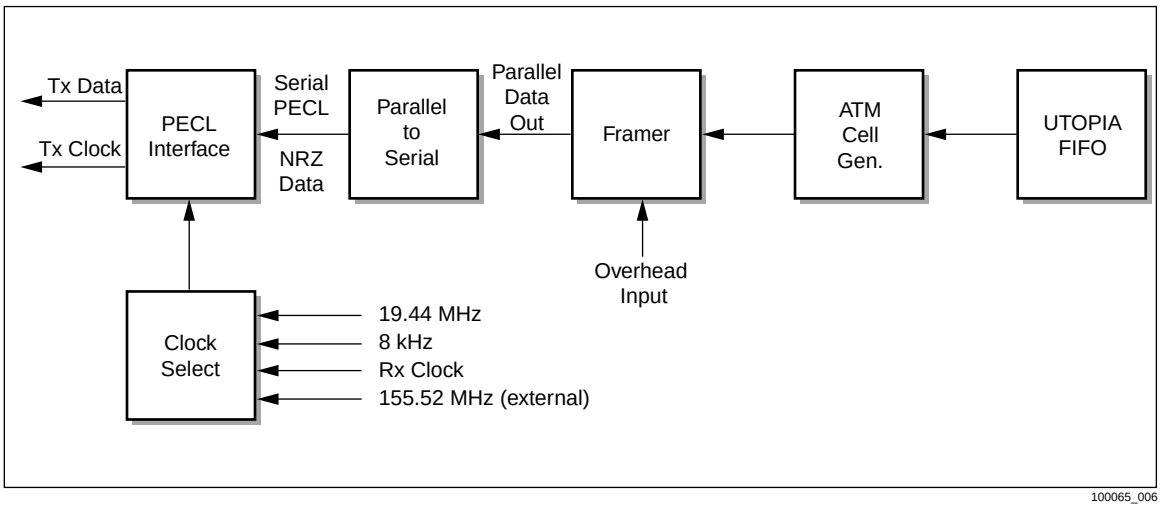
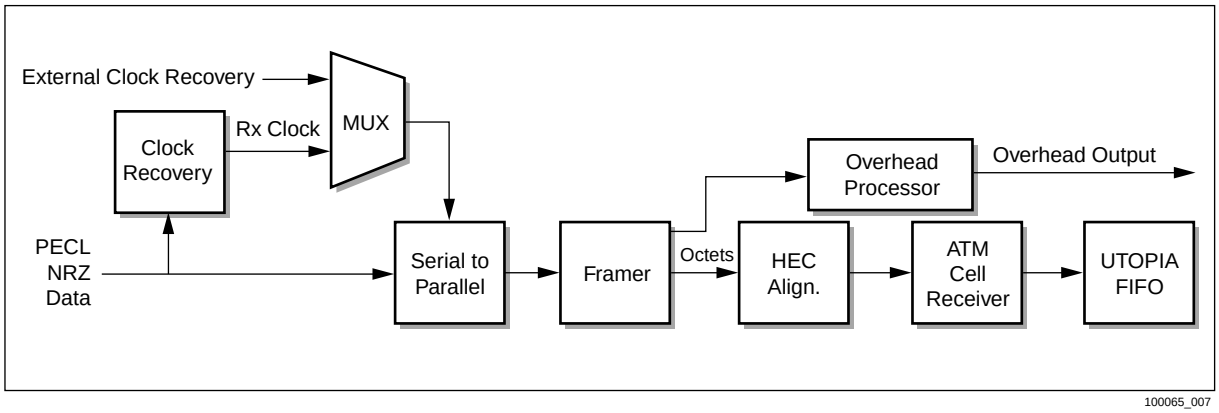


Figure 2-2 shows the RS825x receive signal path. The RS825x recovers the clock from the incoming data stream. The serial data stream is converted to parallel and passed to the framer block where overhead bytes are extracted. HEC alignment is performed to recover the Start of Cell boundary. The cells are then output over the UTOPIA bus to the ATM layer device.

Figure 2-2. RS825x Receiver Block Diagram



2.1 Line Interface

The RS825x communicates with the external network through its line interface, which can connect to either Category (Cat) 5 UTP (Unshielded Twisted Pair) or fiber optic cable. The PHY performs clock recovery via an onboard PLL circuit, which requires no external components. The actual modulation is controlled by a Physical Media Dependent (PMD) device connected to the RS825x via this ATM Forum-compliant WIRE (Workable Interface Requirements Example) interface. The line interface consists of two types of logic, Transistor-Transistor Logic (TTL) and Pseudo-Emitter Coupled Logic (PECL).

2.1.1 TTL/PECL Interface

The LSigDet pin on the RS825x line interface can be driven by TTL or PECL drivers. The RS825x can be connected directly to a TTL interface without external components. When using a single-ended PECL interface, the input signal must be centered around V_{sref} as shown in Table 2-1.

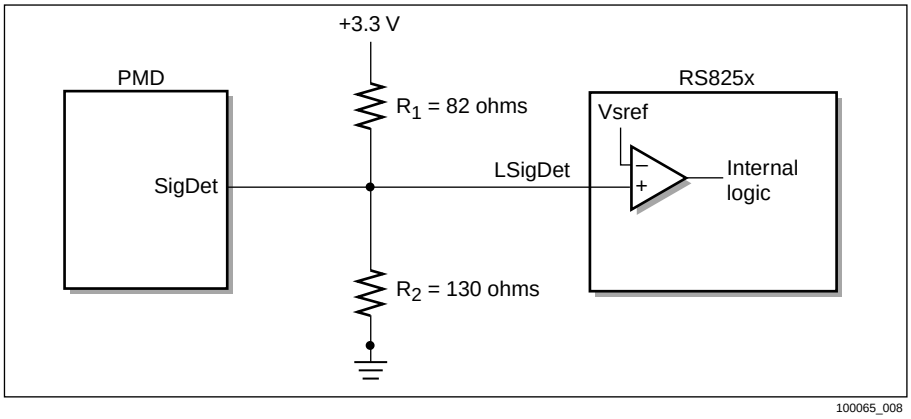
NOTE: For RS825x Revision 14 and later, LSigDet is compatible with single-ended PECL devices.

Table 2-1. Single-ended PECL Table

Symbol	Parameter	Minimum	Typical	Maximum
V_{sref}	Mid-point	Vdd - 1.26	Vdd - 1.25	Vdd - 1.24
V_{ih}	—	V_{sref} + 60 mV	—	—
V_{il}	—	—	—	V_{sref} – 60 mV
I_{ih}	—	—	—	10 µA
I_{il}	—	-10 µA	—	—

A typical PMD/PECL interface is shown in Figure 2-3. This block diagram assumes a 3.3 V PMD. Resistors R1 and R2 set the low-level input voltage, V_{il}, going to the RS825x. The values shown set V_{il} at 1.65 V, which is well below the minimum required by the RS825x. If an external driver/buffer is used, it must provide a current return path to Vdd to reduce noise issues.

Figure 2-3. Single-ended PECL Diagram



2.1.2 PECL Interface

A PECL device requires the same voltage differential on the inputs as an Emitter Coupled Logic (ECL) device. The PECL device is referenced to a positive source, which is generally 3.3 V or 5.0 V. Use caution when interfacing components that use different V_{cc} levels.

The RS825x has five pairs of differential PECL pins: LTxClkI+/-, LTxClkO+/-, LRxClk+/-, LTxDat+/-, and LRxDat+/-. These pins are described in Table 1-2. All inputs and outputs include a positive pin and a negative pin. The voltage difference between the two pins determines the logic value under normal operating conditions (see Section 5.3). The input logic for this PECL interface is shown in Table 2-2.

Table 2-2. PECL Input Logic Table

Input +	Input -	Internal Logic Level
0	0	Invalid
0	1	0
1	0	1
1	1	Invalid

The output logic table for this PECL interface is shown in Table 2-3.

Table 2-3. PECL Output Logic Table

Internal Logic Level	Output +	Output –
0	High Z	1
1	1	High Z

This high-impedance output condition necessitates the use of a pulldown resistor for setting the proper output voltages. Details for selecting the resistor are given in Chapter 3.0.

2.2 Clock Circuits

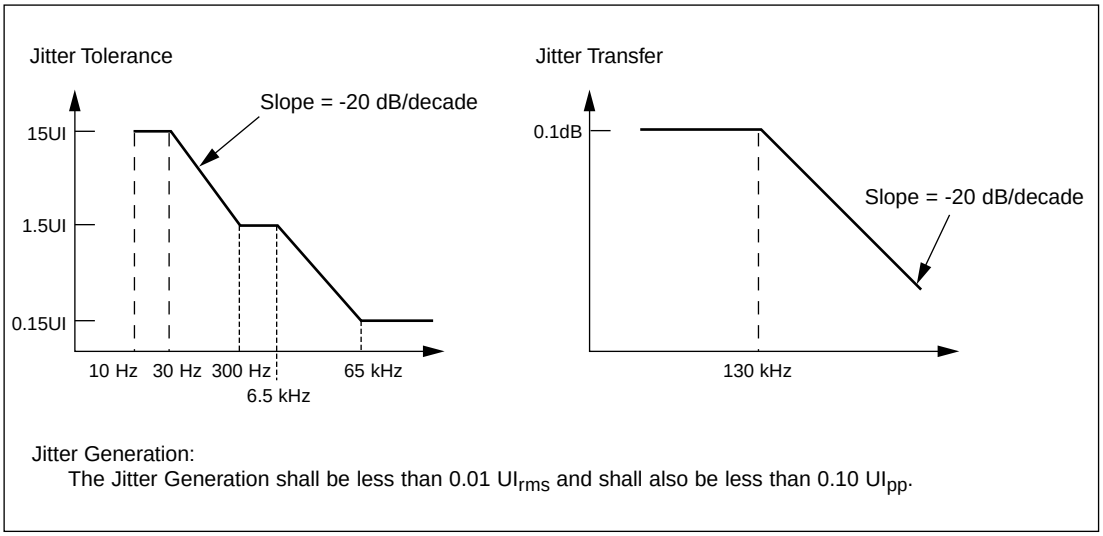
The clock circuit has a receiver section and a transmit section. The transmit section synthesizes the 155.52 MHz clock used for transmitting data. One of four clock sources can be selected by bits 3 and 4 of the CLKREC register (0x01).

- By default, this clock is synthesized from the 19.44 MHz LPLLClk reference input pin (pin 44).
- The clock can be phase-locked to an 8 kHz clock input. This is useful for synchronizing the device with Building Integrated Timing Supply (BITS) clocks.
- If a 155.52 MHz clock is provided on pins 47 and 48, it can be used directly as the transmit clock (bypassing synthesis altogether). The external clock must be accurate to within 20 ppm of 155.52 MHz.
- The clock can be synthesized from the received data via the receiver section.

The receiver section uses an internal Phase Locked Loop (PLL) to recover the clock from the incoming NRZ data stream. The clock recovery circuit requires the 19.44 MHz clock from pin 44. When no NRZ data is present or when the signal detect input (LSigDet, pin 57) is low, indicating that the signal has been lost by the optical transceiver, the receive clock recovery circuit free-runs at a nominal 155.52 MHz so that there is always a receive clock present for the receive data path and the transmit path for loop-timed applications.

This clock meets jitter tolerance and jitter transfer specifications according to Bellcore GR-253 (see Figure 2-4). Jitter tolerance is defined as how much jitter the receiver can tolerate and still extract the correct data from the incoming signal. Jitter transfer is the maximum amount of jitter that any device is allowed to add to the data stream.

Figure 2-4. Bellcore GR-253-CORE Jitter Specifications



2.2.1 Loss of Lock

Loss of Lock (LOL) status indicates that the receive PLL has lost synchronization. When LOL occurs, bit 6 of the SECINT register (0x3D) is asserted if it has been enabled by bit 6 of the ENSEC register (0x35). LOL also appears in bit 6 of the RXSEC register (0x45).

2.3 Serial-Parallel Conversion

The RS825x performs the serial/parallel conversions needed between the SONET/SDH block and the PMD. Serial data from the clock recovery block is converted to 8-bit parallel data by determining octet boundaries based on the A1, A2 bytes (see Section 2.4.2.1). It can then be processed by the SONET/SDH block. After cell processing and SONET framing, 8-bit parallel outgoing data is converted to a bit-serial data stream for transmission by the PMD.

2.4 SONET/SDH Framer and Overhead Processor

Conexant's RS825x SONET/SDH framer has an extensive SONET overhead processing section with external access for D1-D3 and D4-D12 Data Link message processing. The framer provides data transmission at a standard bit rate, frequency justification, pointer processing, and SONET frame delineation. The SONET Overhead processor provides frame synchronization, byte scrambling and descrambling, and byte multiplexing and demultiplexing.

The frame structure for STS-3c/STM-1 can be envisioned as a 270-column by nine-row rectangle of bytes (octets) shown in Figure 2-5. The transmission of the block starts with the first row, working from left to right, then moves to the second row, left to right, and so on down to the byte in the bottom right corner. Thus, the transport overhead octets are actually transmitted in nine groups of nine octets, equally spaced throughout the frame. Since there are 270 x 9 bytes, the data rate is 270 x 9 x 8 (bits/bytes) x 8,000 fps. (the frame period is 125 micro-seconds) = 155.52 Mbps.

Figure 2-5. STS-3c/STM-1 Basic Frame

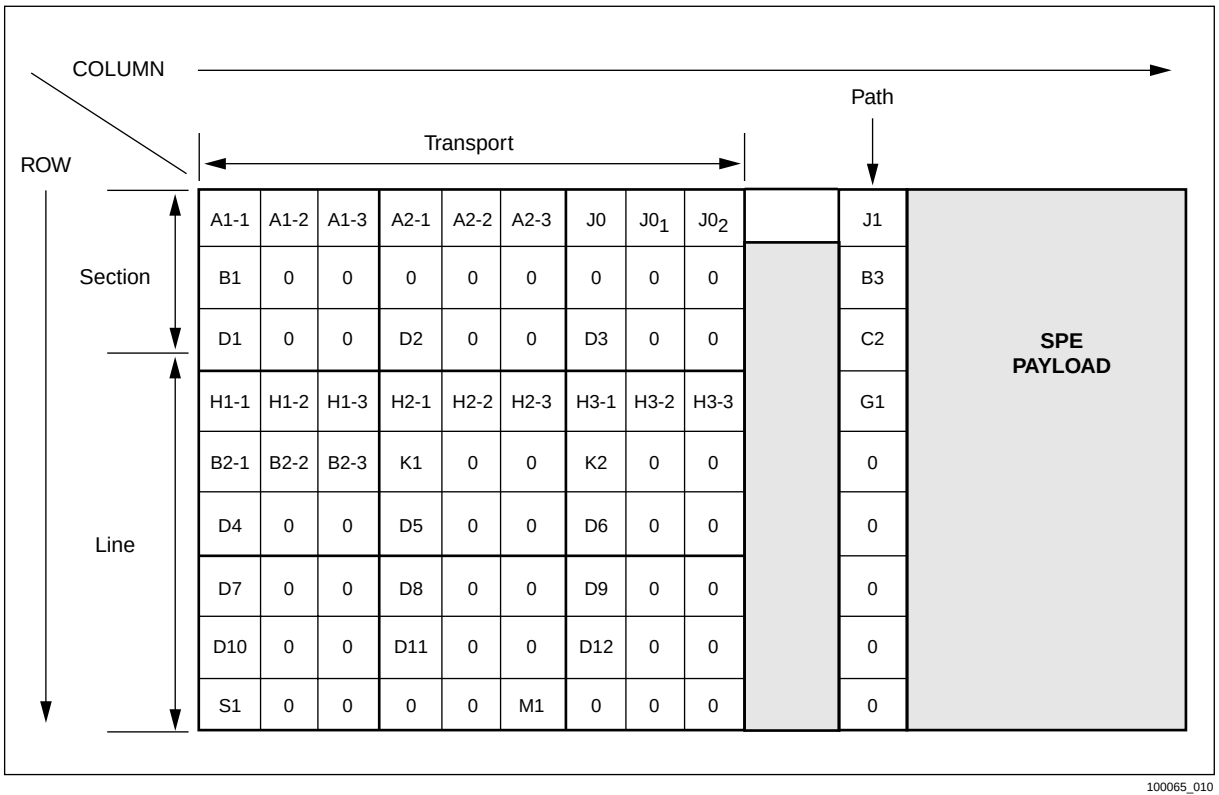
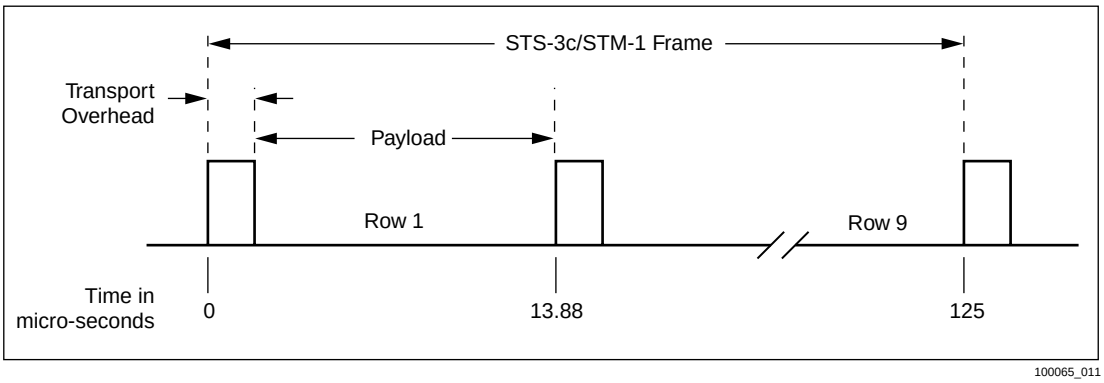


Figure 2-6 provides a linear representation of STS-3c/STM-1 framing. This framing is similar to T1 framing except that SONET delineates the frame with a block of octets, A1 and A2, instead of just one bit. There is payload data in the areas between overhead blocks. In STS-3c, the payload is called the Synchronous Payload Envelope (SPE). In SDH, the payload is called Virtual Container 4 (VC4). This document uses SPE to refer to the payload in either format.

Figure 2-6. STS-3c/STM-1 Frame Timing



The SONET Framer block recovers the A1/A2 framing location from octet-delineated data provided by the clock recovery front-end. This block also performs the pointer processing and generates row and byte counts to identify locations within the frame to downstream blocks such as the SONET overhead processor. The SONET Framer block interfaces directly with the SONET Overhead block and provides status bits to the SONET overhead processor for presentation in status registers. The SONET Overhead block uses defined overhead bytes in an STS-3c/STM-1 frame for Performance Monitoring, Fault Management, and Facility Testing. The SONET Overhead bytes used in the RS825x are listed in Table 2-4, *SONET Overhead Byte Definitions and Values*.

Table 2-4. SONET Overhead Byte Definitions and Values

Layer	Byte	Function	Value
Section	A1	Framing	$F6_h$
	A2	Framing	28_h
	J0	Section Trace	01_h or 64-byte Section Trace message
	$Z0_1$ $Z0_2$	Section Growth “National Bytes”	02_h 03_h
	B1	Section error monitoring	BIP-8
	D1, D2, D3	Data Link channel (WAN only)	—

Table 2-4. SONET Overhead Byte Definitions and Values

Layer	Byte	Function	Value
Line	H1, H2, H3	Pointer/Concatenation indicator Path AIS	see Table 2-7
	B2-1, B2-2, B2-3	Line error monitoring	BIP-24
	K1, K2 (bits 1-5)	APS channel (WAN only)	0000_h (default)
	K2 (bits 6-8)	No alarm Line AIS Line RDI (WAN only)	0_h (default) 7_h 6_h
	D4-D12	Data Link channel (WAN only)	—
	S1	Synchronization Status (WAN only)	programmable
	M1	Line FEBE	B2 error count
Path	J1	Path Trace	00_h or 64-byte Path Trace Message
	B3	Path error monitoring	BIP-8
	C2	Path signal label: ATM Path signal label: Equipped Nonspecific Path signal label: Unequipped User defined for non-ATM applications	13_h (default) 01_h 00_h xx
	G1 (bits 1-4)	Path FEBE	B3 error count
	G1 (bits 5-7)	No alarm Path RDI alarms	0_h (default) $2_h, 5_h, 6_h$

2.4.1 Loss of Signal

The scrambled STS-3c/STM-1 data is monitored for the absence of 1s. When 1620 consecutive octets (6 SONET rows) of 0s are detected, LOS is declared. LOS is cleared when two valid framing words (A1/A2) are received with no intervening LOS detection. The LOS condition is reflected in register RXSEC (0x45) bit 5. In addition, StatOut[7] (pin 126) is asserted if Status Output Pin Mode, bit 2 of the GEN register (0x00), is enabled.

2.4.2 Section Overhead

The Section Overhead handles the transport of the STS-3c/STM-1 frame across the physical medium and section-level communications. Its functions are framing and scrambling on the transmit side, and section error monitoring on the receive side. The transmit and receive functions of the Section Overhead bytes are described in Table 2-5.

Table 2-5. Section Overhead Transmit and Receive Functions

Byte	Transmit	Receive
A1/A2	F6/28 hex or disable 00	Monitor out of frame state machine
B1	Calculated, error insertion option	Checked, errors counted
D1, D2, D3 (WAN only)	00 hex or external serial access	External serial access
J0	01 hex or 64-byte trace buffer	Monitor Rx trace buffer, interrupt on change
$Z0_1$, $Z0_2$	02, 03 hex	Not checked

2.4.2.1 A1, A2 The STS-3c/STM-1 framing bytes, A1 and A2, are used to determine OOF status. When these octets match the framing pattern, the status is “in-frame.” When there are four consecutive frames with one or more framing pattern errors, OOF is declared. This condition asserts StatOut[6] (pin 127) and is reflected in register RXSEC (0x45) bit 4. The transmit A1/A2 bytes can be disabled by writing bit 4 in the TXSEC (0x0C) register to 1. A1 can be inverted by writing bit 7 in the ERRINS (0x06) register to 1. One valid A1/A2 frame clears OOF status.

2.4.2.2 Loss of Frame A Loss of Frame (LOF) condition is declared when Out-of-Frame (OOF) status exists for 24 consecutive frames. This condition is cleared when OOF status is cleared. LOF is reflected in register RXSEC (0x45) bit 3.

2.4.2.3 B1 The Section Bit Interleaved Parity (BIP)-8 byte, B1, is allocated for section layer error monitoring. This byte contains a BIP-8 code using even parity. The code is calculated using all the bits of the previous STS-3c/STM-1 frame after scrambling. Each piece of section terminating equipment calculates the B1 byte of the current STS-3c/STM-1 frame and compares it with the B1 byte received from the next STS-3c/STM-1 frame. If the B1 bytes match, there is no error. If the B1 bytes do not match, the alarm indicator is set. The B1 bytes of the rest of the STS-3c/STM-1 frame are not defined. As many as 64 kb errors per second can be detected. These section level bit errors are gathered in a 16-bit counter (registers B1CNTL [0x54] and B1CNTH [0x55]). The counter is latched so that it can continue to count while the latch is being read. This prevents the loss of any error counts.

2.4.2.4 D1-D3 See Section 2.6

2.4.2.5 J0 The Section Trace byte, J0, is connected to a circular 64-byte buffer, carrying the Section Trace message, which allows section elements to track a continuous connection. This buffer overwrites when full. This message is user-programmable but generally is an 8-bit ASCII CLLI™ code padded with ASCII NULL characters and terminated with CR and LF characters making up 64 bytes total. If Section Trace is enabled, the user is required to enter a message or the current contents of the transmit buffer will be transmitted. If J0 is disabled, 64 impedance are transmitted. J0 can be disabled via register TXSEC (0x0C), bit 5. The J0 transmit buffer is located in register TXSECBUF (0x68). The J0 receive buffer is RXSECBUF (0x6A). If the incoming message differs from the data stored in the receive buffer from the previous message received, an interrupt appears in register SECINT (0x3D) bit 1.

2.4.2.6 Z0 The Section Growth bytes, $Z0_1$ and $Z0_2$, are set to defaults of 02 and 03, respectively.

2.4.3 Line Overhead

The Line Overhead handles the transport of path-level payloads across the physical medium. This layer of the overhead provides synchronization and multiplexing functions for the Line layer. These functions include maintenance and line protection. The Section Overhead must be terminated before the Line Overhead can be accessed. The transmit and receive functions of the Line Overhead are described in Table 2-6.

Table 2-6. Line Overhead Transmit and Receive Functions

Byte	Transmit	Receive
H1/H2	620A/93FF hex pointer	Full GR.253 pointer processor
H3	00 hex	Used in pointer processor
B2	Calculated, error insertion	Checked, errors counted
K1/K2 (WAN only)	Insertable via register	Checked, interrupt on change
D4-12 (WAN only)	00 hex or external serial access	External serial access
S1 (WAN only)	Insertable via register	Checked, interrupt on change
M1	Line FEBE inserted	Checked, errors counted

2.4.3.1 H1, H2, and H3

Bytes H1, H2, and H3 in the STS-3c/STM-1 frame are fixed on the transmit side to locate path overhead byte J1 immediately after the $Z0_2$ byte of the Section Overhead. The receive side performs all processing according to GR-253.

Table 2-7. H1, H2, and H3 Functions

Overhead Byte	STS-3c Value (in hex)	STM-1 Value (in hex)	Error Conditions
H1-1 Transmit	62	6A	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D). 33 hex is inserted for invalid pointer via control bit DisPntr (bit 6) in the TXLIN register (0x0D).
H1-2 Transmit	93	93	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D).
H1-3 Transmit	93	93	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D).
H2-1 Transmit	0A	0A	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D). 33 is inserted for invalid pointer via control bit DisPntr (bit 6) in the TXLIN register (0x0D).
H2-2 Transmit	FF	FF	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D).
H2-3 Transmit	FF	FF	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D).
H3-1 Transmit	00	00	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D).
H3-2 Transmit	00	00	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D).
H3-3 Transmit	00	00	FF hex is inserted via line AIS control bit, InsLnAIS (bit 3) in the TXLIN register (0x0D).

2.4.3.2 Loss of Pointer

A Loss of Pointer (LOP) condition is declared when eight frames of invalid H1, H2 octets are detected. This condition is cleared when three valid H1, H2 pointer frames occur. LOP is described in register RXLIN (0x46) bit 7.

2.4.3.3 B2-1, B2-2, and B2-3

The Line BIP-8 bytes, B2-1, B2-2, and B2-3, are used for line error monitoring. Similar to the B1 byte in the Section Overhead, B2 also uses Bit Interleaved Parity (BIP-24) code with even parity. It contains the result from the calculation of all the bits of the line overhead and STS-1 envelope capacity of the previous STS-1 frame before scrambling.

The STS-3c/STM-1 signal's Line Overhead bytes provide a BIP-8 code using even parity. One byte (either B2-1, B2-2, or B2-3) in the Line Overhead is allocated for a Line BIP-8 calculation on each STS-1 line within the STS-3c/STM-1 section. The Line BIP-8 is calculated for all the bits of the STS-1 line Overhead and Envelope Capacity of the previous frame before scrambling. Thus, in an STS-3c/STM-1 signal, 3 bytes (B2-1, B2-2, and B2-3) are used for the error monitoring function.

As many as 192 k errors per second can be detected. The errors are accumulated in an 18-bit counter (B2CNTL, B2CNTM, B2CNTH; 0x50, 0x51, 0x52). The counter is latched so that it can continue counting while the latch is being read. This prevents loss of any error counts.

Errors can be inserted via register ERRINS (0x06), bits 5, 4, and 3. Bit 5 corresponds to B2-1, bit 4 corresponds to B2-2, and bit 3 corresponds to B2-3.

2.4.3.4 APS Threshold (WAN only)

Automatic Protection Switching (APS) thresholds are monitored by estimating the incoming Bit Error Rate (BER) and setting an alarm status bit and interrupt when the programmed threshold is crossed. Two thresholds are supported: one for Signal Degrade (SD) and one for Signal Fail (SF). Each threshold is programmable for BER levels from 10^{-3} to 10^{-9} in the APSTHRESH register (0x09). Table 2-8 describes the programming range for the thresholds in APSTHRESH. The alarm clearing threshold and observation time are automatically set to 1/10 of the programmed alarm detection threshold.

Table 2-8. SF/SD Threshold Table

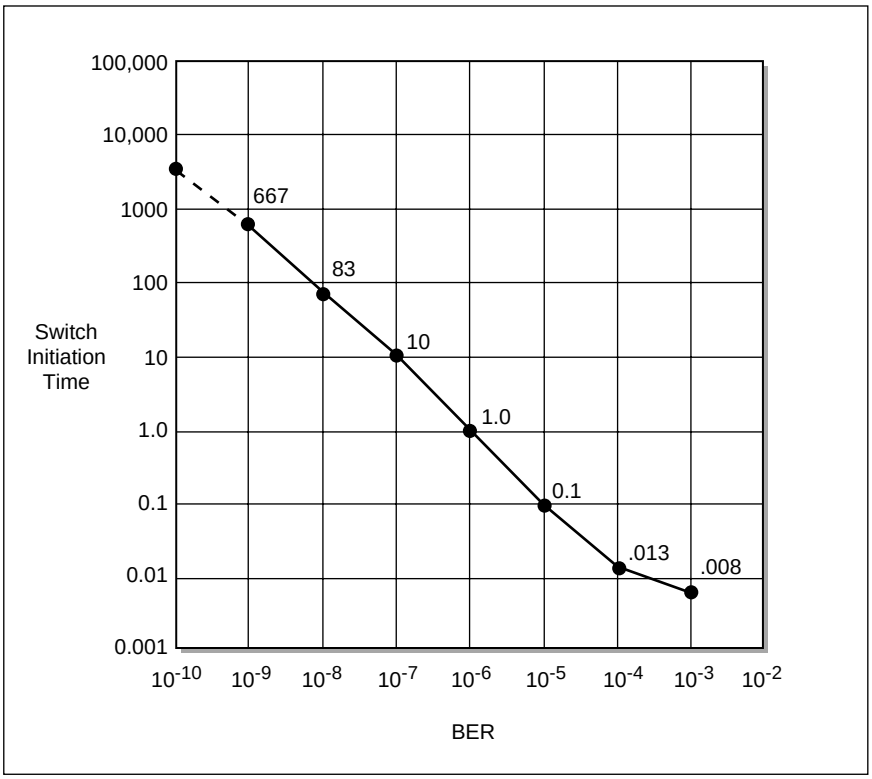
SF Thresh (bits 7-4) SD Thresh (bits 3-0)	Detection Threshold	Clearing Threshold	95% Confidence Interval	RS825x Observation Time	Required Switch Initiation Time
0_h to 3_h	10^{-3}	10^{-4}	64.5 µs	1 ms	8 ms
4_h	10^{-4}	10^{-5}	645 µs	2 ms	13 ms
5_h	10^{-5}	10^{-6}	6.45 ms	16 ms	100 ms
6_h	10^{-6}	10^{-7}	64.5 ms	128 ms	1 s
7_h	10^{-7}	10^{-8}	645 ms	2.048 s	10 s
8_h	10^{-8}	10^{-9}	6.45 s	16.384 s	83 s
9_h to F_h	10^{-9}	10^{-10}	64.5 s	131 s	667 s

The implementation supports the APS switch initiation time requirements shown in Figure 2-7 (from Bellcore Standard *GR-000253-CORE*). The implementation estimates the incoming BER to a >95% confidence level by observing the number of errors per frame as monitored by the B2 line BIP bytes. Table 2-9 describes the required confidence interval for estimating BER versus programmed threshold level. In addition, Table 2-8 describes the actual observation time implemented by the RS825x threshold monitor. This time is the maximum interval for the RS825x to notify via status/interrupt that the programmed threshold has been crossed. These alarm notification times allow software time to process the interrupt and initiate the switching function within the required switch initiation time.

If the incoming BER is actually higher than the programmed threshold, notification takes place in the amount of time listed for the threshold that matches the incoming BER. For example, if the SF threshold is programmed to monitor for BER at a level of 10^{-5} (notification time 16 ms or less) but the actual incoming BER is 10^{-3} the SF status/interrupt is set within 1 ms instead of waiting until the end of the 16 ms window. This allows switch initiation to begin based on the actual incoming BER level versus the programmed level as required by Bellcore Standard GR-000253-CORE. Alarm clearing (when the BER drops below 1/10 of

the programmed threshold) requires observation of the BER for the entire duration of the window as listed for the programmed threshold level. Interrupts occur both when the detection threshold is crossed (BER exceeds programmed threshold) and when the alarm is cleared (BER is below 1/10 of the programmed threshold).

Figure 2-7. Switch Initiation Time Graph



2.4.3.5 K1 and K2 (WAN only)

The APS Channel bytes, K1 and K2, are allocated for Automatic Protection Switching (APS) signaling between line level entities. These bytes are defined only once in an STS-3c/STM-1 signal. The K1/K2 Transmit control registers (0x10/0x11) allow transmission of any value in support of APS. The K2 byte, bits 6–8, Remote Defect Indicator (RDI), and Alarm Indication Signal (AIS), are used to indicate STS line yellow, an alarm condition to the downstream line equipment. The K2 receive status register (0x15) allows observation of incoming octet values. An interrupt can be sent for any change in the received value.

K1/K2 - K1/K2 status occurs when the receiver K1/K2 values are the same for three consecutive frames, but different from the previously latch values. When this occurs, the new values are latched, and an interrupt is generated. A Protection Switching Byte Failure (PSBF) alarm is declared if no three adjacent frames contain the same K1 value in 12 consecutive frames. Bit 4 of the RXAPS register (0x4A) indicates PSBF.

RDI—Line RDI occurs when five consecutive frames containing 110 in bits 6, 7, and 8 are detected in the K2 octet. It is removed when five consecutive frames of any other pattern are detected. Line RDI is inserted by writing the TXLIN (0x0D) register, bit 2 to a 1. This sends the binary code 110 in bits 6, 7, and 8 of the K2 octet.

AIS—Line AIS occurs when three consecutive frames containing 111 in bits 6, 7, and 8 are detected in the K2 octet. It is removed when three consecutive frames of any other pattern are detected. Line AIS insertion can be enabled by writing the TXLIN (0x0D) register, Bit 3 to a 1. It is synchronized to frame boundaries. Line AIS sets all frame values except for the section overhead to 1s before scrambling.

2.4.3.6 Line RDI/AIS Detect

The Remote Defect Indication—Line (RDI-L) signal indicates to a Line Terminating Equipment (LTE) that the remote equipment is detecting a defect somewhere along the SONET line. Received bits 6–8 of the K2 octet are used to convey this information. If the incoming pattern is 110 for five consecutive frames, an RDI-L status is reported. An interrupt is generated when entering and exiting the RDI-L alarm state.

The Alarm Indication Signal—Line (AIS-L) is sent to alert the downstream LTE that a defect has been detected on the incoming SONET section. Received bits 6-8 of the K2 octet are also used to convey this information. If the incoming pattern is 111 for five consecutive frames, an AIS-L status is reported. An interrupt is generated when entering and exiting the AIS-L alarm state.

2.4.3.7 D4-12

See Section 2.6 (WAN only).

2.4.3.8 S1(WAN only)

Bits 5–8 of the Synchronization Status byte, S1, are used to convey the synchronization status of the network elements. Bits 1–4 are currently undefined. These status messages provide an indication of the quality of the synchronization source of the SONET signal. This allows the network elements to determine the best synchronization reference available and reconfigure their synchronization references autonomously without creating timing loops. The S1 byte can be read from RXS1 (0x16). It can be transmitted by writing to TXS1 (0x12).

The values of the S1 byte are described in Table 2-9.

Table 2-9. S1 Byte Description

Acronym	Description	Quality Level	Lower Nibble Bits 5,6,7,8
PRS	Stratum 1 Traceable	1	0001
STU	Sync - Traceability Unknown	2	0000
ST2	Stratum 2 Traceable	3	0111
ST3	Stratum 3 Traceable	4	1010
SMC	SONET Min Clock Traceable	5	1100
ST4	Stratum 4 Traceable	5	1100
DUS	Do not use for Sync	7	1111
RES	Reserved for Network Sync Use	-	1110

2.4.3.9 M1

The M1 byte handles automatic Line FEBE. It is used to inform the far end transmitting equipment that the receiving end is getting errors on the data blocks being sent to it. In practice, the receiver counts the block errors received in a frame (based on B2 bytes) and uses M1 to transmit the number of errors back to the sending equipment. An interrupt is generated when the received M1 octet indicates error counts other than 0.

2.4.4 Path Overhead

The Path Overhead checks for end-to-end communication integrity. The Section and Line Overhead must be terminated before the Path Overhead can be accessed. The transmit and receive functions of the Path Overhead are listed in Table 2-10.

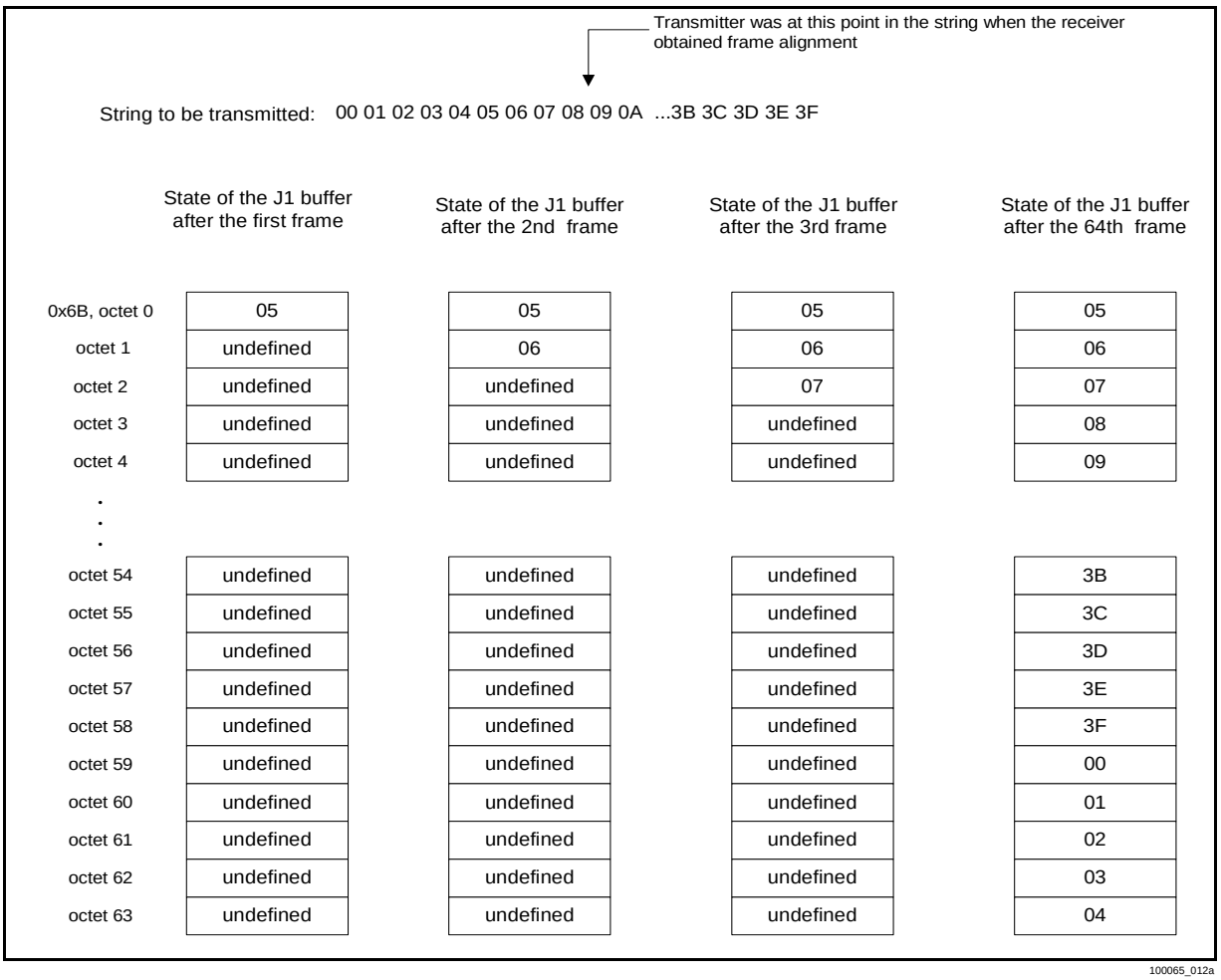
Table 2-10. Path Overhead Transmit and Receive Functions

Byte	Transmit	Receive
J1	00 hex or 64-byte trace buffer	Monitor Rx trace buffer, interrupt on change
B3	Calculated, error insertion	Checked, errors counted
C2	13 hex for ATM mapping	Checked for 01 or 13 hex
G1	Path FEBE, RDI inserted	Checked, errors counted, status

2.4.4.1 J1 The Path Trace byte, J1, is a circular 64-byte buffer that carries the Path Trace message, so a receiving Path Terminating Equipment (PTE) can verify continued connection to the transmitting PTE. This buffer overwrites when full. This message is user programmable but generally is an 8-bit ASCII CLLI™ code padded with ASCII NULL characters and terminated with CR and LF characters making up 64 bytes total. If Path Trace is enabled, the user is required to enter a message or the current contents of the transmit buffer will be transmitted. If J1 is disabled, then 64 zeros are transmitted. J1 can be disabled via register TXPTH (0x0E), bit 7. The J1 transmit buffer is located in register TXPTHBUF (0x69). The J1 receive buffer is RXPTHBUF (0x6B). If the incoming message differs from the data stored in the receive buffer from the previous message received, an interrupt appears in register PTHINT (0x3F) bit 1.

Figure 2-8 illustrates how the J1 buffer behaves during transmission and reception.

Figure 2-8. J1 Buffer Behavior



2.4.4.2 B3 The Path BIP-8 byte, B3, is allocated for path error monitoring. The path B3 byte is calculated over all bits of the previous STS SPE frame before scrambling, using bit-interleaved parity 8 code with even parity. As many as 64 k errors per second can be detected. B3 can be disabled by writing bit 6 in the TXPTH (0x0E) register to 1.

2.4.4.3 C2 The Path Signal label byte, C2, identifies the type of payload being received. The default code transmitted by the RS825x is 13 hex for ATM mapping. However, it can be changed to any other value in the TXC2 register (0x13). The receiver expects 01, 13, FC, or FF hex to be received as valid code words. The SONET block monitors the incoming C2 and generates one of two possible interrupts if 5 consecutive invalid values are received. If the received value is 00 hex, an Unequipped Path (Uneq-P) interrupt is generated in bit 2 in the PTHINT register (0x3F). If any other invalid value is received, a Payload Label Mismatch in Path (PLM-P) interrupt is generated in bit 3 in the PTHINT register.

2.4.4.4 G1 The Path Status byte, G1, is used to convey path terminating status and performance monitoring information back to an originating STS PTE. This feature permits the status and performance of the complete duplex path to be monitored at either end, at any point along that path. Bits 1–4 contain the Path Far End Bit Error (FEBE) count, which is the number of errors indicated by the B3 byte. The FEBE bits have nine valid values (0000–1000). A value greater than 8 is counted as having no errors. Bits 5–7 are a path RDI (yellow alarm) indication.

Bits 5–7 in the G1 byte are used for Path RDI (RDI-P) indications. The transmitter automatically generates RDI-P indications in these three bits if the AutoPthRDI control (bit 1 in TXPTH 0x0E) is set to a 1. Table 2-11 lists the values that are transmitted for various receiver alarm conditions. The user can override these values by setting AutoPthRDI to 0 and directly writing the desired value to be transmitted into TXPTH bits 3–1.

Table 2-11. Transmitted RDI-P Values

Receiver Defect	Transmitter G1 (bits 5-7)
None	000
PLM-P	010
AIS-P, LOP-P	101
UNEQ-P	110

The receiver observes the incoming G1 byte to monitor for RDI-P alarms. When 10 consecutive frames of the same value are received, the value is latched into RXG1 (0x19) so that it can be read. An interrupt is generated if the new value represents an alarm condition change. Interrupts are generated when entering and exiting alarm conditions. The EnhanceRDI control bit (ENPTH 0x37 bit 0) determines whether only bit 5 is observed (set to 0 to interwork with old equipment) or bits 5–7 are observed (set to 1 to conform to new equipment standards). Table 2-12 summarizes the receiver RDI-P interpretation.

Table 2-12. Receiver RDI-P Interpretation

Incoming RDI-P G1 bits 5-7	EnhanceRDI=0 Interpretation	EnhanceRDI=1 Interpretation
000	No remote defect	No remote defect
001	No remote defect	No remote defect
010	No remote defect	Remote payload defect
011	No remote defect	No remote defect
100	Remote defect	No remote defect
101	Remote defect	Remote server defect
110	Remote defect	Remote connectivity defect
111	Remote defect	No remote defect

2.4.5 SONET Frame Scrambler

Each SONET Network Element (NE) must have the capability to derive the clock timing from the incoming OC-3c signal. All transmitted OC-3c signals are timed from this clock. Therefore, it is important to maintain the 1s density in the data stream to ensure enough data transitions for robust clock recovery. The technique commonly used with modems, called scrambling and descrambling, is used in SONET to make the data appear to be more random.

This process uses a frame synchronous scrambler with a sequence length of 127, operating at the line rate. The generating polynomial is $1+x^6+x^7$. The scrambler is reset to 1111111 on the most-significant bit of the J1 byte. This bit and all the subsequent bits to be scrambled are added, modulo 2, to the output from the x^7 position of the scrambler. Everything but the first row of the section overhead is scrambled. This scrambling occurs just before the signal is passed to the PMD sublayer. Scrambling can be disabled by setting bit 7 in register TXSEC (0x0C). All 0s can be sent after scrambling for diagnostic purposes.

2.5 ATM Cell Processor

The RS825x ATM cell processor block is responsible for recovering cell alignment using the HEC octet, performing header error correction, and descrambling the payload octets. The resulting ATM cells are then passed to the ATM layer via the UTOPIA interface. Simultaneously, the ATM block is receiving data from the ATM layer, optionally calculating the HEC, formatting the 48-octet payload segments into 53-octet ATM cells, and sending the cells to the SONET block. If no data is being received from the ATM layer, the cell processor generates idle cells based on the data programmed into the associated registers.

The RS825x has all the counters necessary for capturing ATM error events and performs the payload CRC calculations as required by the AAL formats. It generates cell status bits, cell counts, and error counts.

2.5.1 ATM Cell Transmitter

The ATM cell transmitter controls the generation and formatting of 53-octet ATM cells that are sent to the Framer block. The ATM transmitter block formats an octet stream containing ATM data cells from the ATM layer device when such cells are available. All 53 octets of the data cells can be obtained from the external data source and formatted into the outgoing octet stream.

This block calculates the HEC octet in the outgoing cell from the header field. The calculated HEC octet can be inserted in place of the incoming data octet by writing DisHEC (bit 7) in the CGEN register (0x04) to a logic 0. For testing purposes, this HEC octet can be corrupted by XORing the calculated value with a specific error pattern input set in the ERRPAT register (0x07). This HEC error is achieved by writing InsHECErr (bit 1) in the ERRINS register (0x06) to a logic 1. The remaining 48-octet payload field of the outgoing cell is obtained from the external data source. The payload can be scrambled.

When no data is coming from the ATM layer, the RS825x inserts idle cells automatically in the outgoing data stream. The payload of these cells is read from the Transmit Idle Cell Payload Control register, IDLPAY (0x05). The 4-octet header field for these idle cells comes from the TXIDL1-4 registers (0x20-23). The HEC octet is calculated and inserted automatically. The payload field is filled with the octet contained in the IDLPAY register (0x05).

In normal operation, the 4-octet header field in the outgoing cell is passed on from the ATM layer device. Header patterns can be modified in the TXHDR1-4 registers (0x1C - 0x1F) and inserted into outgoing cells in place of header bytes received from the ATM layer. Bits 0-4 in the CGEN register (0x04) control whether the original header cells or the replacement cells are sent.

2.5.1.1 HEC Generation

In normal operation, the RS825x calculates the HEC for the 4 header bytes of each cell coming from the ATM layer. It then adds the HEC coset and inserts the result in octet 5 of the outgoing cell. HEC calculation can be disabled by setting bit 7 of CGEN (0x04) to a 1. When HEC is disabled, the RS825x leaves the contents of HEC field unchanged and transmits whatever data is placed in that field by the ATM layer.

The HEC coset (55 hex, by ATM standards) is used to maintain a value other than 0 in the HEC field. If the first 4 bytes in the header are 0, the HEC derived from these bytes is also 0. When this occurs and there are strings of 0s in the data, the receiver cannot determine cell boundaries. Therefore, it is recommended that the value 55 hex be added to the HEC before transmission. To enable the HEC coset on the transmit side, set bit 6 in register CGEN (0x04) to 1. To enable the receive HEC coset, set bit 4 in register CVAL (0x08) to 1.

2.5.2 ATM Cell Receiver

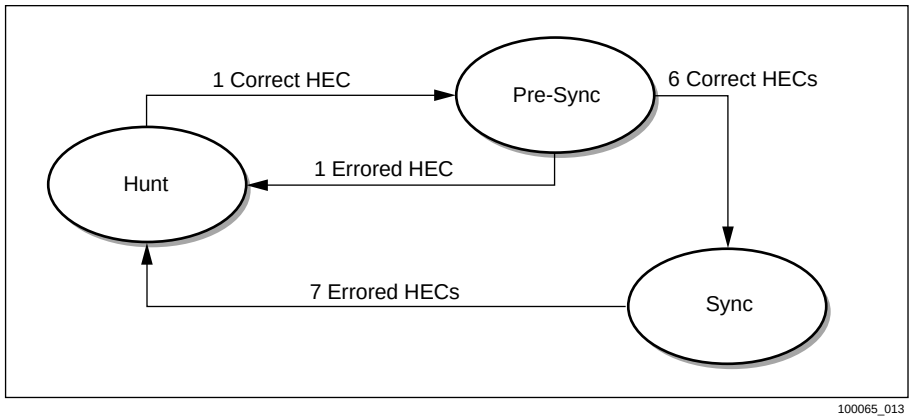
The ATM cell receiver performs cell delineation on incoming data cells by searching for the position of a valid HEC field within the cell. The HEC coset can be either active or inactive, which is determined in bit 4 in the CVAL (0x08) register.

2.5.2.1 Cell Delineation

The ATM block receives octets from the SONET block and recovers ATM cells by means of cell delineation. Cell delineation is achieved by framing ATM cell boundaries using HEC coding. Four consecutive bytes are chosen, and the HEC value is calculated. The result is compared with the value of the following byte. This “hunt” is continued by shifting this 4-byte window, one byte at a time, until the calculated HEC value equals the received HEC value. When this occurs, a pre-sync state is declared, and the next 48 bytes are assumed to be payload. The ATM block calculates HEC on the 4 bytes following this payload, assuming that a new cell has begun. If seven consecutive header blocks are found, synchronization is declared. If any HEC calculation fails in the pre-sync state, the process begins again (see Figure 2-9). Synchronization is held until seven consecutive incorrect HECs are received. At this time, the hunt state is reinitiated.

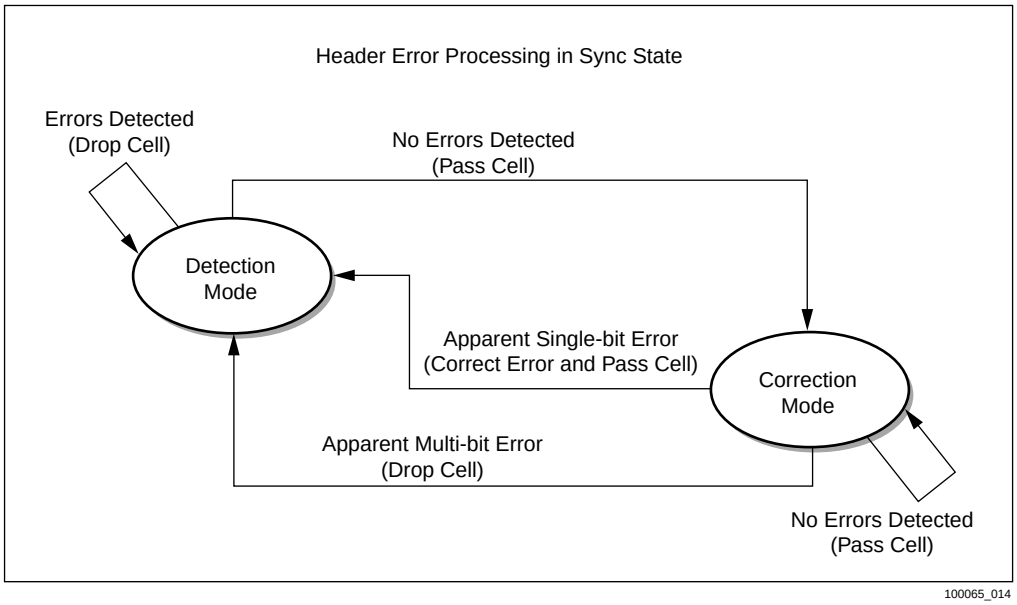
When LOCD occurs, an interrupt is generated and the RS825x automatically enters the hunt mode. However, the payload is still being scrambled by the far-end transmitter, leaving only the headers unscrambled. This means that the only repetitive byte patterns in the data stream that meet the cell delineation criteria are valid headers.

Figure 2-9. Cell Delineation Process



When in the sync state of cell delineation, cells are passed to the ATM block if the HEC is valid. If a single-bit error in the header is detected, the error is corrected, optionally, and the cell is passed to the ATM block. If HEC checking is enabled and HEC correcting is disabled (bit 3 in the CVAL register [0x08]), cells with single-bit HEC errors are discarded. If a multi-bit error is detected, the cell is dropped. Once either type of error is noted, all subsequent errored cells are dropped until a valid cell is received. This rule applies even for single-bit errors that could be corrected. Once a valid cell is detected, the process begins again. (See Figure 2-10.)

Figure 2-10. Header Error Check Process



2.5.2.2 Cell Screening

The RS825x provides two optional types of cell screening. The first type, idle cell rejection, prevents idle cells from being passed on. The second type, user traffic screening, compares the incoming bits to the values in the receive cell header registers. Cells are rejected or accepted based on the bit patterns of their headers.

Idle cell rejection is enabled in bit 6 of the CVAL register (0x08). If this bit is set to 1, all incoming cells that match the contents of the Receive Idle Cell Header Control registers, RXIDL1-4 (0x2C-2F), are rejected. Individual bits in the Receive Idle Cell Mask Control registers, IDLMSK1-4 (0x30-33), can be set to be treated as matching, regardless of their value. If idle cell rejection is disabled, cells pass directly to user traffic screening.

User traffic cell screening is similar to idle cell screening in that the incoming cells are compared to the Receive Cell Header Control registers, RXHDR1-4 (0x24-27). Individual bits in the Receive Cell Mask Control registers, RXMSK1-4 (0x28-2B), can be set to 1 or a don't care state, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their values. The RejHdr bit (bit 7) in the CVAL register (0x08) determines whether matching cells are rejected or accepted. If it is set to 0, matching cells are accepted. If set to 1, matching cells are rejected. See Table 2-13 and Table 2-14.

Table 2-13. Cell Screening - Matching

Receive Cell Mask Bit	Receive Cell Header Bit	Incoming Bit	Result
0	0	0	Match
0	0	1	Fail
0	1	0	Fail
0	1	1	Match
1	x	x	Match

Table 2-14. Cell Screening - Accept/Reject Cell

Cell	Reject Header	Result
Match	0	Accept Cell
Match	1	Reject Cell
Fail	0	Reject Cell
Fail	1	Accept Cell

2.5.3 Cell Payload Scrambler

The ATM standard requires cell payload scrambling in order to ensure that only valid headers are found in the cell delineation process. Scrambling randomizes any repeated patterns or other data strings that could be mistaken for valid headers.

Payload scrambling uses the polynomial $x^{43}+1$ to scramble the payload, leaving the 5 header bytes untouched. Payload scrambling is enabled by setting bit 5 in register CGEN (0x04).

Descrambling uses the same polynomial to recover the 48-byte cell payload. The descrambler polynomial is self-synchronizing. It can be enabled by writing bit 5 in register CVAL (0x08) to 1.

2.6 Data Link Interface (Wan Only Version)

The RS8250/4 provides access to two data link channels, D1—D3 and D4—D12, via the StatOut pins and the TxDL pin. Independent control is provided for receiving and/or transmitting data over each channel, as outlined in Table 2-15.

Table 2-15. LStatOut Configuration

StatSelect					StatOut[7]	StatOut[6]	StatOut[5]	StatOut[4]	StatOut[3]	StatOut[2]	StatOut[1]	StatOut[0]
EnPi Mode	**EnTxSec D1-D3**	**EnTxLin D4-D12**	**EnRxSec D1-D3**	**EnRxLin D4-D12**								
0	0	0	0	0	LOS	OOF	LOP	AIS-L	RDI-L	AIS-P	RDI-P	LOCD
1	0	0	0	0	OutStat[7]	OutStat[6]	OutStat[5]	OutStat[4]	OutStat[3]	OutStat[2]	OutStat[1]	OutStat[0]
x	x	x	1	x	Rx Clock Output	Rx Data Output	Rx Channel Indicator	Note 1	Note 1	Note 1	Note 2	Note 2
x	x	x	x	1	Rx Clock Output	Rx Data Output	Rx Channel Indicator	Note 1	Note 1	Note 1	Note 2	Note 2
x	1	x	x	x	Note 1	Note 1	Note 1	Tx Clock Output	Tx Channel Indicator	Tx Cell Sync	Note 2	Note 2
x	x	1	x	x	Note 1	Note 1	Note 1	Tx Clock Output	Tx Channel Indicator	Tx Cell Sync	Note 2	Note 2

NOTE(S):
(1) Any combination of the four Data Link control bits is allowed and overrides the StatPinMode bit for StatOut[7:2]. StatOut pins not being used for the Data Link operate as determined by StatPinMode.
(2) StatOut[1] and StatOut[0] are only controlled by StatPinMode and are unaffected by the Data Link control bits.

2.6.1 Data Link Transmit

The RS8250/4 can insert data into the D1–D12 octets of the outgoing data stream. This function is controlled by EnTxSecDL, bit 6 of the TXSEC, 0x0C register and EnTxLinDL, bit 4 of the TXLIN, 0x0D register. When EnTxSecDL is set to 1, serial data input on the DLTxData pin is inserted into the D1, D2, and D3 octets. Likewise, setting EnTxLinDL to 1 results in the serial data from the DLTxData pin being inserted in the D4 through D12 octets of the outgoing stream. The RS825x indicates that it is ready for D1, D2, and D3 octets by outputting a logic high on the statout[3] pin; it outputs a logic low when D4-D12 data is expected. If either EnTxSecDL or EnTxLinDL is set, the 0 the corresponding octets will be filled with 0x00.

StatOut [2], StatOut [3] and StatOut [4] are redefined whenever EnTxSecDL or EnTxLinDL are set.

StatOut [2]: This pin outputs a pulse at the beginning of every cell slot time, (both idle and data cells), synchronized to the UTOPIA transmit side. This is provided for SAR scheduling activities.

StatOut [3]: This becomes the transmit Data Link indicator, TxDLI, output. Serial data provided on DLTxData when this pin is high is transmitted in octets D1, D2, and D3. When this line is low, data from the DLTxData pin is inserted into octets D4 through D12.

StatOut [4]: The transmit clock for DL data is output on this pin.

2.6.2 Data Link Receive

Access to incoming octets D1–D12 is provided via the StatOut[5], StatOut[6], and StatOut[7] pins. This function is controlled by bits 0 and 1 of the RXLIN, 0x46, register as shown on page 4-47. When either of these bits is set high, the StatOut pins are defined as follows:

StatOut[5]: This becomes the Receive Data Link indicator, RxDLI, output. Incoming octets D1, D2, and D3 are output serially on StatOut[6] pin when this output is high. When this line is low, data from octets D4 through D12 are output serially on StatOut [6] pin.

StatOut [6]: This pin outputs the incoming data in a serial bit stream synchronized to the clock on StatOut[7].

StatOut [7]: This output is the serial data clock for incoming data and is synchronized with StatOut [6].

Refer to Section 5.1.6 for the Data Link timing.

2.7 UTOPIA Interface

The RS825x uses the ATM Forum's UTOPIA interface as its host interface to communicate with the ATM layer device. This interface is UTOPIA Level 2 compliant and UTOPIA Level 1 compatible. In brief, these two specifications are described as follows:

- UTOPIA Level 1: This is an 8- or 16-bit interface designed for data rates up to 200 Mbps. Both octet-level and cell-level handshaking are supported at a clock rate of 25 MHz. Octet-level handshaking requires the PHY to guarantee the acceptance of at least 4 bytes before it asserts the TxFull control line. In Cell level, it must guarantee the transfer of at least one entire 53-byte cell.
- UTOPIA Level 2: This interface provides all the features of Level 1 plus several enhancements. Level 2 defines multi-PHY functionality, allowing up to 31 PHYs to interface to one ATM layer device. A 33 MHz clock has been added to support the PCI bus. This interface uses either 8-bit or 16-bit wide data buses and cell-level handshaking. The 16-bit mode, which can run at 50 MHz, supports data rates up to 800 Mbps.

When using a single PHY, Conexant recommends using the 8-bit, Level 1 interface with cell handshaking unless the higher data rates are required. This reduces board size, layout complexity, and EMI with no performance impact at 155.52 Mbps.

2.7.1 UTOPIA Transmit and Receive FIFOs

The RS825x UTOPIA block has two sections, transmit and receive, each of which has a 4-cell FIFO buffer. ATM cell data is placed in the transmit FIFOs where it can then be passed to the SONET framing block. On the receive side of the UTOPIA interface, incoming cells are stripped of SONET overhead, converted to ATM formatted cells, and placed in the receive FIFO until sent out.

NOTE: By convention, data being transferred from the PHY to the ATM layer is labelled *received* data and data from the ATM layer to the PHY is called *transmitted* data.

2.7.2 UTOPIA 8-bit and 16-bit Bus Widths

The RS825x has two bus width options, 8-bit or 16-bit, which are selected in bit 3 of the UTOP1 register (0x0A). The protocols and timing are the same in both modes except that 8-bit mode uses only the lower half of the data bus (TxData[7:0] and RxData[7:0]).

In 8-bit mode, each ATM cell consists of 53 bytes (see Table 2-16). The first 5 bytes are used for header information. The remaining bytes are used for payload.

Table 2-16. Cell Format for 8-bit Mode

Bit 7 … Bit 0
Header 1
Header 2
Header 3
Header 4
UDF1 (HEC) (byte 5)
Payload 1
⋮
Payload 48

In 16-bit mode, the cells consists of 54 bytes (see Table 2-17). The first 5 bytes contain header information. The sixth byte, UDF2, is required to maintain alignment but is not read by the RS825x. The remaining bytes are used for payload.

Table 2-17. Cell Format for 16-bit Mode

Bit 15 … Bit 8	Bit7 … Bit 0
Header 1	Header 2
Header 3	Header 4
UDF1 (HEC) (byte 5)	UDF2 (0) (byte 6)
Payload 1	Payload 2
⋮	⋮
Payload 47	Payload 48

NOTE: Normally, the HEC is calculated by the PHY and put in byte 5, UDF1. However, setting bit 7 of the CGEN register (0x04) to 1 disables HEC calculation. In this case, data inserted by the ATM layer into byte 5 is transmitted by the PHY.

2.7.3 UTOPIA Parity

The RS825x supports even and odd parity, which is controlled by bit 2 of the UTOP1 register (0x0A). The parity on received data is calculated for either 8 bits or 16 bits, according to the selected bus width in bit 3 of the UTOP1 register (0x0A). The result is output on URxPrty (pin 119).

Likewise, the parity on transmitted data is calculated for either 8 bits or 16 bits, according to the selected bus width. The calculated result should match the bit present on UTxPrty (pin 88). If it does not match, a parity error has occurred. This error can be observed either in the ParErr bit (bit 7) in the TXCELL register (0x48) or in the ParErrInt bit (bit 7) in the TXCELLINT register (0x40). Systems that do not use parity should disable the generation of interrupts caused by parity errors by writing bit 7 of the ENCELLT register (0x38) to 0.

2.7.4 UTOPIA Multi-PHY Operation

The RS825x supports multi-PHY operation as described in the UTOPIA Level specification (af-phy-0039.000; visit the web site: http://www.atmforum.com). Three primary functions are involved in this operation: polling, selection, and data transfer. These functions are basically the same for both the transmit and receive sides of the UTOPIA bus. The following example describes the transmit functions.

The ATM layer UTOPIA controller polls the connected PHY ports by transmitting the port addresses on the UTxAddr lines. If a port is ready to transfer data, it asserts UTxClAv. The controller determines which port is to transfer data and selects that port by transmitting its address. The controller then asserts UTxEnb* to allow the PHY to transfer data on the UTxData lines. UTxEnb* is deasserted when the transfer is completed. Polling can continue during the data transfer process but not during port selection. It operates independently of the state of UTxEnb*.

To pause the data transfer process, UTxEnb* can be deasserted. To continue the transfer, the controller must reselect the port by transmitting its address one clock cycle before asserting UTxEnb*. The controller must ensure that the cell transfer from this port has been completed, to avoid a start-of-cell error.

The RS825x has a UTOPIA receiver output disable feature which allows the user to set up redundant or back-up PHYs with the same UTOPIA address on the same UTOPIA bus. In this setup, both PHYs' transmitters are enabled, sending out identical data streams. Both PHYs' receivers are enabled, but only one is transferring data to the ATM device. The receiver output is disabled in the backup PHY by writing the UtopDis, bit 5, in the UTOP2 register (0x0B) to a logic 1. This disable places five of the backup PHY's signals; URxData, URxPrty, URxSOC, URxClAv, and UTxClAv; in a high-impedance state, preventing data and control signals from being passed to the ATM layer device. The disabled receiver flushes its FIFOs at the same rate as the enabled one, but all data it has received, except the last four cells, is lost. Should the primary PHY device encounter an unacceptable error rate, software can quickly enable the backup PHY and disable the primary PHY, reducing cell loss in the transition.

NOTE: To facilitate multi-PHY operation, the RS8254/5 assigns a different address to each of its ports by default.

2.7.5 Handshaking

The RS825x provides both cell-level and octet-level handshaking on its UTOPIA interface (only cell-level is used in Level 2). The primary distinction between these two levels is the amount of data that is sent or received. Octet-level sends and receives four octets at a time, while cell-level sends and receives a full cell at a time, depending on FIFO size and availability. In octet-level handshaking, UTxClAv is an active low, FIFO full indicator. In cell-level, it is an active high, cell buffer available indicator. These two options are selectable in the Handshake bit, bit 4, of the UTOP1 register (0x0A).

2.8 Microprocessor Interface

The microprocessor interface transfers control and status information in 8-bit data transfers between the external microprocessor and RS825x by means of write and/or read access to internal registers. This interface allows the microprocessor to configure the RS825x by writing various control registers. These control registers can also be read for configuration confirmation. This interface also provides the ability to read the device's current condition via its status registers and counters. Summary status is available for rapid interrupt identification.

The microprocessor interface has two primary modes of operation: an asynchronous, SRAM-like interface and a synchronous interface. The MSyncMode pin (pin 31) determines which mode is active.

For the asynchronous interface, the microprocessor interface pins are defined as follows: MAcsSel, MCs*, MRd*, MWr*, MInt*, MAddr, MData. In this mode, the MRd* and MWr* strobes direct the data transfers. The asynchronous interface has two secondary operating modes: a high-performance access mode and a low-power access mode. The MAcsSel pin (pin 30) determines which access mode is active. These modes allow for trade-offs between speed and power required for various applications.

For the synchronous interface, the microprocessor interface pins are defined as follows: MClk, MCs*, MW/R*, MAs*, MInt*, MAddr, MData. In this mode, the timing of these signals is synchronized to MClk, which is intended to be directly driven by the external microprocessor. The synchronous interface is compatible with the Bt8230 and Bt8233 SAR devices, providing no-wait-state operation.

2.8.1 Status and Control

Several registers provide status and control information to the microprocessor. Status information includes interrupts, counters, and generic functional status. Control information includes configuration and real-time control, according to the specific function of each control register. There are two types of status input: live and latched. Live status provides the current status of the device. Latched status is used for rapidly changing states to capture information until it can be read.

This device contains general purpose status and control functions, such as a master reset, output status, and device part number and revision. The software-controlled Master Reset, GEN register (0x00) bit 0, restarts all device functions and sets the control and status registers to their default values. The OUTSTAT register (0x02) provides a means for controlling external devices via the OutStat pins (1-5 and 126-128). It is enabled by setting the StatPinMode (bit 2) of the GEN register (0x00). The VER register (0x03) uniquely identifies the device and revision level.

2.8.2 Counters

The RS825x counters record events within the device. There are two types of events: error events, such as Section BIP errors, and transmission events, such as transmitted ATM cells.

Counters which are comprised of more than one register must be accessed by reading the least significant byte first. This guarantees that the value contained in each component register accurately reflects the composite counter value at the time the least significant byte was read since the counter may be updated while the component registers are being read.

Each counter is large enough to accommodate the maximum number of events that may occur within a one-second interval. The counters are cleared after being read. Therefore, if the counters are read every second, the application receives an accurate recording of all event occurrences.

2.8.3 One-second Latching

Conexant's implementation of one-second latching ensures the integrity of the statistics being gathered by the network management software. Internal statistics counters can be latched at one-second intervals, which are synchronized to the OneSecIn pin (pin 33). Therefore, the data read from the statistic counters represents the same "one second" of real-time data, independent of network management software timing.

The RS825x implements one-second latching for both status signals and counter values. When the EnStatLat bit (5) in the GEN register (0x00) is written to a logic 1, a read from any of the status registers returns the state of the device at the time of the previous OneSecIn pin (pin 33) assertion. When the EnCntrLat bit (4) in the GEN register (0x00) is written to a logic 1, a read from any of the counters returns the state of the device at the time of the previous OneSecIn pin (pin 33) assertion. Thus the counters are updated once per second.

The OneSecIn pin is intended to be asserted at one-second intervals. This can be achieved by connecting the OneSecIn pin to the OneSecOut pin (pin 34). The OneSecOut signal is derived from the 8kHzIn pin (pin 37). This signal is asserted for one 8kHzIn clock period, every 8,000 8kHzIn periods. If 8kHzIn is being driven by an 8 kHz clock, the OneSecOut signal is asserted every second.

NOTE: When latching is disabled and a counter is wider than one byte, the LSB should be read first which retains the values of the other bytes for a subsequent read.

2.8.4 Interrupts

The RS825x's interrupt indications can be classified as either single-event or dual-event. A single-event interrupt is triggered by a status assertion. A dual-event interrupt is triggered by either a status assertion or deassertion. Both types of interrupts are further described in the following examples.

Single-event interrupt: When a parity error occurs on the UTOPIA transmit data bus, an interrupt is generated on ParErrInt, bit 7 in the TXCELLINT register (0x40). This bit is cleared when read.

Dual-event interrupt: When LOCD occurs, LOCDInt, bit 7 of the corresponding RXCELLINT register (0x41) is set to 1. This bit is cleared when the register is read. Once cell delineation is recovered, bit 7 is set to 1 again, generating another interrupt.

All interrupt bits have a corresponding enable bit. This allows software to disable or mask interrupts as required.

2.8.4.1 Interrupt Routing

The RS825x uses two levels of interrupt indications. The first level consists of section, line, path, APS, receive, and transmit interrupt indications. The second level summarizes first-level interrupts and indicates one-second interrupts.

The first level interrupt indications are located in registers SECINT, LININT, PTHINT, APSINT, TXCELLINT, and RXCELLINT. Each interrupt bit in these registers can be disabled in the corresponding ENSEC, ENLIN, ENPTH, ENAPS, ENCELLT, or ENCELLR registers, respectively. The result is then ORed into the appropriate bit in the SUMINT register.

The second level consists of summary interrupt indications, located in the SUMINT register. It also includes the OneSecInt indications. Each interrupt bit in these registers can be disabled in the corresponding ENSUMINT register. The result is ORed to the MInt* pin (pin 6). The MInt* pin can be enabled or disabled by setting the EnIntPin (bit 6) in the GEN register (0x00).

Figure 2-11 is a flow chart of the interrupt generation process.

Figure 2-11. Interrupt Indication Flow Chart

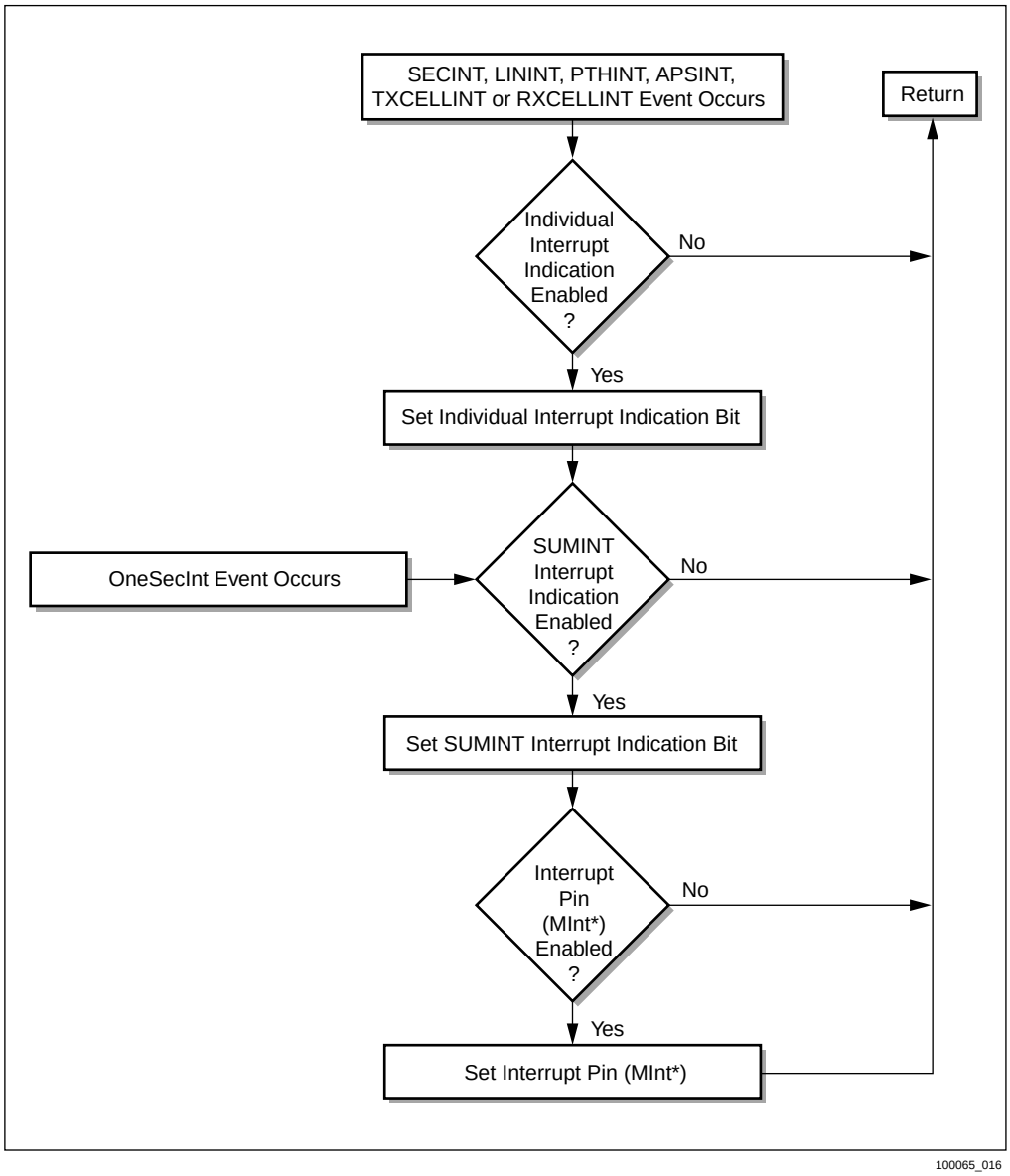
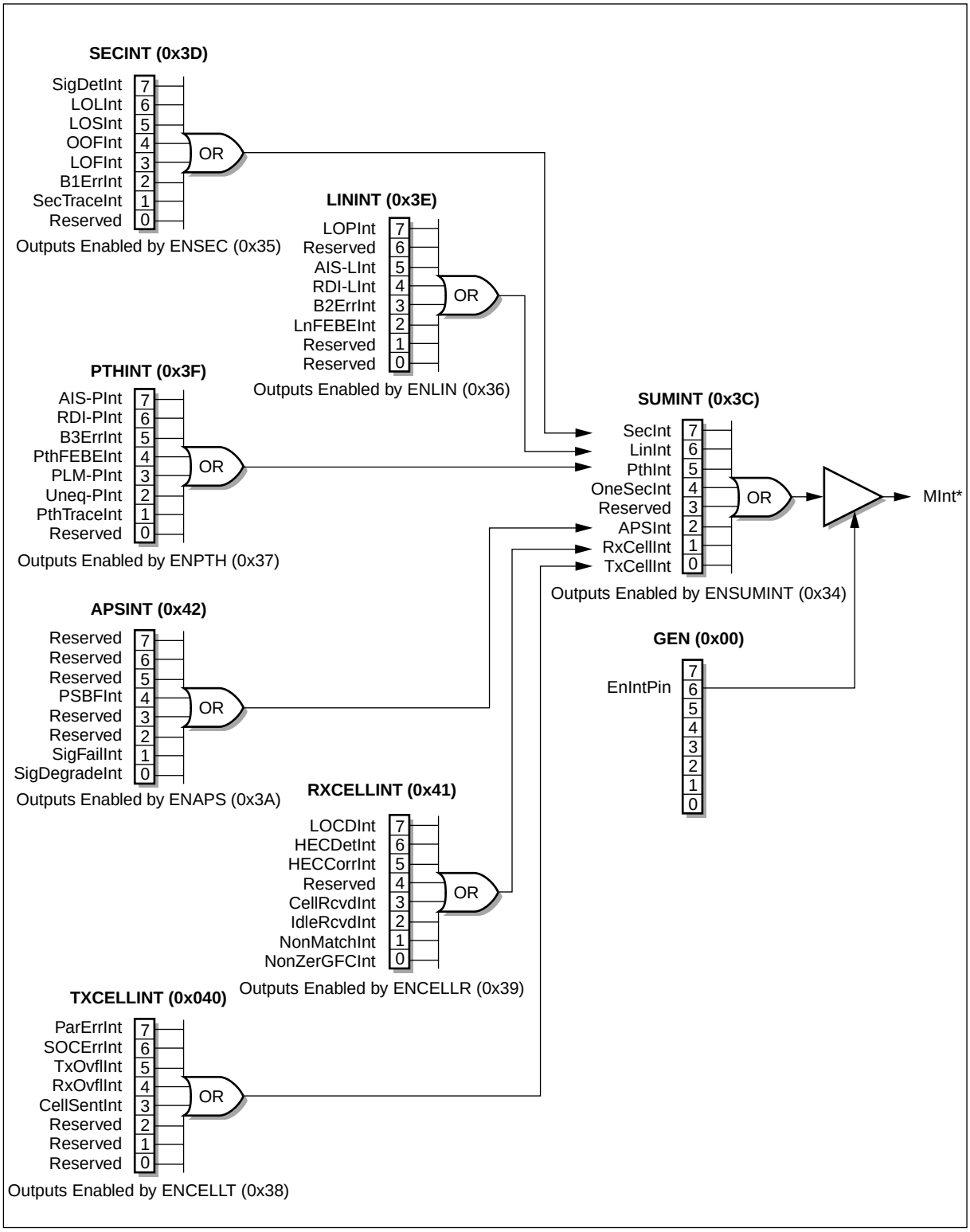


Figure 2-12 shows the registers involved in the interrupt generation process.

Figure 2-12. Interrupt Indication Diagram



2.8.4.2 Interrupt Servicing

When an interrupt occurs on the MInt* pin (pin 6), it could have been generated by any of 35 events. The RS825x's interrupt indication process ensures that a maximum of two register reads are necessary to determine the source of an interrupt. The interrupt is traced back to its source using the following steps:

1. Read the SUMINT register to see which bit(s) shows an interrupt.
   - Bit 0, TxCellInt, reflects activity in the TXCELLINT register.
   - Bit 1, RxCellInt, reflects activity in the RXCELLINT register.
   - Bit 2, APSInt, reflects activity in the APSINT register.
   - Bit 3 is reserved.
   - Bit 4, OneSecInt, indicates a one-second interrupt.
   - Bit 5, PthInt, reflects activity in the PTHINT register.
   - Bit 6, LinInt, reflects activity in the LININT register.
   - Bit 7, SecInt, reflects activity in the SECINT register.
2. If necessary, read the appropriate TXCELLINT, RXCELLINT, APSINT, PTHINT, LININT, or SECINT register.

All Level 1 bits are cleared when the register is read. Once the register is read, ALL bits in that register are reset to their default values. Therefore, interrupt service routines must be designed to handle multiple interrupts in the same registers. In Level 2, OneSecInt is cleared when the register is read. However, the summary bits are cleared only when the corresponding Level 1 register is read and cleared.

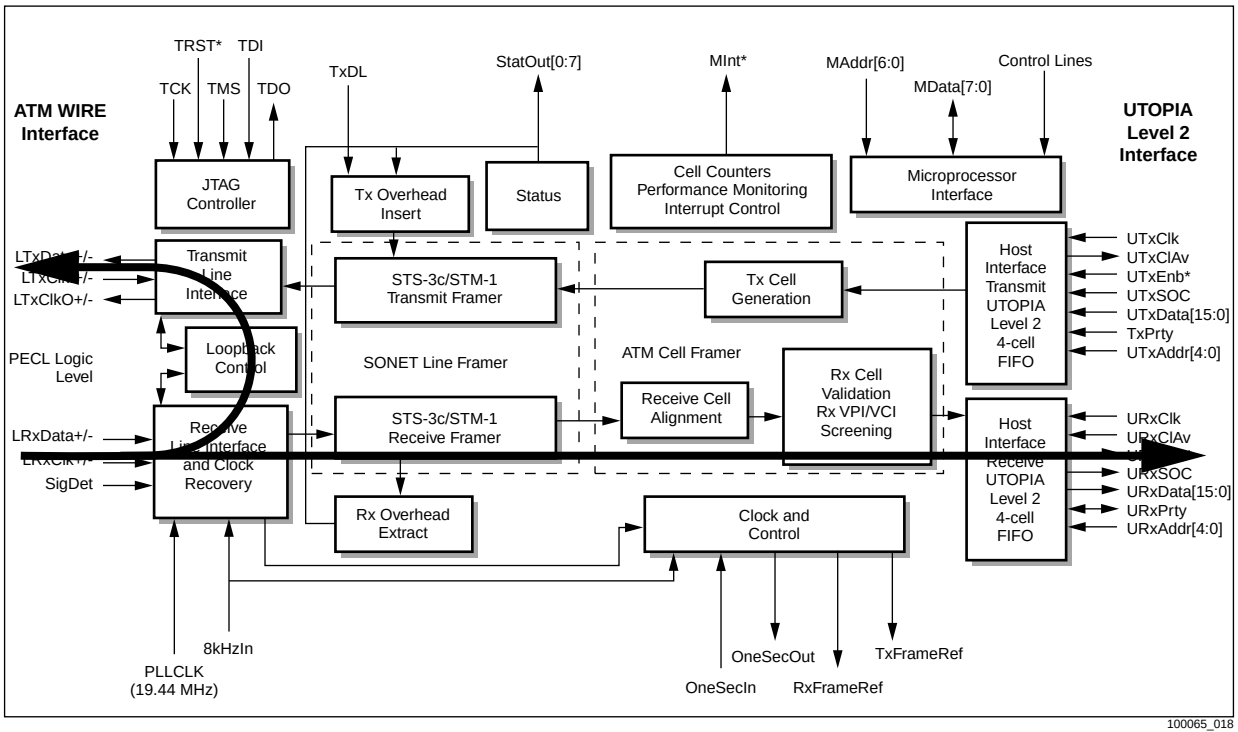
2.9 Loopback Modes

Loopbacks are diagnostic tools that verify the data path. The RS825x has three loopback modes: Line Loopback and UTOPIA Loopback, which check the line between a remote device and the PHY, and Source Loopback, which checks that the host (the ATM layer) is communicating with the PHY. Line Loopback is illustrated in Figure 2-13, and UTOPIA Loopback is illustrated in Figure 2-14. Figure 2-15 illustrates Source Loopback.

2.9.1 Line Loopback

Line loopback is enabled or disabled in bit 1 of the CLKREC register (0x01). When Line Loopback is enabled, all incoming data on the Receive Line Interface is retransmitted out the Transmit Line Interface. The received data is also passed through the PHY's normal path to be output on the UTOPIA interface.

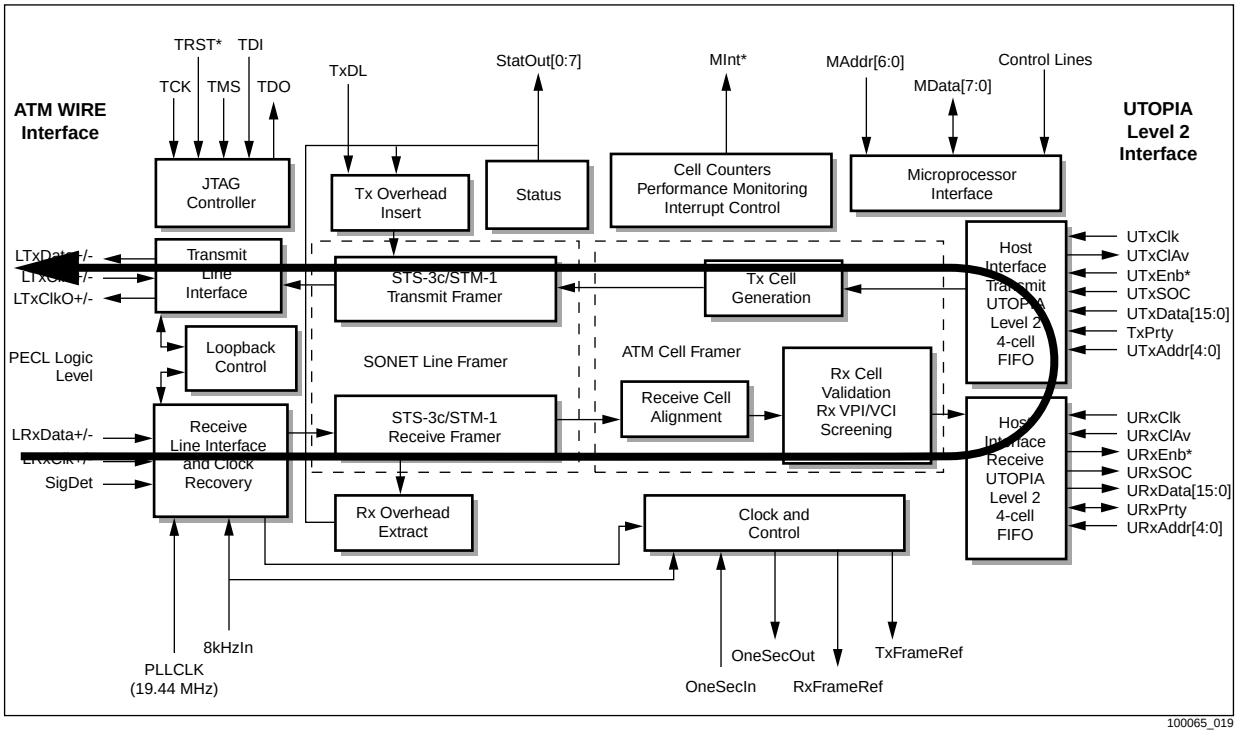
Figure 2-13. Near-end Line Loopback Diagram



2.9.2 UTOPIA Loopback

UTOPIA loopback is enabled or disabled in bit 0 of the CLKREC register (0x01). When UTOPIA loopback is enabled, all received cells in the UTOPIA FIFO are passed to the transmit FIFO for transmission on the Transmit Line Interface. The receive UTOPIA bus is placed in a high-impedance state.

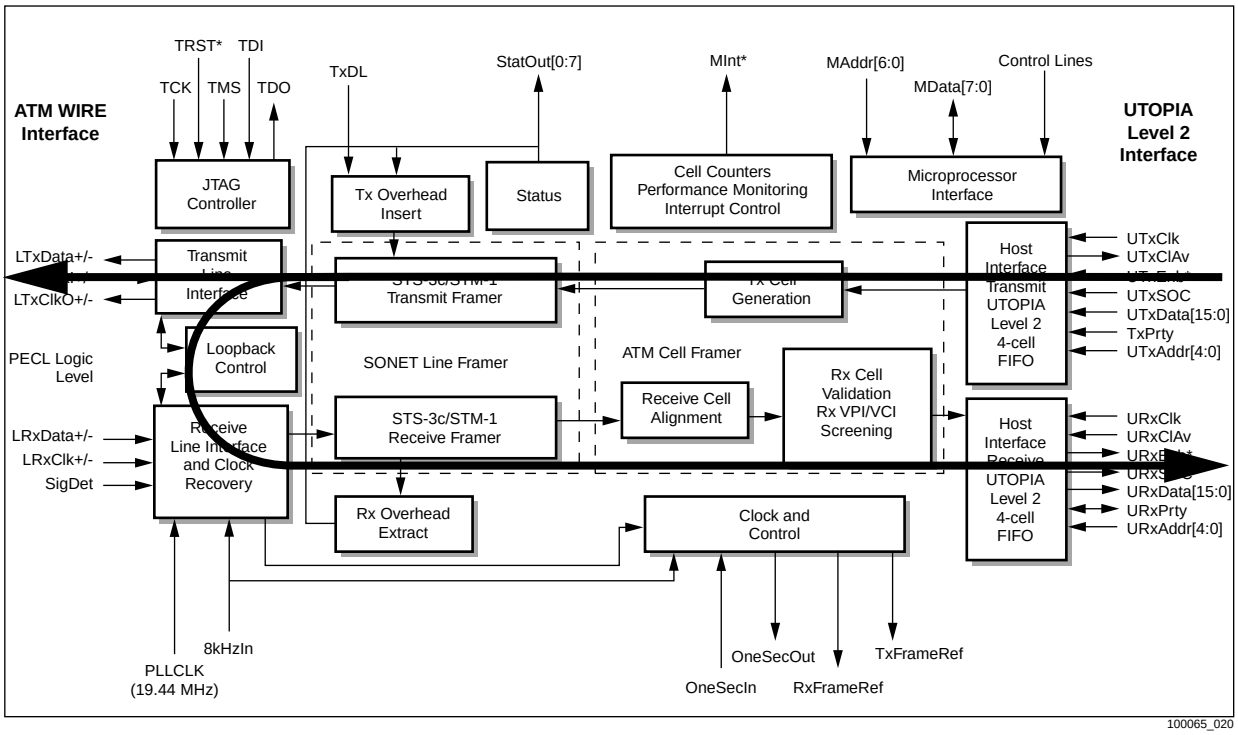
Figure 2-14. UTOPIA Loopback Diagram



2.9.3 Source Loopback

Source loopback is enabled and disabled in bit 2 the CLKREC register (0x01). When source loopback is enabled, all data transmitted by the RS825x is also looped back through the Receive Line Interface. Data from the PMD is ignored.

Figure 2-15. Source Loopback Diagram



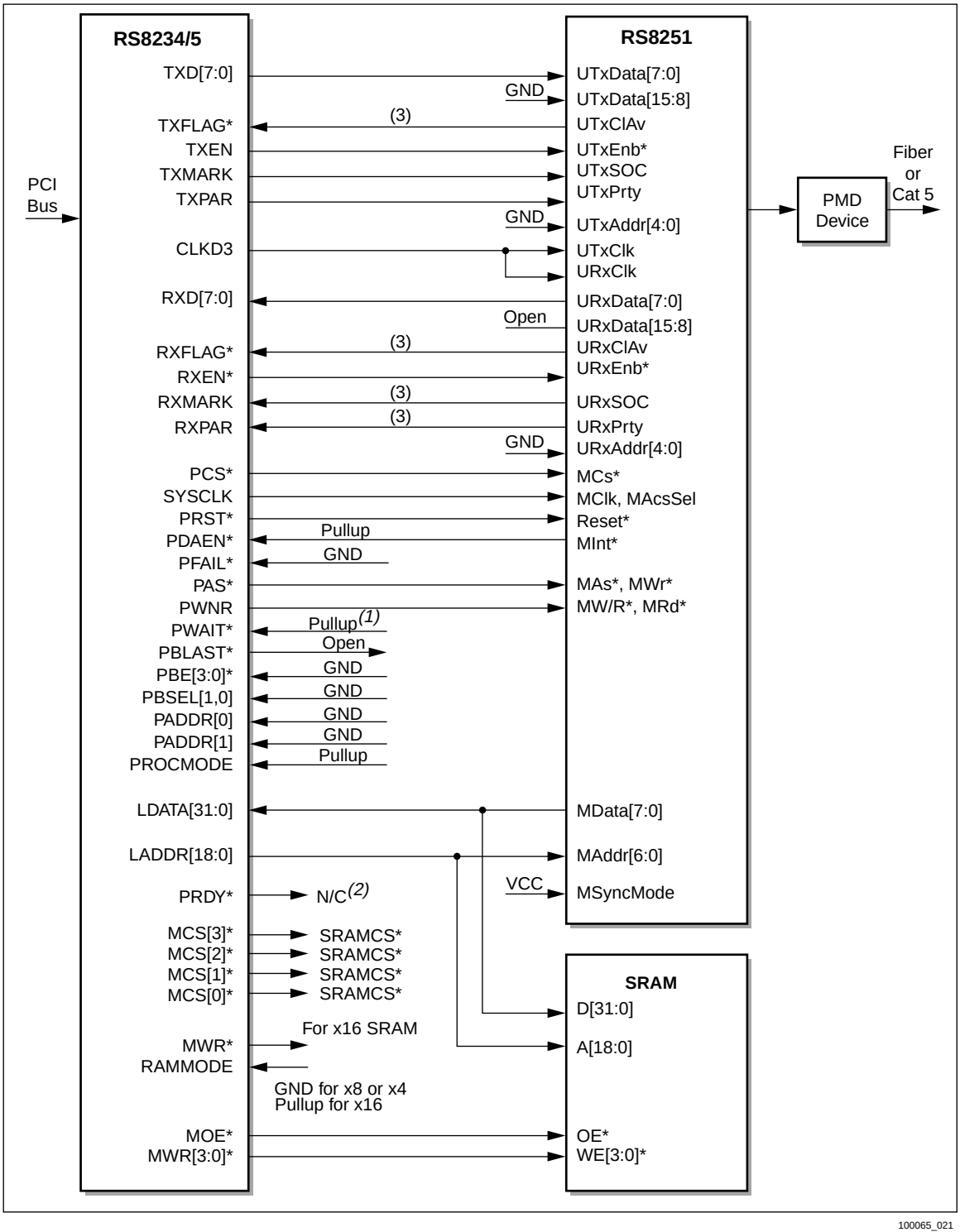
3.0 Applications

This chapter provides application examples for the RS825x. A system application shows the RS8251 connected in a NIC application using Conexant's RS8235 SAR and a Cat 5 PMD. All board layouts, schematics, and the parts list are available from Conexant. Sample source code for the PHY and SAR can be obtained from Conexant. Only minor customization, verification, and compliance testing need to be completed by the OEM prior to production.

3.1 System Application

Figure 3-1 illustrates how the RS8251 is connected to a Conexant RS8234 or RS8235 SAR.

Figure 3-1. RS8251 and SAR (RS8234/5) Application Diagram



NOTE(S):

(1) Can be driven by external circuitry to extend cycles.

(2) Can be used by external circuitry.

(3) A pulldown resistor is required on UTxClav, URxClav, URxSOC, and URXPrty to ensure correct startup of the RS8234 UTOPIA interface.

3.2 PECL Applications

This section provides application examples for the PECL interface.

3.2.1 RS825x to 3.3 V PMD

When using the RS825x with a 3.3 V PMD, ensure that the lines are properly terminated. The recommended scheme is illustrated in Figure 3-2. Resistors R_1 and R_2 must satisfy two equations.

First, since the Vcc supply and ground both provide a path for the high frequency current, resistors R_1 and R_2 are treated as if they were in parallel, ignoring the extremely high impedance of the PECL input.

$$Z_0 = \frac{R_1 \times R_2}{(R_1 + R_2)}$$

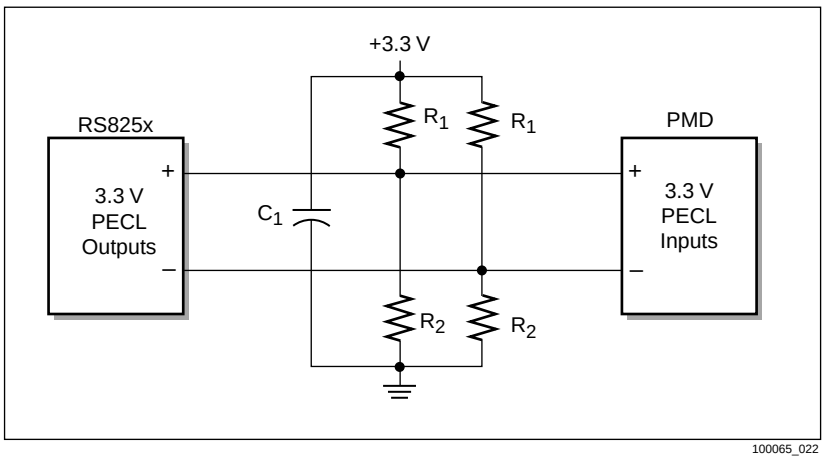
where: Z_0 is the characteristic impedance of the circuit board trace. This matching network should be as close to the destination as possible. An overview of circuit board trace impedance is given in Section 3.2.4.

Second, R_1 and R_2 form a voltage divider network that establishes the low-level voltage.

$$V_{il} = \frac{V_{cc} \times R_2}{(R_1 + R_2)}$$

For example: if Z_0 = 50 Ω, V_{il} = 1.65 V, and V_{cc} = 3.3 V
then R_1 = 100 Ω and R_2 = 100 Ω.

Figure 3-2. RS825x to 3.3 V PMD Diagram



NOTE(S): C_1 = 220 pF RF grade capacitor

3.2.2 RS825x to 5 V PMD Inputs

When connecting the RS825x 3.3 V PECL outputs to 5 V PECL inputs, ensure that the lines are properly terminated. In addition, the input voltage levels must be shifted. Both can be accomplished by the circuit in Figure 3-3.

The termination impedance is given by:

$$Z_0 = \frac{(R_3 + R_4) \times R_5}{(R_3 + R_4 + R_5)}$$

The outputs of the RS825x need to be biased near V_{ref} (2.0 V). Therefore:

$$V_{ref} = \frac{V_{cc} \times R_5}{(R_3 + R_4 + R_5)}$$

Furthermore, V_{ih} and V_{il} going to the PMD are given by:

$$V_{ih} = \frac{(V_{cc} - V_{oh}) \times R_4}{(R_3 + R_4)} + V_{oh}$$

where: V_{oh} is the high level output from the RS825x and:

$$V_{il} = \frac{(R_3 + R_4) \times V_{cc}}{(R_3 + R_4 + R_5)}$$

Using the values:

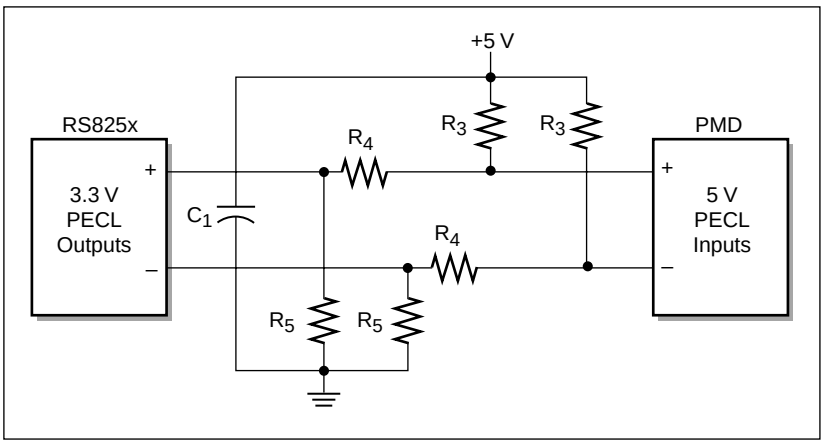
R_3 = 75 Ω
R_4 = 52 Ω
R_5 = 82.5 Ω
V_{oh} = 2.5 V

results in:

V_{ref} = 1.968 V
V_{ih} = 3.52 V
V_{il} = 3.03 V

These values are well within the desired ranges and provide adequate voltage differential for the PMD.

Figure 3-3. RS825x to 5 V PMD Inputs Diagram



3.2.3 RS825x to 5 V PMD Outputs

The recommended termination and level shifting circuit for connecting 5.0 V PECL outputs to the RS825x 3.3 V PECL inputs is illustrated in Figure 3-4. The line termination impedance is demonstrated in the following equation:

$$Z_0 = \frac{(R_7 + R_8) \times R_6}{(R_6 + R_7 + R_8)}$$

The outputs of the 5 V PECL should be biased at around V_{ref}, which is generally V_{cc}-2.0. Therefore:

$$3.0V = \frac{(R_7 + R_8) \times V_{cc}}{(R_6 + R_7 + R_8)}$$

If you select:

R_6 = 82.5 Ω
R_7 = 56 Ω
R_8 = 75 Ω
Z_0 = 50 Ω

Then the low level input voltage, V_{il}, going to the RS825x is:

$$V_{il} = \frac{5.0 \times R_8}{(R_6 + R_7 + R_8)} = 1.76V$$

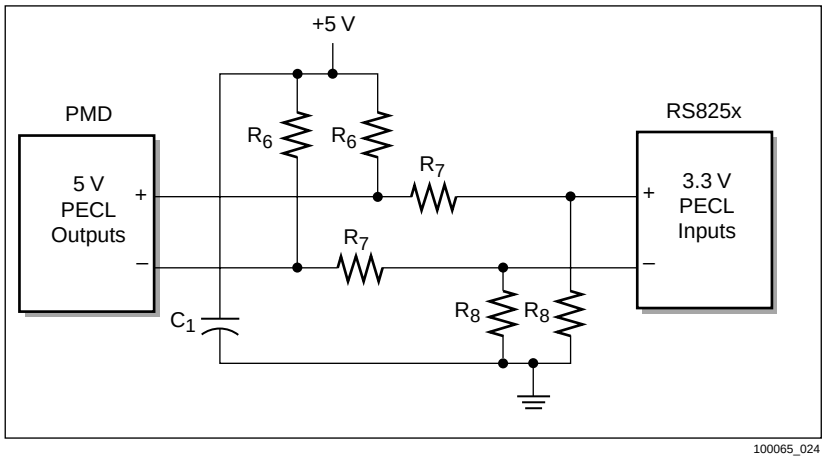
This is well below the maximum of V_{ref}-0.06 V.

Given that the V_{oh} for 5 V PECL is around V_{cc}-1.3 V, then V_{ih} for the RS825x is:

$$V_{ih} = \frac{3.7 \times R_8}{(R_7 + R_8)} = 2.1V$$

Not only is this above the minimum (V_{ref}+0.06), but it provides a differential of 340 mV.

Figure 3-4. RS825x to 5 V PMD Outputs Diagram



3.2.4 PECL Layout

All PECL traces must be treated as transmission lines. Therefore, standard high-speed practices must be followed:

- Keep traces as short as reasonable.
- Do not allow traces to cross discontinuities in the ground/power planes.
- Use separate Power and Ground planes.
- Terminate all inputs and outputs as described above.
- Place the terminating resistors as close to the destination IC as possible.
- Do not route signal traces through the board through vias.
- Check that each IC has two high-quality RF bypass capacitors that are at least an order of magnitude apart; e.g., 200 pF and 0.1 µF.
- Avoid 90 degree turns in trace routing.
- Ensure that the trace width results in a line impedance that matches the input impedance of the load. Trace width can be found from the formula below:

$$w = \left(7.745 \times h \times e^{-\left[\frac{\sqrt{e_r + 1.41} \times Z_0}{87} \right]} \right) - \frac{t}{0.8}$$

where: w = trace width

Z_0 = characteristic line impedance

h = board thickness (not including copper layers)

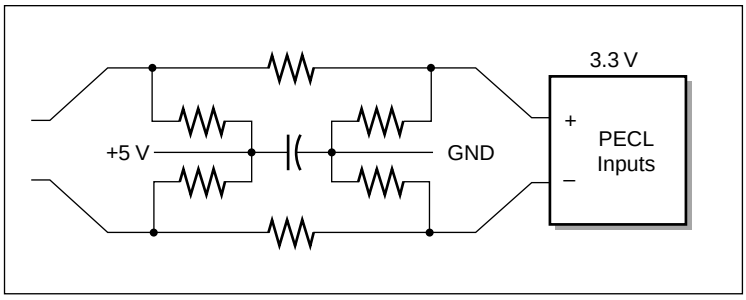
t = thickness of copper layers

e_r = relative dielectric constant of the board

Using the generic values Z_0 = 50 Ω, h = 0.060, t = 0.0015 and e_r = 4.8 results in a width (w) of 0.11 inches.

The ideal PECL Layout is illustrated in Figure 3-5.

Figure 3-5. PECL Layout Diagram (3.3 V Inputs)



3.2.5 The RS825x/RS8235 Network Interface Card Reference Design

The following schematic shows a single-port RS8251 implementing the ATM forum standard for 155 Mbps over Cat 5 twisted pair in a network interface card, NIC, with the Conexant RS8235 SAR. This design was developed as a low cost, ATM-to-the-desktop example. Board layout details, including Gerber files, are available free of charge from Conexant (contact your sales representative). While this design is fully functional, no guarantee regarding suitability for manufacture is implied.

The RS8235 Segmentation and Reassembly device integrates ATM terminal functions, PCI Bus Master and Slave controllers, and a UTOPIA interface with service-specific functions in a single package. The RS8235 generates and terminates ATM traffic and automatically schedules cells for transmission. The RS8235 is targeted at cost-sensitive 155 Mbps throughput systems where the performance of the overall system is critical but the number of VCCs is not large. The SAR defaults to UTOPIA Level 2 mode, so if Level 1 is desired, it must be reset to that mode before operation.

The major design considerations of this application are the following:

- StatOut Indicators: In this design only the LOCD output line, StatOut[0] (pin 5), has a status LED. LEDs can be connected to other StatOut pins to provide additional system status. Two lines, StatOut[6] and StatOut[7], are used to control the PMD. Because of this, StatPinMode, bit 2 of the GEN register (0x00), must be written to a logic 1. This places the output pins under software control. Software must read the appropriate pins and set them in the OutStat register (0x02).
- UTOPIA: URxClav and URxSOC have pulldown resistors to prevent problems during boot-up and before software has a chance to reprogram the SAR to UTOPIA level 1. Since this is not a multi-PHY design, the UTOPIA address lines are tied low to match the default port address of the RS825x.
- 3.3 V regulator: This regulator was included to support legacy motherboards without 3.3 V on the PCI connector. It can be omitted for designs that are to be used only in systems with 3.3 V on the PCI connector.
- ML6674CH UTP Transceiver: The Micro Linear ATM 155 Mbps UTP Transceiver is also known as a PMD. This device accepts data in NRZ format from the PECL interface and outputs it on the line using a current loop transmitter. Likewise, incoming data is converted to NRZ format at the appropriate PECL levels. In addition, the transceiver corrects baseline wander and performs adaptive equalization. In this application, the TXOFF* and LPBK* inputs of the ML6674 are under software control through the StatOut pins of the PHY.
- PE-68508: These transformers provide isolation between the PMD and the physical wire of the network.

4.0 Registers

The RS825x registers are used to control and observe the device's operations. A list of these control and status registers, buffers, and counters is presented in Table 4-1. All registers are 8 bits wide. All control registers can be read to verify contents.

NOTE: Control bits that do not have a defined function are reserved and must be written to zero.

NOTE: Some of these registers are active only in the WAN devices, and are labelled as (**WAN)** under the register name.

Table 4-1. Control and Status Registers *(1 of 5)*

Address	Name	Type	OneSec Latching	Description	Page Number
0x00	GEN	R/W	—	General Control Register	page 4-7
0x01	CLKREC	R/W	—	Clock Recovery Control Register	page 4-6
0x02	OUTSTAT	R/W	—	Output Pin Control Register	page 4-8
0x03	VERSION	R	—	Part Number/Version Status Register	page 4-8
0x04	CGEN	R/W	—	Cell Generation Control Register	page 4-9
0x05	IDLPAY	R/W	—	Transmit Idle Cell Payload Control Register	page 4-10
0x06	ERRINS	R/W(1)	—	Error Insertion Control Register	page 4-26
0x07	ERRPAT	R/W	—	Error Pattern Control Register	page 4-27
0x08	CVAL	R/W	—	Cell Validation Control Register	page 4-15
0x09	APSTHRESH (WAN)	R/W	—	APS Threshold Control Register	page 4-33
0x0A	UTOP1	R/W	—	UTOPIA Control Register 1	page 4-24
0x0B	UTOP2	R/W	—	UTOPIA Control Register 2	page 4-25
0x0C	TXSEC	R/W	—	Transmit Section Overhead Control Register	page 4-31
0x0D	TXLIN	R/W	—	Transmit Line Overhead Control Register	page 4-29
0x0E	TXPTH	R/W	—	Transmit Path Overhead Control Register	page 4-30
0x0F	—	—	—	Unused	—

Table 4-1. Control and Status Registers *(2 of 5)*

Address	Name	Type	OneSec Latching	Description	Page Number
0x10	TXK1 (WAN)	R/W	—	Transmit K1 Overhead Control Register	page 4-28
0x11	TXK2 (WAN)	R/W	—	Transmit K2 Overhead Control Register	page 4-28
0x12	TXS1 (WAN)	R/W	—	Transmit S1 Overhead Status Register	page 4-31
0x13	TXC2	R/W	—	Transmit C2 Overhead Control Register	page 4-27
0x14	RXK1	R	—	Receive K1 Overhead Status Register	page 4-35
0x15	RXK2	R	—	Receive K2 Overhead Status Register	page 4-35
0x16	RXS1 (WAN)	R	—	Receive S1 Overhead Status Register	page 4-36
0x17	—	—	—	Unused	—
0x18	RXC2	R	—	Receive C2 Overhead Status Register	page 4-34
0x19	RXG1	R	—	Receive G1 Overhead Status Register	page 4-34
0x1A	—	—	—	Unused	—
0x1B	—	—	—	Unused	—
0x1C	TXHDR1	R/W	—	Transmit Cell Header Control Register 1	page 4-10
0x1D	TXHDR2	R/W	—	Transmit Cell Header Control Register 2	page 4-11
0x1E	TXHDR3	R/W	—	Transmit Cell Header Control Register 3	page 4-11
0x1F	TXHDR4	R/W	—	Transmit Cell Header Control Register 4	page 4-12
0x20	TXIDL1	R/W	—	Transmit Idle Cell Header Control Register 1	page 4-12
0x21	TXIDL2	R/W	—	Transmit Idle Cell Header Control Register 2	page 4-13
0x22	TXIDL3	R/W	—	Transmit Idle Cell Header Control Register 3	page 4-13
0x23	TXIDL4	R/W	—	Transmit Idle Cell Header Control Register 4	page 4-14
0x24	RXHDR1	R/W	—	Receive Cell Header Control Register 1	page 4-18
0x25	RXHDR2	R/W	—	Receive Cell Header Control Register 2	page 4-18
0x26	RXHDR3	R/W	—	Receive Cell Header Control Register 3	page 4-19
0x27	RXHDR4	R/W	—	Receive Cell Header Control Register 4	page 4-19
0x28	RXMSK1	R/W	—	Receive Cell Mask Control Register 1	page 4-20
0x29	RXMSK2	R/W	—	Receive Cell Mask Control Register 2	page 4-20
0x2A	RXMSK3	R/W	—	Receive Cell Mask Control Register 3	page 4-21
0x2B	RXMSK4	R/W	—	Receive Cell Mask Control Register 4	page 4-21

Table 4-1. Control and Status Registers *(3 of 5)*

Address	Name	Type	OneSec Latching	Description	Page Number
0x2C	RXIDL1	R/W	—	Receive Idle Cell Header Control Register 1	page 4-22
0x2D	RXIDL2	R/W	—	Receive Idle Cell Header Control Register 2	page 4-22
0x2E	RXIDL3	R/W	—	Receive Idle Cell Header Control Register 3	page 4-23
0x2F	RXIDL4	R/W	—	Receive Idle Cell Header Control Register 4	page 4-23
0x30	IDLMSK1	R/W	—	Receive Idle Cell Mask Control Register 1	page 4-16
0x31	IDLMSK2	R/W	—	Receive Idle Cell Mask Control Register 2	page 4-16
0x32	IDLMSK3	R/W	—	Receive Idle Cell Mask Control Register 3	page 4-17
0x33	IDLMSK4	R/W	—	Receive Idle Cell Mask Control Register 4	page 4-17
0x34	ENSUMINT	R/W	—	Summary Interrupt Mask Control Register	page 4-43
0x35	ENSEC	R/W	—	Receive Section Interrupt Mask Control Register	page 4-42
0x36	ENLIN	R/W	—	Receive Line Interrupt Mask Control Register	page 4-41
0x37	ENPTH	R/W	—	Receive Path Interrupt Mask Control Register	page 4-42
0x38	ENCELLT	R/W	—	Transmit Cell Interrupt Mask Control Register	page 4-41
0x39	ENCELLR	R/W	—	Receive Cell Interrupt Mask Control Register	page 4-40
0x3A	ENAPS (WAN)	R/W	—	APS Interrupt Mask Control Register	page 4-39
0x3B	—	—	—	Unused	—
0x3C	SUMINT	R	—	Summary Interrupt Indication Status Register	page 4-50
0x3D	SECINT	R	—	Receive Section Interrupt Indication Status Register	page 4-49
0x3E	LININT	R	—	Receive Line Interrupt Indication Status Register	page 4-44
0x3F	PTHINT	R	—	Receive Path Interrupt Indication Status Register	page 4-45
0x40	TXCELLINT	R	—	Transmit Cell Interrupt Indication Status Register	page 4-51
0x41	RXCELLINT	R	—	Receive Cell Interrupt Indication Status Register	page 4-46
0x42	APSINT (WAN)	R	—	APS Interrupt Indication Status Register	page 4-38
0x43	—	—	—	Unused	—
0x44	—	—	—	Unused	—
0x45	RXSEC	R[7:2] R/W[1:0]	✓(2)	Receive Section Overhead Status Register	page 4-48
0x46	RXLIN	R[7:2] R/W[1:0]	✓(2)	Receive Line Overhead Status Register	page 4-47
0x47	RXPTH	R	✓(2)	Receive Path Overhead Status Register	page 4-47

Table 4-1. Control and Status Registers *(4 of 5)*

Address	Name	Type	OneSec Latching	Description	Page Number
0x48	TXCELL	R	✓(2)	Transmit Cell Status Register	page 4-51
0x49	RXCELL	R	✓(2)	Receive Cell Status Register	page 4-46
0x4A	RXAPS (WAN)	R	—	Receive APS Status Register	page 4-45
0x4B	—	—	—	unused	—
0x4C	LOCDCNT	R	✓(3)	LOCD Event Counter	page 4-57
0x4D	CORRCNT	R	✓(3)	Corrected HEC Error Counter	page 4-55
0x4E	UNCCNT	R	✓(3)	Uncorrected HEC Error Counter	page 4-63
0x4F	OOFCNT	R	✓(3)	OOF Event Counter	page 4-58
0x50	B2CNTL	R	✓(3)	Line BIP Error Counter (low byte)	page 4-58
0x51	B2CNTM	R	✓(3)	Line BIP Error Counter (mid byte)	page 4-54
0x52	B2CNTH	R	✓(3)	Line BIP Error Counter (high byte)	page 4-53
0x53	—	—	—	Unused	—
0x54	B1CNTL	R	✓(3)	Section BIP Error Counter (low byte)	page 4-52
0x55	B1CNTH	R	✓(3)	Section BIP Error Counter (high byte)	page 4-52
0x56	B3CNTL	R	✓(3)	Path BIP Error Counter (low byte)	page 4-55
0x57	B3CNTH	R	✓(3)	Path BIP Error Counter (high byte)	page 4-54
0x58	LFCNTL	R	✓(3)	Line FEBE Error Counter (low byte)	page 4-56
0x59	LFCNTM	R	✓(3)	Line FEBE Error Counter (mid byte)	page 4-57
0x5A	LFCNTH	R	✓(3)	Line FEBE Error Counter (high byte)	page 4-56
0x5B	—	—	—	unused	—
0x5C	PFCNTL	R	✓(3)	Path FEBE Error Counter (low byte)	page 4-59
0x5D	PFCNTH	R	✓(3)	Path FEBE Error Counter (high byte)	page 4-58
0x5E	NONCNTL	R	✓(3)	Non-Matching Cell Counter (low byte)	page 4-60
0x5F	NONCNTH	R	✓(3)	Non-Matching Cell Counter (high byte)	page 4-59
0x60	TXCNTL	R	✓(3)	Transmitted Cell Counter (low byte)	page 4-62
0x61	TXCNTM	R	✓(3)	Transmitted Cell Counter (mid byte)	page 4-63
0x62	TXCNTH	R	✓(3)	Transmitted Cell Counter (high byte)	page 4-62

Table 4-1. Control and Status Registers *(5 of 5)*

Address	Name	Type	OneSec Latching	Description	Page Number
0x63	—	—	—	Unused	—
0x64	RXCNTL	R	✓(3)	Received Cell Counter (low byte)	page 4-61
0x65	RXCNTM	R	✓(3)	Received Cell Counter (mid byte)	page 4-61
0x66	RXCNTH	R	✓(3)	Received Cell Counter (high byte)	page 4-60
0x67	—	—	—	Unused	—
0x68	TXSECBUF	R/W	—	Transmit Section Trace Circular Buffer	page 4-32
0x69	TXPTHBUF	R/W	—	Transmit Path Trace Circular Buffer	page 4-30
0x6A	RXSECBUF	R/W	—	Receive Section Trace Circular Buffer	page 4-37
0x6B	RXPTHBUF	R/W	—	Receive Path Trace Circular Buffer	page 4-36
0x6C	—	—	—	Unused	—
0x6D	—	—	—	Unused	—
0x6E	—	—	—	Unused	—
0x6F	—	—	—	Unused	—
0x70-0x7F	—	—	—	Unused	—

NOTE(S):

(1) These bits are cleared automatically by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register.

(2) Enabled by setting EnStatLat in the General Control register (0x00), bit 5 to a logic 1.

(3) Enabled by setting EnCntrLat in General Control register (0x00), bit 4 to a logic 1.

4.1 General Use Registers

This section describes several registers that are used for basic functions of the device.

0x01—CLKREC (Clock Recovery Control Register)

The CLKREC register controls the clock recovery and loopback testing capabilities of the device.

Bit	Default	Name	Description
7	0	InvTxClk	When written to a logic 1, this bit inverts the Transmit Clock output on LTxClk0+/- (pins 50, 51).
6	0	InvRxClk	This bit selects the type of Receive Clock sampling when using external clock recovery (Bit 5 is written to 1). When written to 1, the receive clock samples data on the falling edge. When written to 0, the receive clock samples data on the rising edge. When Bit 5 is written to 0, the setting of this bit has no effect.
5	0	ExtClkRec	When written to a logic 1, this bit enables External Clock Recovery. When enabled, the internal clock recovery circuit is bypassed. When written to 0, internal clock recovery is used.
4	0	TxClkSel(1)	These bits in combination provide the Transmit Clock Select as follows: 00 - TX clock synthesized from external 19.44 MHz input on PLLClk 01 - TX clock synthesized from recovered receive clock (loop timing) 10 - TX clock synthesized from external 8 kHz input on 8khzIn 11 - TX clock from external 155.52 MHz input on TxClkI+/-
3	0	TxClkSel(0)	
2	0	SrcLoop	When written to a logic 1, this bit invokes a source loopback. The receiver clock and data inputs are connected to the transmitter clock and data inputs. See Section 2.9 for more information.
1	0	LinLoop	When written to a logic 1, this bit enables Near-end Line Loopback. When enabled, the received line clock and data inputs are connected to line transmitter outputs. See Section 2.9 for more information.
0	0	UtopLoop	When written to a logic 1, this bit enables UTOPIA Loopback. When enabled, the received UTOPIA clock and data outputs are connected to UTOPIA transmitter inputs. The UTOPIA bus is placed in a high-impedance state. See Section 2.9 for more information.

0x00—GEN (General Control Register)

The GEN register controls the receiver hold input pin, one-second latch enables, block mode error counting, status pin selection, and device reset.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	EnIntPin	When written to a logic 1, this bit enables the MInt* pin (pin 6).
5	0	EnStatLat	When written to a logic 1, this bit enables 1-second status latching. When one-second status latching is enabled, the registers indicated in Table 4-1, footnote 2 is updated with new status information after a rising edge of the OneSecIn pin (pin 33). Status information in these registers is updated continuously if one-second status latching is disabled.
4	0	EnCntrLat	When written to a logic 1, this bit enables 1-second counter latching. When one-second counter latching is enabled, the registers indicated in Table 4-1, footnote 3 is updated with new count information after a rising edge of the OneSecIn pin (pin 33). Count information in these registers is updated continuously if one-second counter latching is disabled.
3	0	BlkMode	When written to a logic 1, this bit enables the Block Error Mode operation for BIP and FEBE counters. When this mode is enabled, a received BIP (section, line, and path) or FEBE (line and path) error increments the counter value by one count for each errored frame. There are 5 counters; B1Cnt, B2Cnt, B3Cnt, LFCnt and PFCnt. When this bit is written to 0, the actual number of BIP or FEBE errors received is added to the counter value.
2	0	User-defined Mode	When written to a logic 1, this bit enables the Status Output Pin Mode. When this mode is enabled, the StatOut[7:0] pins reflect the values in the OUTSTAT control register (0x02). When this bit is written to 0, output status for LOS, OOF, LOP, AIS-L, RDI-L, AIS-P, RDI-P and LOCD appears on the StatOut[7:0] pins or Data Link outputs. ***NOTE:*** This feature is overridden by the Data Link enables: EnTxSecDL (bit 6) in the TXSEC register (0x0C), EnTxLinDL (bit 4) in the TXLIN register (0x0D), EnRxSecDL (bit 0), and EnRxLinDL (bit 1) in the RXLIN register (0x46). See Section 2.4.3.4.
1	0	LgcRst	When written to a logic 1, this bit initiates a Logic Reset. When the device resets, all internal state machines are reset, but all registers (0x00 to 0x7F) listed as “Type: W/R” in Table 4-1 are unaltered.
0	0	MstRst	When written to a logic 1, this bit initiates a device Master Reset. When the device resets, internal state machines are held in reset, all registers (0x00 to 0x7F) assume their default values and Bits 1-7 in this register are overwritten with their default values.

0x02—OUTSTAT (Output Pin Control Register)

The OUTSTAT register contains the values that are reflected on the StatOut[7:0] pins when register 0x00 (GEN), bit 2 is written to 1, enabling Status Output Pin Mode.

Bit	Default	Name	Description
7	0	Outstat[7]	Value to be reflected to StatOut[7] pin.
6	0	Outstat[6]	Value to be reflected to StatOut[6] pin.
5	0	Outstat[5]	Value to be reflected to StatOut[5] pin.
4	0	Outstat[4]	Value to be reflected to StatOut[4] pin.
3	0	Outstat[3]	Value to be reflected to StatOut[3] pin.
2	0	Outstat[2]	Value to be reflected to StatOut[2] pin.
1	0	Outstat[1]	Value to be reflected to StatOut[1] pin.
0	0	Outstat[0]	Value to be reflected to StatOut[0] pin.

0x03—VERSION (Part Number/Version Status Register)

The VERSION register is used to identify the Conexant device and its revision level.

Bit	Default	Name	Description
7	WAN - 0 LAN - 1	Part[3] - MSB	This is the part number that uniquely identifies the RS825x device. The part number for the WAN RS825x (RS8250 and RS8254) is 0111. The part number for the LAN RS825x (RS8251 and RS8255) is 1111.
6	1	Part[2]	
5	1	Part[1]	
4	1	Part[0] - LSB	
3	0	Ver[3] - MSB	This is the version number that uniquely identifies the specific version of the RS825x device. Version numbers start at 1 for the first version and are incremented for each revision thereafter.
2	0	Ver[2]	
1	1	Ver[1]	
0	1	Ver[0] - LSB	

4.2 Cell Transmit Control Registers

This section describes the control registers used for transmission of traffic.

0x04—CGEN (Cell Generation Control Register)

The CGEN register controls the device's cell generation functions.

Bit	Default	Name	Description
7	0	DisHEC	When written to a logic 1, this bit disables internal generation of the HEC field. When disabled, the HEC field from the UTOPIA interface remains unchanged in the outgoing cell. When written to 0, HEC is internally calculated and inserted in the outgoing cell.
6	1	EnTxCos	When written to a logic 1, this bit enables the Transmitter HEC Coset. When written to 0, the HEC Coset is disabled.
5	1	EnTxCellScr	When written to a logic 1, this bit enables the $x^{43}+1$ Transmit Cell Scrambler in the cell generator. When written to 0, the Cell Scrambler is disabled.
4	0	InsGFC	When written to a logic 1, this bit inserts a Generic Flow Control (GFC) field in the outgoing header from the TXHDR registers. When written to 0, the GFC field comes from the UTOPIA interface.
3	0	InsVPI	When written to a logic 1, this bit inserts a Virtual Path Identifier (VPI) field in the outgoing header from the TXHDR registers. When written to 0, the VPI field comes from the UTOPIA interface.
2	0	InsVCI	When written to a logic 1, this bit inserts a Virtual Channel Identifier (VCI) field in the outgoing header from the TXHDR registers. When written to 0, the VCI field comes from the UTOPIA interface.
1	0	InsPT	When written to a logic 1, this bit inserts a Payload Type (PT) field in the outgoing header from the TXHDR registers. When written to 0, the PT field comes from the UTOPIA interface.
0	0	InsCLP	When written to a logic 1, this bit inserts a Cell Loss Priority (CLP) bit in the outgoing header from bit 0 in the TXHDR4 register (0x1F). When written to 0, the CLP field comes from the UTOPIA interface.

0x05—IDLPAY (Transmit Idle Cell Payload Control Register)

The IDLPAY register contains the transmit idle cell payload.

Bit	Default	Name	Description
7	0	IdlPay[7]	These bits hold the Transmit Idle Cell Payload values for outgoing idle cells.
6	1	IdlPay[6]	
5	1	IdlPay[5]	
4	0	IdlPay[4]	
3	1	IdlPay[3]	
2	0	IdlPay[2]	
1	1	IdlPay[1]	
0	0	IdlPay[0]	

0x1C—TXHDR1 (Transmit Cell Header Control Register 1)

The TXHDR1 register contains the first byte of the Transmit Cell Header. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxHdr1[7]	These bits hold the Transmit Header values for Octet 1 of the outgoing cell. Insertion of the bits is controlled by register 0x04 (CGEN). GFC bits. (Bit 7 is the GFC MSB.)
6	0	TxHdr1[6]	
5	0	TxHdr1[5]	
4	0	TxHdr1[4]	
3	0	TxHdr1[3]	VPI bits. (Bit 3 is the GFC MSB.)
2	0	TxHdr1[2]	
1	0	TxHdr1[1]	
0	0	TxHdr1[0]	

0x1D—TXHDR2 (Transmit Cell Header Control Register 2)

The TXHDR2 register contains the second byte of the Transmit Cell Header. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxHdr2[7]	These bits hold the Transmit Header values for Octet 2 of the outgoing cell. Insertion of the bits is controlled by the CGEN register (0x04). VPI bits. (Bit 4 is the VPI LSB.)
6	0	TxHdr2[6]	
5	0	TxHdr2[5]	
4	0	TxHdr2[4]	
3	0	TxHdr2[3]	VCI bits. (BIT 3 is the VCI MSB.)
2	0	TxHdr2[2]	
1	0	TxHdr2[1]	
0	0	TxHdr2[0]	

0x1E—TXHDR3 (Transmit Cell Header Control Register 3)

The TXHDR3 register contains the third byte of the Transmit Cell Header. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxHdr3[7]	These bits hold the Transmit Header values for Octet 3 of the outgoing cell. Insertion of the bits is controlled by the CGEN register (0x04). VCI bits. (Bit 0 is the VCI LSB.)
6	0	TxHdr3[6]	
5	0	TxHdr3[5]	
4	0	TxHdr3[4]	
3	0	TxHdr3[3]	
2	0	TxHdr3[2]	
1	0	TxHdr3[1]	
0	0	TxHdr3[0]	

0x1F—TXHDR4 (Transmit Cell Header Control Register 4)

The TXHDR4 register contains the fourth byte of the Transmit Cell Header. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxHdr4[7]	These bits hold the Transmit Header values for Octet 4 of the outgoing cell. Insertion of the bits is controlled by the CGEN register (0x04). VCI bits. (Bit 4 is the VCI LSB).
6	0	TxHdr4[6]	
5	0	TxHdr4[5]	
4	0	TxHdr4[4]	
3	0	TxHdr4[3]	Payload-type bits
2	0	TxHdr4[2]	
1	0	TxHdr4[1]	
0	0	TxHdr4[0]	Cell Loss Priority bit

0x20—TXIDL1 (Transmit Idle Cell Header Control Register 1)

The TXIDL1 register contains the first byte of the Transmit Idle Cell Header. It contains the header value that is inserted in idle cells transmitted from the device. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxIdl1[7]	These bits hold the Transmit Idle Cell Header values for Octet 1 of the outgoing cell. GFC bits. (Bit 7 is the GFC MSB.)
6	0	TxIdl1[6]	
5	0	TxIdl1[5]	
4	0	TxIdl1[4]	
3	0	TxIdl1[3]	VPI bits. (Bit 3 is the VPI MSB.)
2	0	TxIdl1[2]	
1	0	TxIdl1[1]	
0	0	TxIdl1[0]	

0x21—TXIDL2 (Transmit Idle Cell Header Control Register 2)

The TXIDL2 register contains the second byte of the Transmit Idle Cell Header. It contains the header value that is inserted in idle cells transmitted from the device. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxIdl2[7]	These bits hold the Transmit Idle Cell Header values for Octet 2 of the outgoing cell.
6	0	TxIdl2[6]	VPI bits. (Bit 4 is the VPI LSB.)
5	0	TxIdl2[5]	
4	0	TxIdl2[4]	
3	0	TxIdl2[3]	VCI bits. ((Bit 3 is the VCI MSB.)
2	0	TxIdl2[2]	
1	0	TxIdl2[1]	
0	0	TxIdl2[0]	

0x22—TXIDL3 (Transmit Idle Cell Header Control Register 3)

The TXIDL3 register contains the third byte of the Transmit Idle Cell Header. It contains the header value that is inserted in idle cells transmitted from the device. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxIdl3[7]	These bits hold the Transmit Idle Cell Header values for Octet 3 of the outgoing cell.
6	0	TxIdl3[6]	VCI bits
5	0	TxIdl3[5]	
4	0	TxIdl3[4]	
3	0	TxIdl3[3]	
2	0	TxIdl3[2]	
1	0	TxIdl3[1]	
0	0	TxIdl3[0]	

0x23—TXIDL4 (Transmit Idle Cell Header Control Register 4)

The TXIDL4 register contains the fourth byte of the Transmit Idle Cell Header. It contains the header value that is inserted in idle cells transmitted from the device. This header consists of 32 bits divided among four registers. Cell generation is described in detail in Section 2.5.

Bit	Default	Name	Description
7	0	TxIdl4[7]	These bits hold the Transmit Idle Cell Header values for Octet 4 of the outgoing cell.
6	0	TxIdl4[6]	VCI bits. (Bit 4 is the VCI LSB.)
5	0	TxIdl4[5]	
4	0	TxIdl4[4]	
3	0	TxIdl4[3]	Payload-type bits
2	0	TxIdl4[2]	
1	0	TxIdl4[1]	
0	1	TxIdl4[0]	Cell Loss Priority bit

4.3 Cell Receive Control Registers

This section describes the control registers used for reception of traffic.

0x08—CVAL (Cell Validation Control Register)

The CVAL register controls the validation of incoming cells to be received across the UTOPIA interface.

Bit	Default	Name	Description
7	0	RejHdr	When written to a logic 1, this bit enables the Reject Header function. When enabled, cells with matching headers are rejected and all others are accepted. When written to 0, cells with headers matching the RXHDRx/RXMSKx definition are accepted.
6	1	DelIdle	When written to a logic 1, this bit enables the Deletion of Idle Cells. When enabled, cells matching the RXIDL/IDLMSK definition are deleted from the received cell stream. When written to 0, idle cells are included in the received stream.
5	1	EnRxCellScr	When written to a logic 1, this bit enables the $x^{43}+1$ Cell Scrambler in the cell receiver.
4	1	EnRxCos	When written to a logic 1, this bit enables the Receiver HEC Coset.
3	0	EnHdrCorr	When written to a logic 1, this bit enables the HEC Correction state machine. When written to 0, only HEC error detection is performed.
2	0	DisHECChk	When written to a logic 1, this bit disables HEC Checking. When disabled, HEC checking is not performed as a cell validation criteria.
1	0	DisCellRcvr	When written to a logic 1, this bit disables the Cell Receiver. When disabled, all cell reception is disabled on the next cell boundary. When written to 0, cell reception begins or resumes on the next cell boundary. (See also UtopDis (bit 5) in the 0x0B–UTOP2 register, on page 4-25.)
0	0	DisLOCD	When written to a logic 1, this bit disables Loss of Cell Delineation. When disabled, cells are passed to the UTOPIA port even if cell delineation has not been found. When written to 0, cells are passed to the UTOPIA port only while cell alignment has been achieved.

0x30—IDLMSK1 (Receive Idle Cell Mask Control Register 1)

The IDLMSK1 register contains the first byte of the Receive Idle Cell Mask. It modifies the ATM cell screen in the RXIDL1 register. Setting a bit in the Mask register causes the corresponding bit in the received ATM idle cell header to be disregarded for screening. For example, setting IDLMSK1, bit 0 to 1, causes cells to be accepted as ATM idle cells with either 1 or 0 in the octet 1, bit 0 position. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	IdlMsk1[7]	These bits hold the Receive Idle cell header mask for Octet 1 of the incoming cell.
6	0	IdlMsk1[6]	
5	0	IdlMsk1[5]	
4	0	IdlMsk1[4]	
3	0	IdlMsk1[3]	
2	0	IdlMsk1[2]	
1	0	IdlMsk1[1]	
0	0	IdlMsk1[0]	

0x31—IDLMSK2 (Receive Idle Cell Mask Control Register 2)

The IDLMSK2 register contains the second byte of the Receive Idle Cell Mask. It modifies the ATM cell screen in the RXIDL1 register. Setting a bit in the Mask register causes the corresponding bit in the received ATM idle cell header to be disregarded for screening. For example, setting IDLMSK1, bit 0 to 1, causes cells to be accepted as ATM idle cells with either 1 or 0 in the octet 1, bit 0 position. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	IdlMsk2[7]	These bits hold the Receive Idle cell header mask for Octet 2 of the incoming cell.
6	0	IdlMsk2[6]	
5	0	IdlMsk2[5]	
4	0	IdlMsk2[4]	
3	0	IdlMsk2[3]	
2	0	IdlMsk2[2]	
1	0	IdlMsk2[1]	
0	0	IdlMsk2[0]	

0x32—IDLMSK3 (Receive Idle Cell Mask Control Register 3)

The IDLMSK3 register contains the third byte of the Receive Idle Cell Mask. It modifies the ATM cell screen in the Receive Cell Header register. Setting a bit in the Mask register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1, bit 0 to 1, causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	IdlMsk3[7]	These bits hold the Receive Idle cell header mask for Octet 3 of the incoming cell.
6	0	IdlMsk3[6]	
5	0	IdlMsk3[5]	
4	0	IdlMsk3[4]	
3	0	IdlMsk3[3]	
2	0	IdlMsk3[2]	
1	0	IdlMsk3[1]	
0	0	IdlMsk3[0]	

0x33—IDLMSK4 (Receive Idle Cell Mask Control Register 4)

The IDLMSK4 register contains the fourth byte of the Receive Idle Cell Mask. It modifies the ATM cell screen in the Receive Cell Header register. Setting a bit in the Mask register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1, bit 0 to 1, causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	IdlMsk4[7]	These bits hold the Receive Idle cell header mask for Octet 4 of the incoming cell.
6	0	IdlMsk4[6]	
5	0	IdlMsk4[5]	
4	0	IdlMsk4[4]	
3	0	IdlMsk4[3]	
2	0	IdlMsk4[2]	
1	0	IdlMsk4[1]	
0	0	IdlMsk4[0]	

0x24—RXHDR1 (Receive Cell Header Control Register 1)

The RXHDR1 register contains the first byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port. If an incoming ATM cell header matches the value in the header register, the cell is directed to the UTOPIA port. Receive Header Mask registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxHdr1[7]	These bits hold the Receive Header values for Octet 1 of the incoming cell.
6	0	RxHdr1[6]	
5	0	RxHdr1[5]	
4	0	RxHdr1[4]	
3	0	RxHdr1[3]	
2	0	RxHdr1[2]	
1	0	RxHdr1[1]	
0	0	RxHdr1[0]	

0x25—RXHDR2 (Receive Cell Header Control Register 2)

The RXHDR2 register contains the second byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port. If an incoming ATM cell header matches the value in the header register, the cell is directed to the UTOPIA port. Receive Header Mask registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxHdr2[7]	These bits hold the Receive Header values for Octet 2 of the incoming cell.
6	0	RxHdr2[6]	
5	0	RxHdr2[5]	
4	0	RxHdr2[4]	
3	0	RxHdr2[3]	
2	0	RxHdr2[2]	
1	0	RxHdr2[1]	
0	0	RxHdr2[0]	

0x26—RXHDR3 (Receive Cell Header Control Register 3)

The RXHDR3 register contains the third byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port. If an incoming ATM cell header matches the value in the header register, the cell is directed to the UTOPIA port. Receive Header Mask registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxHdr3[7]	These bits hold the Receive Header values for Octet 3 of the incoming cell.
6	0	RxHdr3[6]	
5	0	RxHdr3[5]	
4	0	RxHdr3[4]	
3	0	RxHdr3[3]	
2	0	RxHdr3[2]	
1	0	RxHdr3[1]	
0	0	RxHdr3[0]	

0x27—RXHDR4 (Receive Cell Header Control Register 4)

The RXHDR4 register contains the fourth byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port. If an incoming ATM cell header matches the value in the header register, the cell is directed to the UTOPIA port. Receive Header Mask registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxHdr4[7]	These bits hold the Receive Header values for Octet 4 of the incoming cell.
6	0	RxHdr4[6]	
5	0	RxHdr4[5]	
4	0	RxHdr4[4]	
3	0	RxHdr4[3]	
2	0	RxHdr4[2]	
1	0	RxHdr4[1]	
0	0	RxHdr4[0]	

0x28—RXMSK1 (Receive Cell Mask Control Register 1)

The RXMSK1 register contains the first byte of the Receive Cell Mask. It modifies the ATM cell screen in the Receive Cell Header register. Setting a bit in the Mask register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1, bit 0 to 1, causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	1	RxMsk1[7]	These bits hold the Receive Header Mask for Octet 1 of the incoming cell.
6	1	RxMsk1[6]	
5	1	RxMsk1[5]	
4	1	RxMsk1[4]	
3	1	RxMsk1[3]	
2	1	RxMsk1[2]	
1	1	RxMsk1[1]	
0	1	RxMsk1[0]	

0x29—RXMSK2 (Receive Cell Mask Control Register 2)

The RXMSK2 register contains the second byte of the Receive Cell Mask. It modifies the ATM cell screen in the Receive Cell Header register. Setting a bit in the Mask register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1, bit 0 to 1, causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	1	RxMsk2[7]	These bits hold the Receive Header Mask for Octet 2 of the incoming cell.
6	1	RxMsk2[6]	
5	1	RxMsk2[5]	
4	1	RxMsk2[4]	
3	1	RxMsk2[3]	
2	1	RxMsk2[2]	
1	1	RxMsk2[1]	
0	1	RxMsk2[0]	

0x2A—RXMSK3 (Receive Cell Mask Control Register 3)

The RXMSK3 register contains the third byte of the Receive Cell Mask. It modifies the ATM cell screen in the Receive Cell Header register. Setting a bit in the Mask register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1, bit 0 to 1, causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	1	RxMsk3[7]	These bits hold the Receive Header Mask for Octet 3 of the incoming cell.
6	1	RxMsk3[6]	
5	1	RxMsk3[5]	
4	1	RxMsk3[4]	
3	1	RxMsk3[3]	
2	1	RxMsk3[2]	
1	1	RxMsk3[1]	
0	1	RxMsk3[0]	

0x2B—RXMSK4 (Receive Cell Mask Control Register 4)

The RXMSK4 register contains the fourth byte of the Receive Cell Mask. It modifies the ATM cell screen in the Receive Cell Header register. Setting a bit in the Mask register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1, bit 0 to 1, causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	1	RxMsk4[7]	These bits hold the Receive Header Mask for Octet 4 of the incoming cell.
6	1	RxMsk4[6]	
5	1	RxMsk4[5]	
4	1	RxMsk4[4]	
3	1	RxMsk4[3]	
2	1	RxMsk4[2]	
1	1	RxMsk4[1]	
0	1	RxMsk4[0]	

0x2C—RXIDL1 (Receive Idle Cell Header Control Register 1)

The RXIDL1 register contains the first byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are counted and discarded from the received stream if DelIdle, bit 6 in the CVAL register (0x08), is set to 1. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxIdl1[7]	These bits hold the Receive Idle cell header for Octet 1 of the incoming cell.
6	0	RxIdl1[6]	
5	0	RxIdl1[5]	
4	0	RxIdl1[4]	
3	0	RxIdl1[3]	
2	0	RxIdl1[2]	
1	0	RxIdl1[1]	
0	0	RxIdl1[0]	

0x2D—RXIDL2 (Receive Idle Cell Header Control Register 2)

The RXIDL2 register contains the second byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are counted and discarded from the received stream if DelIdle, bit 6 in the CVAL register (0x08), is set to 1. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxIdl2[7]	These bits hold the Receive Idle cell header for Octet 2 of the incoming cell.
6	0	RxIdl2[6]	
5	0	RxIdl2[5]	
4	0	RxIdl2[4]	
3	0	RxIdl2[3]	
2	0	RxIdl2[2]	
1	0	RxIdl2[1]	
0	0	RxIdl2[0]	

0x2E—RXIDL3 (Receive Idle Cell Header Control Register 3)

The RXIDL3 register contains the third byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are counted and discarded from the received stream if DelIdle, bit 6 in the CVAL register (0x08), is set to 1. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxIdl3[7]	These bits hold the Receive Idle cell header for Octet 3 of the incoming cell.
6	0	RxIdl3[6]	
5	0	RxIdl3[5]	
4	0	RxIdl3[4]	
3	0	RxIdl3[3]	
2	0	RxIdl3[2]	
1	0	RxIdl3[1]	
0	0	RxIdl3[0]	

0x2F—RXIDL4 (Receive Idle Cell Header Control Register 4)

The RXIDL4 register contains the fourth byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are counted and discarded from the received stream if DelIdle, bit 6 in the CVAL register (0x08), is set to 1. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxIdl4[7]	These bits hold the Receive Idle cell header for Octet 4 of the incoming cell.
6	0	RxIdl4[6]	
5	0	RxIdl4[5]	
4	0	RxIdl4[4]	
3	0	RxIdl4[3]	
2	0	RxIdl4[2]	
1	0	RxIdl4[1]	
0	1	RxIdl4[0]	

4.4 UTOPIA Control Registers

This section describes the control registers for the UTOPIA block of the device.

0x0A—UTOP1 (UTOPIA Control Register 1)

The UTOP1 register controls the mode of operation for the UTOPIA interface.

Bit	Default	Name	Description
7	0	TxReset	When written to a logic 1, this bit resets the transmit FIFO pointers. This reset must be used as a test function since it can create short cells.
6	0	RxReset	When written to a logic 1, this bit resets the receive FIFO pointers. This reset must be used as a test function since it can create short cells.
5	1	UtopMode	When written to a logic 1, this bit enables UTOPIA Level 2 Mode. When written to a logic 0, UTOPIA Level 1 operation is enabled.
4	1	Handshake	When written to a logic 1, this bit enables cell handshaking. When written to a logic 0, octet handshaking is enabled.
3	0	BusWidth	When written to a logic 1, this bit enables the 8-bit bus. When written to a logic 0, the 16-bit bus is enabled.
2	0	Odd/Even	This bit determines Odd/Even Parity. When written to a logic 1, even parity is generated and checked. When written to a logic 0, odd parity is generated and checked.
1	0	TxFill[1]	These bits set the Transmit FIFO Fill Level threshold for UTxClAv (pin 89). 00 - UTxClav indicates full after 1 more cell 01 - UTxClav indicates full after 2 more cells 10 - UTxClav indicates full after 3 more cells 11 - UTxClav indicates full after 3 more cells
0	0	TxFill[0]	

0x0B—UTOP2 (UTOPIA Control Register 2)

The UTOP2 register contains the multi-PHY address value for the device.

Bit	Default	Name	Description
7	0	Test 1	This is a test function; set to a logic 0.
6	0	Test 2	This is a test function; set to a logic 0.
5	0	UtopDis	When written to a logic 1, this bit disables the UTOPIA receiver outputs. (This must not be confused with the DisCellRcvr bit, which completely stops cell processing). The UtopDis bit puts the receive side of the UTOPIA outputs (i.e., URxData[15:0], URxPrty, URxSOC, URxClav, and UTxClav) in a high impedance state.
4	0	MphyAddr[4] - MSB	These bits hold the Multi-PHY Device Address. ~The dual and quad devices, RS8254/5, have a multi-PHY default address of 00000 for port A and 00001 for port B. Additionally, quad devices, RS8254/5, have a multi-PHY default address of 000010 for port C and 00011 for port D.
3	0	MphyAddr[3]	
2	0	MphyAddr[2]	
1	0~	MphyAddr[1]	
0	0~	MphyAddr[0] - LSB	

4.5 SONET Overhead Transmit Control Registers

This section describes the control registers used for SONET Overhead transmission.

0x06—ERRINS (Error Insertion Control Register)

The ERRINS register controls error insertion into various octets for diagnostic purposes. These bits are cleared automatically by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register.

Bit	Default	Name	Description
7	0	InsFrErr	When written to a logic 1, this bit inverts the A1 bytes for one transmit frame. When written to 0, the A1 bytes are not inverted.
6	0	InsB1Err	This bit XORs the B1 BIP calculation with the ERRPAT register (0x07) value and inserts the new value into the transmitted B1 byte for one transmit frame only.
5	0	InsB2Err1	This bit XORs the B2-1 BIP calculation with the ERRPAT register (0x07) value and inserts the new value into the transmitted B2-1 byte for one transmit frame only.
4	0	InsB2Err2	This bit XORs the B2-2 BIP calculation with the ERRPAT register (0x07) value and inserts the new value into the transmitted B2-2 byte for one transmit frame only.
3	0	InsB2Err3	This bit XORs the B2-3 BIP calculation with the ERRPAT register (0x07) value and inserts the new value into the transmitted B2-3 byte for one transmit frame only.
2	0	InsB3Err	This bit XORs the B3 BIP calculation with the ERRPAT register (0x07) value and inserts the new value into the transmitted B3 byte for one transmit frame only.
1	0	InsHECErr	This bit XORs the HEC byte with the ERRPAT register (0x07) value and inserts the new value into the transmitted HEC byte for one transmit cell only.
0	0	—	Reserved, set to 0.

0x07—ERRPAT (Error Pattern Control Register)

The ERRPAT register provides the error pattern for the error insertion functions listed in the ERRINS register. Each bit in the error pattern register is XORed with the corresponding bit of the octet to be errored.

Bit	Default	Name	Description
7	0	ErrPat[7]	Error pattern bit 7.
6	0	ErrPat[6]	Error pattern bit 6.
5	0	ErrPat[5]	Error pattern bit 5.
4	0	ErrPat[4]	Error pattern bit 4.
3	0	ErrPat[3]	Error pattern bit 3.
2	0	ErrPat[2]	Error pattern bit 2.
1	0	ErrPat[1]	Error pattern bit 1.
0	0	ErrPat[0]	Error pattern bit 0.

0x13—TXC2 (Transmit C2 Overhead Control Register)

The TXC2 register controls the C2 byte in the transport overhead. This byte is allocated to identify the construction and content of the STS-level SPE.

Bit	Default	Name	Description
7	0	TxC2[1]	Transmit value for C2 Overhead Octet—bit 1 (MSB)
6	0	TxC2[2]	Transmit value for C2 Overhead Octet—bit 2
5	0	TxC2[3]	Transmit value for C2 Overhead Octet—bit 3
4	1	TxC2[4]	Transmit value for C2 Overhead Octet—bit 4
3	0	TxC2[5]	Transmit value for C2 Overhead Octet—bit 5
2	0	TxC2[6]	Transmit value for C2 Overhead Octet—bit 6
1	1	TxC2[7]	Transmit value for C2 Overhead Octet—bit 7
0	1	TxC2[8]	Transmit value for C2 Overhead Octet—bit 8 (LSB)

0x10—TXK1 (Transmit K1 Overhead Control Register) (WAN Only)

The TXK1 register controls the K1 byte in the transport overhead. The K1 and K2 bytes are allocated for Automatic Protection Switching (APS) signaling between Line level entities. These bytes are defined only for the first STS-1 of the STS-3c signal.

This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bit	Default	Name	Description
7	0	TxK1[1]	Transmit value for K1 Overhead Octet—bit 1 (MSB)
6	0	TxK1[2]	Transmit value for K1 Overhead Octet—bit 2
5	0	TxK1[3]	Transmit value for K1 Overhead Octet—bit 3
4	0	TxK1[4]	Transmit value for K1 Overhead Octet—bit 4
3	0	TxK1[5]	Transmit value for K1 Overhead Octet—bit 5
2	0	TxK1[6]	Transmit value for K1 Overhead Octet—bit 6
1	0	TxK1[7]	Transmit value for K1 Overhead Octet—bit 7
0	0	TxK1[8]	Transmit value for K1 Overhead Octet—bit 8 (LSB)

0x11—TXK2 (Transmit K2 Overhead Control Register) (WAN Only)

The TXK2 register controls the K2 byte in the transport overhead. The K1 byte and bits 0-5 of the K2 byte are allocated for Automatic Protection Switching (APS) signaling between Line level entities. These bytes are defined only for the first STS-1 of the STS-3c signal. This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bits 6-8 of the K2 byte are allocated for Alarm Indication Signal (AIS) and Remote Defect Indicator (RDI). These bytes are defined only for the first STS-1 of the STS-3c signal.

Bit	Default	Name	Description
7	0	TxK2[1]	Transmit value for K2 Overhead Octet—bit 1 (MSB)
6	0	TxK2[2]	Transmit value for K2 Overhead Octet—bit 2
5	0	TxK2[3]	Transmit value for K2 Overhead Octet—bit 3
4	0	TxK2[4]	Transmit value for K2 Overhead Octet—bit 4
3	0	TxK2[5]	Transmit value for K2 Overhead Octet—bit 5
2	0	TxK2[6]	Transmit value for K2 Overhead Octet—bit 6
1	0	TxK2[7]	Transmit value for K2 Overhead Octet—bit 7
0	0	TxK2[8]	Transmit value for K2 Overhead Octet—bit 8 (LSB)

0x0D—TXLIN (Transmit Line Overhead Control Register)

The TXLIN register controls the transmission of various octets in the Line Overhead of the SONET frame.

Bit	Default	Name	Description
7	0	STMMode	When written to a logic 1, this bit enables the STM-1 Mode pointer. When enabled, the H1/H2 bytes are 6A/0A. When written to 0, the H1/H2 bytes are 62/0A. Bit 6 (DisPntr) overrides this function.
6	0	DisPntr	When this bit is written to a logic 1, the H1/H2 Overhead bytes are forced to 33, When written to 0, the H1/H2 value is determined by bit 7.
5	0	DisB2	When written to a logic 1, this bit disables the BIP calculations for the Line Overhead. When disabled, the B2 bytes are set to 00. When written to 0, the BIP calculations are enabled, and the results are placed in the B2 bytes.
4	0	EnTxLinDL	When written to a logic 1, this bit enables the Transmit D4-D12 bytes of the Data Link. When written to 0, these bytes are forced to all 00.
3	0	InsLnAIS	When written to a logic 1, this bit inserts Line AIS. All bits except the section overhead octets are written to a logic 1 prior to scrambling. When written to 0, Line AIS is not inserted.
2	0	InsLnRDI	When written to a logic 1, this bit inserts Line RDI. K2 bits 6, 7, and 8 are set to 110. When written to 0, K2 bits 6, 7, and 8 are set to the values of the bits 6, 7, and 8 in the TxK2 register.
1	1	AutoLnRDI	When written to a logic 1, this bit enables Automatic Line RDI. When enabled, line RDI is automatically generated upon reception of LOS, LOF, or AIS-L. When written to 0, Automatic Line RDI is disabled.
0	1	AutoLnFEBE	When written to a logic 1, this bit enables Automatic Line FEBE. When written to 1, line FEBE codes are automatically inserted upon reception of line BIP errors. When written to 0, Automatic Line FEBE is disabled.

0x0E—TXPTH (Transmit Path Overhead Control Register)

The TXPTH register controls the transmission of various octets in the Path Overhead of the SONET frame.

Bit	Default	Name	Description
7	0	EnPthTr	When written to a logic 1, this bit enables the Path Trace Message (J1). When written to 0, the J1 byte contains 00.
6	0	DisB3	When written to a logic 1, this bit disables the BIP calculation for the Path Overhead. When disabled, the B3 byte is set to 00. When written to 0, the BIP calculation is enabled, and the result is placed in the B3 byte.
5	1	AutoPthFEBE	When written to a logic 1, this bit enables Automatic Path FEBE. When enabled, path FEBE codes are automatically inserted upon reception of path BIP errors. When written to 0, Automatic Path FEBE is not enabled.
4	0	InsPthAIS	When written to a logic 1, this bit inserts Path AIS. When written to 0, Path AIS is not inserted.
3	0	TxRDI[7]	This value is mapped to Transmit RDI bit 7 in the G1 path overhead octet.(1)
2	0	TxRDI[6]	This value is mapped to Transmit RDI bit 6 in the G1 path overhead octet.
1	1	TxRDI[5]	This value is mapped to Transmit RDI bit 5 in the G1 path overhead octet.(1)
0	1	AutoPthRDI	When written to a logic 1, this bit enables Automatic Path RDI. When enabled, path RDI is automatically generated for at least 10 frames upon reception of LOS, LOF, LOP, AIS-L, AIS-P, UNEQ-P, or PLM-P. When written to 0, path RDI (G1, bits 5-7) is inserted from bits 3:1 of this register.

NOTE(S):
(1) Transmit RDI bits 5 and 7 are reversed as compared to Receive G1 Overhead Status register (0x 19–RX G1). See 0x19—RXG1 (Receive G1 Overhead Status register) on page 4-35.

0x69—TXPTHBUF (Transmit Path Trace Circular Buffer)

The TXPTHBUF buffer, the J1 byte, is used to transmit repeatedly a 64-byte, fixed-length string so that a receiving terminal in a path can verify its continued connection to the intended transmitter.

Bit	Default	Name	Description
7	x	TxPthBuf[7]	Transmit Path Trace Circular Buffer bit 7.
6	x	TxPthBuf[6]	Transmit Path Trace Circular Buffer bit 6.
5	x	TxPthBuf[5]	Transmit Path Trace Circular Buffer bit 5.
4	x	TxPthBuf[4]	Transmit Path Trace Circular Buffer bit 4.
3	x	TxPthBuf[3]	Transmit Path Trace Circular Buffer bit 3.
2	x	TxPthBuf[2]	Transmit Path Trace Circular Buffer bit 2.
1	x	TxPthBuf[1]	Transmit Path Trace Circular Buffer bit 1.
0	x	TxPthBuf[0]	Transmit Path Trace Circular Buffer bit 0.

0x12—TXS1 (Transmit S1 Overhead Control Register) (WAN Only)

The TXS1 register controls the S1 byte in the transport overhead. This byte is allocated for transporting synchronization status messages and is defined only for the first STS-1 of the STS-3c signal. These messages provide an indication of the quality level of the synchronization source of the SONET signal.

This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bit	Default	Name	Description
7	0	TxS1[1]	Transmit value for S1 Overhead Octet—bit 1 (MSB)
6	0	TxS1[2]	Transmit value for S1 Overhead Octet—bit 2
5	0	TxS1[3]	Transmit value for S1 Overhead Octet—bit 3
4	0	TxS1[4]	Transmit value for S1 Overhead Octet—bit 4
3	0	TxS1[5]	Transmit value for S1 Overhead Octet—bit 5
2	0	TxS1[6]	Transmit value for S1 Overhead Octet—bit 6
1	0	TxS1[7]	Transmit value for S1 Overhead Octet—bit 7
0	0	TxS1[8]	Transmit value for S1 Overhead Octet—bit 8 (LSB)

0x0C—TXSEC (Transmit Section Overhead Control Register)

The TXSEC register controls transmission of various octets in the Section Overhead of the SONET frame.

Bit	Default	Name	Description
7	0	DisTxScr	When written to a logic 1, this bit disables the Transmit Frame Scrambler. When written to 0, scrambling is enabled.
6	0	EnTxSecDL	When written to a logic 1, this bit enables the Transmit D1/D2/D3 bytes of the Data Link. When written to 0, these bytes are forced to all 00.
5	0	EnSecTr	When written to a logic 1, this bit enables the Section Trace Message (J0). When written to 0, the J0 byte contains 01. The Z0/Z0 bytes contain 02/03 regardless of the Bit 5 setting.
4	0	DisA1A2	When this bit is written to a logic 1, the A1/A2 Overhead bytes are forced to 00. When written to 0, the A1/A2 Overhead bytes contain their default values (F6/28).
3	0	DisB1	When written to a logic 1, this bit disables the BIP calculation for the Section Overhead. When disabled, the B1 byte is set to 00. When written to 0, the BIP calculation is enabled, and the result is placed in the B1 byte.
2	0	InsAllZer	When written to a logic 1, this bit inserts 0s after the Transmit Frame Scrambler output. When written to 0, cell/overhead data is transmitted.
1	0	TxFrmPulOut	This bit selects the type of output sent to the TxFrameRef pin (pin 35). When written to a logic 1, the transmit octet clock (19.44 MHz) is present. When written to a logic 0, a Transmit Frame Pulse (8 kHz) is present.
0	0	TxFrmPulPol	This bit selects the polarity of the TxFrameRef pin (pin 35). When written to a logic 1, the frame pulse output is an active high. When written to 0, the frame pulse output is an active low.

0x68—TXSECBUF (Transmit Section Trace Circular Buffer, J0)

The TXSECBUF buffer, the J0 byte, is used to transmit repeatedly a 64-byte, fixed-length string so that a receiving terminal in a section can verify its continued connection to the intended transmitter. This buffer is also used as a Section trace for SDH.

Bit	Default	Name	Description
7	x	TxSecBuf[7]	Transmit Section Trace Circular Buffer bit 7.
6	x	TxSecBuf[6]	Transmit Section Trace Circular Buffer bit 6.
5	x	TxSecBuf[5]	Transmit Section Trace Circular Buffer bit 5.
4	x	TxSecBuf[4]	Transmit Section Trace Circular Buffer bit 4.
3	x	TxSecBuf[3]	Transmit Section Trace Circular Buffer bit 3.
2	x	TxSecBuf[2]	Transmit Section Trace Circular Buffer bit 2.
1	x	TxSecBuf[1]	Transmit Section Trace Circular Buffer bit 1.
0	x	TxSecBuf[0]	Transmit Section Trace Circular Buffer bit 0.

4.6 SONET Overhead Receive Control Registers

This section describes the control registers used for SONET Overhead reception.

0x09—APSTHRESH (APS Threshold Control Register) (WAN Only)

The APSTHRESH register sets the threshold value for Signal Fail and Signal Degrade Alarm generation. Bits 7–4 are the signal fail threshold exponent (default = 10^{-3}) and bits 3–0 are the signal degrade threshold exponent (default = 10^{-6}).

This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bit	Default	Name	Description
7	0	SFThresh[3]	Threshold exponent value for setting signal fail status—Bit 3 (MSB)
6	0	SFThresh[2]	Threshold exponent value for setting signal fail status—Bit 2
5	1	SFThresh[1]	Threshold exponent value for setting signal fail status—Bit 1
4	1	SFThresh[0]	Threshold exponent value for setting signal fail status—Bit 0 (LSB)
3	0	SDThresh[3]	Threshold exponent value for setting signal degrade status—Bit 3 (MSB)
2	1	SDThresh[2]	Threshold exponent value for setting signal degrade status—Bit 2
1	1	SDThresh[1]	Threshold exponent value for setting signal degrade status—Bit 1
0	0	SDThresh[0]	Threshold exponent value for setting signal degrade status—Bit 0 (LSB)

0x18—RXC2 (Receive C2 Overhead Status Register)

The RXC2 register provides C2 overhead status. This byte is allocated to identify the construction and content of the STS-level SPE, and for STS Path Defect Indication (PDI-P). PDI-P indicates to downstream equipment that there is a payload defect.

Bit	Default	Name	Description
7	x	RxC2[1]	Receive value for C2 Overhead Octet—bit 1 (MSB)
6	x	RxC2[2]	Receive value for C2 Overhead Octet—bit 2
5	x	RxC2[3]	Receive value for C2 Overhead Octet—bit 3
4	x	RxC2[4]	Receive value for C2 Overhead Octet—bit 4
3	x	RxC2[5]	Receive value for C2 Overhead Octet—bit 5
2	x	RxC2[6]	Receive value for C2 Overhead Octet—bit 6
1	x	RxC2[7]	Receive value for C2 Overhead Octet—bit 7
0	x	RxC2[8]	Receive value for C2 Overhead Octet—bit 8 (LSB)

0x19—RXG1 (Receive G1 Overhead Status Register)

The RXG1 register is used to provide path status information to the originating terminal.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	0	—	Reserved, set to 0.
3	x	RxRDI[5]	Received value of bit 5 of the G1 octet.
2	x	RxRDI[6]	Received value of bit 6 of the G1 octet.
1	x	RxRDI[7]	Received value of bit 7 of the G1 octet.
0	0	—	Reserved, set to 0.

0x14—RXK1 (Receive K1 Overhead Status Register) (WAN Only)

The RXK1 register provides K1 overhead status. The K1 and K2 bytes are allocated for Automatic Protection Switching (APS) signaling between Line level entities. These bytes are defined only for the first STS-1 of the STS-3c signal.

This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bit	Default	Name	Description
7	x	RxK1[1]	Receive value for K1 Overhead Octet—bit 1 (MSB)
6	x	RxK1[2]	Receive value for K1 Overhead Octet—bit 2
5	x	RxK1[3]	Receive value for K1 Overhead Octet—bit 3
4	x	RxK1[4]	Receive value for K1 Overhead Octet—bit 4
3	x	RxK1[5]	Receive value for K1 Overhead Octet—bit 5
2	x	RxK1[6]	Receive value for K1 Overhead Octet—bit 6
1	x	RxK1[7]	Receive value for K1 Overhead Octet—bit 7
0	x	RxK1[8]	Receive value for K1 Overhead Octet—bit 8 (LSB)

0x15—RXK2 (Receive K2 Overhead Status Register) (WAN Only)

The RXK2 register controls the K2 byte in the transport overhead. The K1 byte and bits 0–5 of the K2 byte are allocated for Automatic Protection Switching (APS) signaling between line level entities. These bytes are defined only for the first STS-1 of the STS-3c signal. This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bits 6–8 of the K2 byte are allocated for Alarm Indication Signal (AIS) and Remote Defect Indicator (RDI). These bytes are defined only for the first STS-1 of the STS-3c signal.

Bit	Default	Name	Description
7	x	RxK2[1]	Receive value for K2 Overhead Octet—bit 1 (MSB)
6	x	RxK2[2]	Receive value for K2 Overhead Octet—bit 2
5	x	RxK2[3]	Receive value for K2 Overhead Octet—bit 3
4	x	RxK2[4]	Receive value for K2 Overhead Octet—bit 4
3	x	RxK2[5]	Receive value for K2 Overhead Octet—bit 5
2	x	RxK2[6]	Receive value for K2 Overhead Octet—bit 6
1	x	RxK2[7]	Receive value for K2 Overhead Octet—bit 7
0	x	RxK2[8]	Receive value for K2 Overhead Octet—bit 8 (LSB)

0x6B—RXPTHBUF (Receive Path Trace Circular Buffer, J1)

The RXSECBUF buffer is used to receive repeatedly a 64-byte, fixed-length string so that a receiving terminal in a path can verify its continued connection to the intended transmitter.

Bit	Default	Name	Description
7	x	RxPthBuf[7]	Receive Path Trace Circular Buffer bit 7.
6	x	RxPthBuf[6]	Receive Path Trace Circular Buffer bit 6.
5	x	RxPthBuf[5]	Receive Path Trace Circular Buffer bit 5.
4	x	RxPthBuf[4]	Receive Path Trace Circular Buffer bit 4.
3	x	RxPthBuf[3]	Receive Path Trace Circular Buffer bit 3.
2	x	RxPthBuf[2]	Receive Path Trace Circular Buffer bit 2.
1	x	RxPthBuf[1]	Receive Path Trace Circular Buffer bit 1.
0	x	RxPthBuf[0]	Receive Path Trace Circular Buffer bit 0.

0x16—RXS1 (Receive S1 Overhead Status Register) (WAN Only)

The RXS1 register provides S1 overhead status. This byte is allocated for transporting synchronization status messages. This byte is defined only for the first STS-1 of the STS-3c signal. These messages provide an indication of the quality level of the synchronization source of the SONET signal.

This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bit	Default	Name	Description
7	x	RxS1[1]	Receive value for S1 Overhead Octet—bit 1 (MSB)
6	x	RxS1[2]	Receive value for S1 Overhead Octet—bit 2
5	x	RxS1[3]	Receive value for S1 Overhead Octet—bit 3
4	x	RxS1[4]	Receive value for S1 Overhead Octet—bit 4
3	x	RxS1[5]	Receive value for S1 Overhead Octet—bit 5
2	x	RxS1[6]	Receive value for S1 Overhead Octet—bit 6
1	x	RxS1[7]	Receive value for S1 Overhead Octet—bit 7
0	x	RxS1[8]	Receive value for S1 Overhead Octet—bit 8 (LSB)

0x6A—RXSECBUF (Receive Section Trace Circular Buffer)

The RXSECBUF buffer, the J0 byte, is used to receive repeatedly a 64-byte, fixed-length string so that a receiving terminal in a section can verify its continued connection to the intended transmitter. This buffer is also used as a Section trace for SDH.

Bit	Default	Name	Description
7	x	RxSecBuf[7]	Receive Section Trace Circular Buffer bit 7.
6	x	RxSecBuf[6]	Receive Section Trace Circular Buffer bit 6.
5	x	RxSecBuf[5]	Receive Section Trace Circular Buffer bit 5.
4	x	RxSecBuf[4]	Receive Section Trace Circular Buffer bit 4.
3	x	RxSecBuf[3]	Receive Section Trace Circular Buffer bit 3.
2	x	RxSecBuf[2]	Receive Section Trace Circular Buffer bit 2.
1	x	RxSecBuf[1]	Receive Section Trace Circular Buffer bit 1.
0	x	RxSecBuf[0]	Receive Section Trace Circular Buffer bit 0.

4.7 Status and Interrupt Registers

These registers contain status and interrupt information.

0x42—APSINT (APS Interrupt Indication Status Register) (WAN Only)

The APSINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	x	PSBFInt(2)	When a logic 1 is read, this bit indicates that a Protection Switching Byte Failure (PSBF) alarm interrupt has occurred.
3	0	—	Reserved, set to 0.
2	0	—	Reserved, set to 0.
1	x	SigFailInt(1)	When a logic 1 is read, this bit indicates that a Signal Fail interrupt has occurred.
0	x	SigDegradeInt(1)	When a logic 1 is read, this bit indicates that a Signal Degrade interrupt has occurred.

NOTE(S):
(1) Dual event—A 0–> 1 and 1–> 0 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.
(2) Single event—A 0 –> 1 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.

0x3A—ENAPS (APS Interrupt Mask Control Register) (WAN Only)

The ENAPS register controls which of the interrupts listed in the APSInt register (0x42) appear on the MInt* pin (pin 6), provided that EnAPSInt (bit 2) in the ENSUMINT register (0x34) is enabled, and EnIntPin (bit 6) in the GEN register (0x00) is enabled.

This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	1	EnPSBF	When written to a logic 1, this bit enables the Protection Switch Byte Failure (PSBF) Interrupt.
3	0	—	Reserved, set to 0.
2	0	—	Reserved, set to 0.
1	1	EnSigFail	When written to a logic 1, this bit enables the Signal Failure (SF) Interrupt.
0	1	EnSigDegrade	When written to a logic 1, this bit enables the Signal Degrade (SD) Interrupt.

0x39—ENCELLR (Receive Cell Interrupt Mask Control Register)

The ENCELLR register controls which of the interrupts listed in the RxCellInt register (0x41) appear on the MInt* pin (pin 6), provided that EnRxCellInt (bit 1) in the ENSUMINT register (0x34) is enabled, and EnIntPin (bit 6) in the GEN register (0x00) is enabled.

Bit	Default	Name	Description
7	1	EnLOCD	When written to a logic 1, this bit enables a Loss of Cell Delineation Interrupt. When enabled, the interrupt appears on the MInt* pin for the LOCD interrupt indication bit.
6	1	EnHECDet	When written to a logic 1, this bit enables a HEC Error Detected Interrupt. When enabled, the interrupt appears on the MInt* pin for the HECDet interrupt indication bit.
5	1	EnHECCorr	When written to a logic 1, this bit enables a HEC Error Corrected Interrupt. When enabled, the interrupt appears on the MInt* pin for the HECCorr interrupt indication bit.
4	0	—	Reserved, set to 0.
3	1	EnCellRcvd	When written to a logic 1, this bit enables a Cell Received Interrupt. When enabled, the interrupt appears on the MInt* pin for the CellRcvd interrupt indication bit.
2	1	EnIdleRcvd	When written to a logic 1, this bit enables an Idle Cell Received Interrupt. When enabled, the interrupt appears on the MInt* pin for the IdleRcvd interrupt indication bit.
1	1	EnNonMatch	When written to a logic 1, this bit enables a Non-matching Cell Received Interrupt. When enabled, the interrupt appears on the MInt* pin for the NonMatch interrupt indication bit.
0	1	EnNonZerGFC	When written to a logic 1, this bit enables a Non-0 GFC Received Interrupt. When enabled, the interrupt appears on the MInt* pin for the NonZerGFC interrupt indication bit.

0x38—ENCELLT (Transmit Cell Interrupt Mask Control Register)

The ENCELLT register controls which of the interrupts listed in the TxCellInt register (0x40) appear on the MInt* pin (pin 6), provided that EnTxCellInt (bit 0) in the ENSUMINT register (0x34) is enabled, and EnIntPin (bit 6) in the GEN register (0x00) is enabled.

Bit	Default	Name	Description
7	1	EnParErr	When written to a logic 1, this bit enables the Parity Error Interrupt. When enabled, the interrupt appears on the MInt* pin for the ParErr interrupt indication bit.
6	1	EnSOCErr	When written to a logic 1, this bit enables the Start of Cell Alignment Error Interrupt. When enabled, the interrupt appears on the MInt* pin for the SOCErr interrupt indication bit.
5	1	EnTxOvfl	When written to a logic 1, this bit enables the Transmit FIFO Overflow Interrupt. When enabled, the interrupt appears on the MInt* pin for the TxOvfl interrupt indication bit.
4	1	EnRxOvfl	When written to a logic 1, this bit enables the Receive FIFO Overflow Interrupt. When enabled, the interrupt appears on the MInt* pin for the RxOvfl interrupt indication bit.
3	1	EnCellSent	When written to a logic 1, this bit enables the Cell Sent Interrupt. When enabled, the interrupt appears on the MInt* pin for the CellSent interrupt indication bit.
2	0	—	Reserved, set to 0.
1	0	—	Reserved, set to 0.
0	0	—	Reserved, set to 0.

0x36—ENLIN (Receive Line Interrupt Mask Control Register)

The ENLIN register controls which of the interrupts listed in the LinInt register (0x3E) appear on the MInt* pin (pin 6), provided that EnLinInt (bit 6) in the ENSUMINT register (0x34) is enabled, and EnIntPin (bit 6) in the GEN register (0x00) is enabled.

Bit	Default	Name	Description
7	1	EnLOP	When written to a logic 1, this bit enables the LOP Interrupt.
6	1	EnK1K2	This bit is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255). When written to a logic 1, this bit enables the K1K2 Interrupt.
5	1	EnAIS-L	When written to a logic 1, this bit enables the AIS-L Interrupt.
4	1	EnRDI-L	When written to a logic 1, this bit enables the RDI-L Interrupt.
3	1	EnB2Err	When written to a logic 1, this bit enables the B2 Error Interrupt.
2	1	EnLnFEBE	When written to a logic 1, this bit enables the Line FEBE Error Interrupt.
1	0	—	Reserved, set to 0.
0	1	EnS1Intr	This bit is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255). When written to a logic 1, this bit enables the S1 Byte Change Interrupt.

0x37—ENPTH (Receive Path Interrupt Mask Control Register)

The ENPTH register controls which of the interrupts listed in the PthInt register (0x3F) appear on the MInt* pin (pin 6), provided that EnPthInt (bit 5) in the ENSUMINT register (0x34) is enabled, and EnIntPin (bit 6) in the GEN register (0x00) is enabled.

Bit	Default	Name	Description
7	1	EnAIS-P	When written to a logic 1, this bit enables the AIS-P Interrupt.
6	1	EnRDI-P	When written to a logic 1, this bit enables the RDI-P Interrupt.
5	1	EnB3Err	When written to a logic 1, this bit enables the B3 Error Interrupt.
4	1	EnPthFEBE	When written to a logic 1, this bit enables the Path FEBE Interrupt.
3	1	EnPLM-P	When written to a logic 1, this bit enables the Payload Label Mismatch-Path (PLM-P) Interrupt.
2	1	EnUneq-P	When written to a logic 1, this bit enables the STS Path Unequipped (Uneq-P) Interrupt.
1	1	EnPthTrace	When written to a logic 1, this bit enables the Path Trace Interrupt.
0	1	EnhanceRDI	When written to a logic 1, this bit enables the Enhanced RDI function. When written to 0, reduced RDI functionality detection is performed.

0x35—ENSEC (Receive Section Interrupt Mask Control Register)

The ENSEC register controls which of the interrupts listed in the SecInt register (0x3D) appear on the MInt* pin (pin 6), provided that EnSecInt (bit 7) in the ENSUMINT register (0x34) is enabled, and EnIntPin (bit 6) in the GEN register (0x00) is enabled.

Bit	Default	Name	Description
7	1	EnSigDet	When written to a logic 1, this bit enables the Signal Detect Interrupt.
6	1	EnLOL	When written to a logic 1, this bit enables the Loss of Lock Interrupt.
5	1	EnLOS	When written to a logic 1, this bit enables the Loss of Signal Interrupt.
4	1	EnOOF	When written to a logic 1, this bit enables the Out of Frame Interrupt.
3	1	EnLOF	When written to a logic 1, this bit enables the Loss of Frame Interrupt.
2	1	EnB1Err	When written to a logic 1, this bit enables the Section BIP Error Interrupt.
1	1	EnSecTrace	When written to a logic 1, this bit enables the Section Trace Interrupt.
0	0	DisRxScr	When written to a logic 1, this bit disables the Receive Frame Scrambler. When written to 0, scrambling is enabled.

0x34—ENSUMINT (Summary Interrupt Mask Control Register)

The ENSUMINT register determines which of the interrupts listed in register 0x3C (SUMINT) are observed on the MInt* (pin 6).

Bit	Default	Name	Description
7	1	EnSecInt	When written to a logic 1, this bit enables the SONET Section Overhead interrupt. It is a global disable for the SONET Section interrupt sources.
6	1	EnLinInt	When written to a logic 1, this bit enables the SONET Line Overhead interrupt. It is a global disable for the SONET Line interrupt sources.
5	1	EnPthInt	When written to a logic 1, this bit enables the SONET Path Overhead interrupt. It is a global disable for the SONET Path interrupt sources.
4	1	EnOneSecInt	When written to a logic 1, this bit enables the One Second Interrupt generated by the OneSecIn pin (pin 33) to appear on the MInt* output pin.
3	0	—	Reserved, set to 0.
2	1	EnAPSInt (WAN Only)	When written to a logic 1, this bit enables the APS interrupt. It is a global disable for the APS interrupt sources. Set to 0 in LAN parts.
1	1	EnRxCellInt	When written to a logic 1, this bit enables the Receive Cell Interrupt. It is a global disable for the RxCellInt interrupt sources.
0	1	EnTxCellInt	When written to a logic 1, this bit enables the Transmit Cell Interrupt. It is a global disable for the TxCellInt interrupt sources.

0x3E—LININT (Receive Line Interrupt Indication Status Register)

The LININT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	LOPInt(1)	When a logic 1 is read, this bit indicates that a LOP Interrupt has occurred.
6	x	K1K2Int(2)	This bit is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255). When a logic 1 is read, this bit indicates that a K1/K2 Interrupt has occurred.
5	x	AIS-Lint(1)	When a logic 1 is read, this bit indicates that a AIS-L Interrupt has occurred.
4	x	RDI-Lint(1)	When a logic 1 is read, this bit indicates that a RDI-L Interrupt has occurred.
3	x	B2ErrInt(2)	When a logic 1 is read, this bit indicates that a B2 Error Interrupt has occurred.
2	x	LnFEBEInt(2)	When a logic 1 is read, this bit indicates that a Line BIP Error Interrupt has occurred.
1	0	—	Reserved, set to 0.
0	x	S1Intr2	This bit is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255). When a logic 1 is read, this bit indicates that an S1 Byte Change Interrupt has occurred.

NOTE(S):
(1) Dual event—Either a 0 –> 1 or a 1 –> 0 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.
(2) Single event—A 0 –> 1 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.

0x3F—PTHINT (Receive Path Interrupt Indication Status Register)

The PTHINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	AIS-PInt(1)	When a logic 1 is read, this bit indicates that an AIS-P Interrupt has occurred.
6	x	RDI-PInt(1)	When a logic 1 is read, this bit indicates that an RDI-P Interrupt has occurred.
5	x	B3ErrInt(2)	When a logic 1 is read, this bit indicates that a B3 Error Interrupt has occurred.
4	x	PthFEBEInt(2)	When a logic 1 is read, this bit indicates that a Path FEBE Interrupt has occurred.
3	x	PLM-PInt(1)	When a logic 1 is read, this bit indicates that a PLM-P Interrupt has occurred. This means that the contents of Path Overhead byte C2 is not equal to 13 hex for ATM mapping.
2	x	Uneq-PInt(1)	When a logic 1 is read, this bit indicates that an Uneq-P Interrupt has occurred. This means that the contents of Path Overhead byte C2 is equal to 0.
1	x	PthTraceInt(2)	When a logic 1 is read, this bit indicates that a Path Trace Interrupt has occurred.
0	0	—	Reserved, set to 0.

NOTE(S):
(1) Dual event—A 0 –> 1 and 1–> 0 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.
(2) Single event—A 0 –> 1 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.

0x4A—RXAPS (Receive APS Status Register) (WAN Only)

The RXAPS register contains status information for the receiver APS functions.

This register is active only in the WAN parts (RS8250 and RS8254). It is set to 0 and disabled in the LAN parts (RS8251 and RS8255).

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	x	PSBF(2)	When a logic 1 is read, this bit indicates a Protection Byte Switching Failure (PSBF).
3	0	—	Reserved, set to 0.
2	0	—	Reserved, set to 0.
1	x	SigFail(1)	When a logic 1 is read, this bit indicates a Signal Failure (SF).
0	x	SigDegrade(1)	When a logic 1 is read, this bit indicates a Signal Degradation (SD).

NOTE(S):
(1) This status reflects the current state of the circuit.
(2) This status shows an event that has occurred since the register was last read.

0x49—RXCELL (Receive Cell Status Register)

The RXCELL register contains status for the cell alignment, header error correction, and header screening functions in the cell receiver.

Bit	Default	Name	Description
7	x	LOCD(1)	When a logic 1 is read, this bit indicates that there is a Loss of Cell Delineation.
6	x	HECDet(2)	When a logic 1 is read, this bit indicates that an uncorrected HEC Error was detected.
5	x	HECCorr(2)	When a logic 1 is read, this bit indicates that a HEC Error was corrected.
4	0	—	Reserved, set to 0.
3	x	CellRcvd(2)	When a logic 1 is read, this bit indicates that a cell with a header matching the receive header value and mask criteria was received.
2	x	IdleRcvd(2)	When a logic 1 is read, this bit indicates that a cell with a header matching the receive idle cell header value and mask criteria was received.
1	x	NonMatch(2)	When a logic 1 is read, this bit indicates that a cell with a header not matching either the receive cell or idle cell criteria was received.
0	x	NonZerGFC(2)	When a logic 1 is read, this bit indicates that a cell with a Non-zero GFC field in the header was received.

NOTE(S):
(1) This status reflects the current state of the circuit.
(2) This status shows an event that has occurred since the register was last read.

0x41—RXCELLINT (Receive Cell Interrupt Indication Status Register)

The RXCELLINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	LOCDInt(1)	When a logic 1 is read, this bit indicates that a Loss of Cell Delineation has occurred.
6	x	HECDetInt(2)	When a logic 1 is read, this bit indicates that a HEC Error has been detected.
5	x	HECCorrInt(2)	When a logic 1 is read, this bit indicates that a HEC Error has been corrected.
4	0	—	Reserved, set to 0.
3	x	CellRcvdInt(2)	When a logic 1 is read, this bit indicates that a Cell Received Interrupt has occurred.
2	x	IdleRcvdInt(2)	When a logic 1 is read, this bit indicates that an Idle Cell Received Interrupt has occurred.
1	x	NonMatchInt(2)	When a logic 1 is read, this bit indicates that a Non-matching Cell Received Interrupt has occurred.
0	x	NonZerGFCInt(2)	When a logic 1 is read, this bit indicates that a Non-zero GFC Received Interrupt has occurred.

NOTE(S):
(1) Dual event—Either a 0–> 1 or a 1 –> 0 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.
(2) Single event—A 0–> 1 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.

0x46—RXLIN (Receive Line Overhead Status Register)

The RXLIN register contains status information for the receiver Line Overhead.

Bit	Default	Name	Description
7	x	LOP(1)	When a logic 1 is read, this bit indicates that a Loss of Pointer condition exists.
6	x	K1K2(2)	When a logic 1 is read, this bit indicates that an K1K2 Value Change was received.
5	x	AIS-L(1)	When a logic 1 is read, this bit indicates that an AIS-L condition exists.
4	x	RDI-L(1)	When a logic 1 is read, this bit indicates that an RDI-L condition exists.
3	x	B2Err(2)	When a logic 1 is read, this bit indicates that a Line BIP Error was received.
2	x	LnFEBE(2)	When a logic 1 is read, this bit indicates that a Line FEBE Error was received.
1	0	EnRxLinDL	When written to a logic 1, this bit enables the Receive D4-12 bytes of the Data Link.
0	0	EnRxSecDL	When written to a logic 1, this bit enables the Receive D1/D2/D3 bytes of the Data Link.

NOTE(S):
(1) This status reflects the current state of the circuit.
(2) This status shows an event that has occurred since the register was last read.

0x47—RXPTH (Receive Path Overhead Status Register)

The RXPTH register contains status information for the receiver Path Overhead.

Bit	Default	Name	Description
7	x	AIS-P(1)	When a logic 1 is read, this bit indicates that an AIS-P condition exists.
6	x	RDI-P(1)	When a logic 1 is read, this bit indicates that an RDI-P condition exists.
5	x	B3Err(2)	When a logic 1 is read, this bit indicates that a B3 Error was received.
4	x	PthFEBE(2)	When a logic 1 is read, this bit indicates that a Path FEBE Error was received.
3	x	PLM-P(1)	When a logic 1 is read, this bit indicates that a PLM-P condition exists.
2	x	Uneq-P(1)	When a logic 1 is read, this bit indicates that a Uneq-P condition exists.
1	0	—	Reserved, set to 0.
0	0	—	Reserved, set to 0.

NOTE(S):
(1) This status reflects the current state of the circuit.
(2) This status shows an event that has occurred since the register was last read.

0x45—RXSEC (Receive Section Overhead Status Register)

The RXSEC register provides section overhead status.

Bit	Default	Name	Description
7	x	SigDet(1)	When a logic 1 is read, this bit indicates that a Signal Detect condition exists on the LSigDet input pin (pin 56).
6	x	LOL(1)	When a logic 1 is read, this bit indicates that a Loss of Lock condition exists.
5	x	LOS(1)	When a logic 1 is read, this bit indicates that a Loss of Signal condition exists.
4	x	OOF(1)	When a logic 1 is read, this bit indicates that an Out of Frame condition exists.
3	x	LOF(1)	When a logic 1 is read, this bit indicates that a Loss of Frame condition exists.
2	x	B1Err(2)	When a logic 1 is read, this bit indicates that a Section BIP Error was received.
1	0	RxFrmPulOut	This bit selects the type of output sent to the RxFrameRef pin (pin 36). When written to a logic 1, the receive octet clock (19.44 MHz) is present. When written to a logic 0, a Receive Frame Pulse (8 kHz) is present.
0	0	RxFrmPulPol	This bit selects the polarity of the RxFrameRef output pin (pin 36). When written to a logic 1, the frame pulse output is an active high. When written to 0, the frame pulse output is an active low.

NOTE(S):
(1) This status reflects the current state of the circuit.
(2) This status shows an event that has occurred since the register was last read.

0x3D—SECINT (Receive Section Interrupt Indication Status Register)

The SECINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	SigDetInt(1)	When a logic 1 is read, this bit indicates that a Signal Detect Interrupt has occurred.
6	x	LOLInt(1)	When a logic 1 is read, this bit indicates that a Loss of Lock Interrupt has occurred.
5	x	LOSInt(1)	When a logic 1 is read, this bit indicates that a Loss of Signal Interrupt has occurred.
4	x	OOFInt(1)	When a logic 1 is read, this bit indicates that a Out of Frame Interrupt has occurred.
3	x	LOFInt(1)	When a logic 1 is read, this bit indicates that a Loss of Frame Interrupt has occurred.
2	x	B1ErrInt(2)	When a logic 1 is read, this bit indicates that a Section BIP Error Interrupt has occurred.
1	x	SecTraceInt(2)	When a logic 1 is read, this bit indicates that a Section Trace Interrupt has occurred.
0	0	—	Reserved, set to 0.

NOTE(S):
(1) Dual event—Either a 0–> 1 or a 1 –> 0 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.
(2) Single event—A 0–> 1 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.

0x3C—SUMINT (Summary Interrupt Indication Status Register)

The SUMINT register indicates data link interrupts, one-second interrupts, and additional summary interrupts.

Bit	Default	Name	Description
7	x	SecInt(2)	When a logic 1 is read, this bit indicates a SONET Section Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication has occurred in the SECINT register (0x3D).
6	x	LinInt(2)	When a logic 1 is read, this bit indicates a SONET Line Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication has occurred in the LININT register (0x3E).
5	x	PthInt(2)	When a logic 1 is read, this bit indicates a SONET Path Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication has occurred in the PTHINT register (0x3F).
4	x	OneSecInt(1)	When a logic 1 is read, this bit indicates a One Second Interrupt. This interrupt signifies that a rising edge occurred on the OneSecIn pin (pin 33). The interrupt is generated for each rising edge on the OneSecIn pin and is cleared upon a read of this status register.
3	0	—	Reserved, set to 0.
2	x	APSInt(2) (WAN Only)	When a logic 1 is read, this bit indicates an APS Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication has occurred in the APSINT register (0x42). Set this bit to 0 on LAN parts.
1	x	RxCellInt(2)	When a logic 1 is read, this bit indicates a Receive Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication has occurred in the Receive Cell Indication Register (0x41).
0	x	TxCellInt(2)	When a logic 1 is read, this bit indicates a Transmit Cell/UTOPIA Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication has occurred in the Transmit Cell Indication Register (0x40).

NOTE(S):

(1) Single event—A 0–> 1 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

(2) These bits are summary indications of any interrupt events set in the indicated registers. These bits can serve as direction to which status registers need to be read next. These bits are cleared when the interrupt bits in the indicated individual interrupt registers are read and cleared.

0x48—TXCELL (Transmit Cell Status Register)

The TXCELL register contains status for the cell transmitter and the UTOPIA interface.

Bit	Default	Name	Description
7	x	ParErr(1)	When a logic 1 is read, this bit indicates that a parity error was received on the transmit UTOPIA input data octet.
6	x	SOCErr(1)	When a logic 1 is read, this bit indicates that a Start of Cell Alignment Error was received on the UTxSOC input pin.
5	x	TxOvfl(1)	When a logic 1 is read, this bit indicates that a Transmit FIFO Overflow condition occurred in the transmit UTOPIA FIFO.
4	x	RxOvfl(1)	When a logic 1 is read, this bit indicates that a Receive FIFO Overflow condition occurred in the receive UTOPIA FIFO.
3	x	CellSent(1)	When a logic 1 is read, this bit indicates that a non-idle cell was formatted and transmitted from the UTOPIA interface.
2	0	—	Reserved, set to 0.
1	0	—	Reserved, set to 0.
0	0	—	Reserved, set to 0.

NOTE(S):
(1) This status shows an event that has occurred since the register was last read.

0x40—TXCELLINT (Transmit Cell Interrupt Indication Status Register)

The TXCELLINT register indicates that a change of status has occurred within its affiliated status signals.

Bit	Default	Name	Description
7	x	ParErrInt(1)	When a logic 1 is read, this bit indicates that a Parity Error has occurred.
6	x	SOCErrInt(1)	When a logic 1 is read, this bit indicates that a Start of Cell Alignment Error has occurred.
5	x	TxOvflInt(1)	When a logic 1 is read, this bit indicates that a Transmit FIFO Overflow has occurred.
4	x	RxOvflInt(1)	When a logic 1 is read, this bit indicates that a Receive FIFO Overflow has occurred.
3	x	CellSentInt(1)	When a logic 1 is read, this bit indicates that a Cell Sent Interrupt has occurred.
2	0	—	Reserved, set to 0.
1	0	—	Reserved, set to 0.
0	0	—	Reserved, set to 0.

NOTE(S):
(1) Single event—A 0–> 1 transition on the corresponding status bit causes this interrupt to occur provided that this interrupt has been enabled by the corresponding enable bit. Reading the interrupt register clears the interrupt.

4.8 Counters

This section describes the RS825x's 12 counters. When the counters fill, they saturate and do not roll over. The counts have been sized such that they will not saturate within a one-second interval. Therefore, when one-second latching is enabled, the counters will be read and cleared before they can saturate.

0x55—B1CNTH (Section BIP Error Counter [High Byte])

The B1CNTH counter tracks the number of Section BIP errors.

Bit	Default	Name	Description
7	x	B1Cnt[15]	Section BIP Error counter bit 15 (MSB).
6	x	B1Cnt[14]	Section BIP Error counter bit 14.
5	x	B1Cnt[13]	Section BIP Error counter bit 13.
4	x	B1Cnt[12]	Section BIP Error counter bit 12.
3	x	B1Cnt[11]	Section BIP Error counter bit 11.
2	x	B1Cnt[10]	Section BIP Error counter bit 10.
1	x	B1Cnt[9]	Section BIP Error counter bit 9.
0	x	B1Cnt[8]	Section BIP Error counter bit 8.

0x54—B1CNTL (Section BIP Error Counter [Low Byte])

The B1CNTL counter tracks the number of Section BIP errors.

Bit	Default	Name	Description
7	x	B1Cnt[7]	Section BIP Error counter bit 7.
6	x	B1Cnt[6]	Section BIP Error counter bit 6.
5	x	B1Cnt[5]	Section BIP Error counter bit 5.
4	x	B1Cnt[4]	Section BIP Error counter bit 4.
3	x	B1Cnt[3]	Section BIP Error counter bit 3.
2	x	B1Cnt[2]	Section BIP Error counter bit 2.
1	x	B1Cnt[1]	Section BIP Error counter bit 1.
0	x	B1Cnt[0]	Section BIP Error counter bit 0 (LSB).

0x52—B2CNTH (Line BIP Error Counter [High Byte])

The B2CNTH counter tracks the number of Line BIP errors.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	0	—	Reserved, set to 0.
3	0	—	Reserved, set to 0.
2	0	—	Reserved, set to 0.
1	x	B2Cnt[17]	Line BIP Error counter bit 17 (MSB).
0	x	B2Cnt[16]	Line BIP Error counter bit 16.

0x50—B2CNTL (Line BIP Error Counter [Low Byte])

The B2CNTL counter tracks the number of Line BIP errors.

Bit	Default	Name	Description
7	x	B2Cnt[7]	Line BIP Error counter bit 7.
6	x	B2Cnt[6]	Line BIP Error counter bit 6.
5	x	B2Cnt[5]	Line BIP Error counter bit 5.
4	x	B2Cnt[4]	Line BIP Error counter bit 4.
3	x	B2Cnt[3]	Line BIP Error counter bit 3.
2	x	B2Cnt[2]	Line BIP Error counter bit 2.
1	x	B2Cnt[1]	Line BIP Error counter bit 1.
0	x	B2Cnt[0]	Line BIP Error counter bit 0 (LSB).

0x51—B2CNTM (Line BIP Error Counter [Mid Byte])

The B2CNTM counter tracks the number of Line BIP errors.

Bit	Default	Name	Description
7	x	B2Cnt[15]	Line BIP Error counter bit 15.
6	x	B2Cnt[14]	Line BIP Error counter bit 14.
5	x	B2Cnt[13]	Line BIP Error counter bit 13.
4	x	B2Cnt[12]	Line BIP Error counter bit 12.
3	x	B2Cnt[11]	Line BIP Error counter bit 11.
2	x	B2Cnt[10]	Line BIP Error counter bit 10.
1	x	B2Cnt[9]	Line BIP Error counter bit 9.
0	x	B2Cnt[8]	Line BIP Error counter bit 8.

0x57—B3CNTH (Path BIP Error Counter [High Byte])

The B3CNTH counter tracks the number of Path BIP errors.

Bit	Default	Name	Description
7	x	B3Cnt[15]	Path BIP Error counter bit 15 (MSB).
6	x	B3Cnt[14]	Path BIP Error counter bit 14.
5	x	B3Cnt[13]	Path BIP Error counter bit 13.
4	x	B3Cnt[12]	Path BIP Error counter bit 12.
3	x	B3Cnt[11]	Path BIP Error counter bit 11.
2	x	B3Cnt[10]	Path BIP Error counter bit 10.
1	x	B3Cnt[9]	Path BIP Error counter bit 9.
0	x	B3Cnt[8]	Path BIP Error counter bit 8.

0x56—B3CNTL (Path BIP Error Counter [Low Byte])

The B3CNTL counter tracks the number of Path BIP errors.

Bit	Default	Name	Description
7	x	B3Cnt[7]	Path BIP Error counter bit 7.
6	x	B3Cnt[6]	Path BIP Error counter bit 6.
5	x	B3Cnt[5]	Path BIP Error counter bit 5.
4	x	B3Cnt[4]	Path BIP Error counter bit 4.
3	x	B3Cnt[3]	Path BIP Error counter bit 3.
2	x	B3Cnt[2]	Path BIP Error counter bit 2.
1	x	B3Cnt[1]	Path BIP Error counter bit 1.
0	x	B3Cnt[0]	Path BIP Error counter bit 0 (LSB).

0x4D—CORRCNT (Corrected HEC Error Counter)

The CORRCNT counter tracks the number of corrected HEC errors.

Bit	Default	Name	Description
7	x	CorrCnt[7]	Corrected HEC Error counter bit 7 (MSB).
6	x	CorrCnt[6]	Corrected HEC Error counter bit 6.
5	x	CorrCnt[5]	Corrected HEC Error counter bit 5.
4	x	CorrCnt[4]	Corrected HEC Error counter bit 4.
3	x	CorrCnt[3]	Corrected HEC Error counter bit 3.
2	x	CorrCnt[2]	Corrected HEC Error counter bit 2.
1	x	CorrCnt[1]	Corrected HEC Error counter bit 1.
0	x	CorrCnt[0]	Corrected HEC Error counter bit 0 (LSB).

0x5A—LFCNTH (Line FEBE Error Counter [High Byte])

The LFCNTH counter tracks the number of Line FEBE errors.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	0	—	Reserved, set to 0.
3	0	—	Reserved, set to 0.
2	0	—	Reserved, set to 0.
1	x	LFCnt[17]	Line FEBE Error counter bit 17 (MSB).
0	x	LFCnt[16]	Line FEBE Error counter bit 16.

0x58—LFCNTL (Line FEBE Error Counter [Low Byte])

The LFCNTL counter tracks the number of Line FEBE errors.

Bit	Default	Name	Description
7	x	LFCnt[7]	Line FEBE Error counter bit 7.
6	x	LFCnt[6]	Line FEBE Error counter bit 6.
5	x	LFCnt[5]	Line FEBE Error counter bit 5.
4	x	LFCnt[4]	Line FEBE Error counter bit 4.
3	x	LFCnt[3]	Line FEBE Error counter bit 3.
2	x	LFCnt[2]	Line FEBE Error counter bit 2.
1	x	LFCnt[1]	Line FEBE Error counter bit 1.
0	x	LFCnt[0]	Line FEBE Error counter bit 0 (LSB).

0x59—LFCNTM (Line FEBE Error Counter [Mid Byte])

The LFCNTM counter tracks the number of Line FEBE errors.

Bit	Default	Name	Description
7	x	LFCnt[15]	Line FEBE Error counter bit 15.
6	x	LFCnt[14]	Line FEBE Error counter bit 14.
5	x	LFCnt[13]	Line FEBE Error counter bit 13.
4	x	LFCnt[12]	Line FEBE Error counter bit 12.
3	x	LFCnt[11]	Line FEBE Error counter bit 11.
2	x	LFCnt[10]	Line FEBE Error counter bit 10.
1	x	LFCnt[9]	Line FEBE Error counter bit 9.
0	x	LFCnt[8]	Line FEBE Error counter bit 8.

0x4C—LOCDCNT (LOCD Event Counter)

The LOCDCNT counter tracks the number of LOCD events.

Bit	Default	Name	Description
7	x	LOCDCnt[7]	LOCD Event counter bit 7 (MSB).
6	x	LOCDCnt[6]	LOCD Event counter bit 6.
5	x	LOCDCnt[5]	LOCD Event counter bit 5.
4	x	LOCDCnt[4]	LOCD Event counter bit 4.
3	x	LOCDCnt[3]	LOCD Event counter bit 3.
2	x	LOCDCnt[2]	LOCD Event counter bit 2.
1	x	LOCDCnt[1]	LOCD Event counter bit 1.
0	x	LOCDCnt[0]	LOCD Event counter bit 0 (LSB).

0x4F—OOFCNT (OOF Event Counter)

The OOFCNT counter tracks the number OOF events.

Bit	Default	Name	Description
7	x	OOFCnt[7]	OOF Event counter bit 7 (MSB).
6	x	OOFCnt[6]	OOF Event counter bit 6.
5	x	OOFCnt[5]	OOF Event counter bit 5.
4	x	OOFCnt[4]	OOF Event counter bit 4.
3	x	OOFCnt[3]	OOF Event counter bit 3.
2	x	OOFCnt[2]	OOF Event counter bit 2.
1	x	OOFCnt[1]	OOF Event counter bit 1.
0	x	OOFCnt[0]	OOF Event counter bit 0 (LSB).

0x5D—PFCNTH (Path FEBE Error Counter [High Byte])

The PFCNTH counter tracks the number of Path FEBE errors.

Bit	Default	Name	Description
7	x	PFCnt[15]	Path FEBE Error counter bit 15 (MSB).
6	x	PFCnt[14]	Path FEBE Error counter bit 14.
5	x	PFCnt[13]	Path FEBE Error counter bit 13.
4	x	PFCnt[12]	Path FEBE Error counter bit 12.
3	x	PFCnt[11]	Path FEBE Error counter bit 11.
2	x	PFCnt[10]	Path FEBE Error counter bit 10.
1	x	PFCnt[9]	Path FEBE Error counter bit 9.
0	x	PFCnt[8]	Path FEBE Error counter bit 8.

0x5C—PFCNTL (Path FEBE Error Counter [Low Byte])

The PFCNTL counter tracks the number of Path FEBE errors.

Bit	Default	Name	Description
7	x	PFCnt[7]	Path FEBE Error counter bit 7.
6	x	PFCnt[6]	Path FEBE Error counter bit 6.
5	x	PFCnt[5]	Path FEBE Error counter bit 5.
4	x	PFCnt[4]	Path FEBE Error counter bit 4.
3	x	PFCnt[3]	Path FEBE Error counter bit 3.
2	x	PFCnt[2]	Path FEBE Error counter bit 2.
1	x	PFCnt[1]	Path FEBE Error counter bit 1.
0	x	PFCnt[0]	Path FEBE Error counter bit 0 (LSB).

0x5F—NONCNTH (Non-matching Cell Counter [High Byte])

The NONCNTH counter tracks the number of non-matching cells.

Bit	Default	Name	Description
7	x	NonCnt[15]	Non-matching cell counter bit 15 (MSB).
6	x	NonCnt[14]	Non-matching cell counter bit 14.
5	x	NonCnt[13]	Non-matching cell counter bit 13.
4	x	NonCnt[12]	Non-matching cell counter bit 12.
3	x	NonCnt[11]	Non-matching cell counter bit 11.
2	x	NonCnt[10]	Non-matching cell counter bit 10.
1	x	NonCnt[9]	Non-matching cell counter bit 9.
0	x	NonCnt[8]	Non-matching cell counter bit 8.

0x5E—NONCNTL (Non-matching Cell Counter [Low Byte])

The NONCNTL counter tracks the number of non-matching cells.

Bit	Default	Name	Description
7	x	NonCnt[7]	Non-matching cell counter bit 7.
6	x	NonCnt[6]	Non-matching cell counter bit 6.
5	x	NonCnt[5]	Non-matching cell counter bit 5.
4	x	NonCnt[4]	Non-matching cell counter bit 4.
3	x	NonCnt[3]	Non-matching cell counter bit 3.
2	x	NonCnt[2]	Non-matching cell counter bit 2.
1	x	NonCnt[1]	Non-matching cell counter bit 1.
0	x	NonCnt[0]	Non-matching cell counter bit 0 (LSB).

0x66—RXCNTH (Received Cell Counter [High Byte])

The RXCNTH counter tracks the number of received cells.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	0	—	Reserved, set to 0.
3	0	—	Reserved, set to 0.
2	x	RxCnt[18]	Received cell counter bit 18 (MSB).
1	x	RxCnt[17]	Received cell counter bit 17.
0	x	RxCnt[16]	Received cell counter bit 16.

0x64—RXCNTL (Received Cell Counter [Low Byte])

The RXCNTL counter tracks the number of received cells.

Bit	Default	Name	Description
7	x	RxCnt[7]	Received cell counter bit 7.
6	x	RxCnt[6]	Received cell counter bit 6.
5	x	RxCnt[5]	Received cell counter bit 5.
4	x	RxCnt[4]	Received cell counter bit 4.
3	x	RxCnt[3]	Received cell counter bit 3.
2	x	RxCnt[2]	Received cell counter bit 2.
1	x	RxCnt[1]	Received cell counter bit 1.
0	x	RxCnt[0]	Received cell counter bit 0 (LSB).

0x65—RXCNTM (Received Cell Counter [Mid Byte])

The RXCNTM register tracks the number of received cells.

Bit	Default	Name	Description
7	x	RxCnt[15]	Received cell counter bit 15.
6	x	RxCnt[14]	Received cell counter bit 14.
5	x	RxCnt[13]	Received cell counter bit 13.
4	x	RxCnt[12]	Received cell counter bit 12.
3	x	RxCnt[11]	Received cell counter bit 11.
2	x	RxCnt[10]	Received cell counter bit 10.
1	x	RxCnt[9]	Received cell counter bit 9.
0	x	RxCnt[8]	Received cell counter bit 8.

0x62—TXCNTH (Transmitted Cell Counter [High Byte])

The TXCNTH counter tracks the number of transmitted cells.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	—	Reserved, set to 0.
5	0	—	Reserved, set to 0.
4	0	—	Reserved, set to 0.
3	0	—	Reserved, set to 0.
2	x	TxCnt[18]	Transmitted cell counter bit 18 (MSB).
1	x	TxCnt[17]	Transmitted cell counter bit 17.
0	x	TxCnt[16]	Transmitted cell counter bit 16.

0x60—TXCNTL (Transmitted Cell Counter [Low Byte])

The TXCNTL counter tracks the number of transmitted cells.

Bit	Default	Name	Description
7	x	TxCnt[7]	Transmitted cell counter bit 7.
6	x	TxCnt[6]	Transmitted cell counter bit 6.
5	x	TxCnt[5]	Transmitted cell counter bit 5.
4	x	TxCnt[4]	Transmitted cell counter bit 4.
3	x	TxCnt[3]	Transmitted cell counter bit 3.
2	x	TxCnt[2]	Transmitted cell counter bit 2.
1	x	TxCnt[1]	Transmitted cell counter bit 1.
0	x	TxCnt[0]	Transmitted cell counter bit 0 (LSB).

0x61—TXCNTM (Transmitted Cell Counter [Mid Byte])

The TXCNTM counter tracks the number of transmitted cells.

Bit	Default	Name	Description
7	x	TxCnt[15]	Transmitted cell counter bit 15.
6	x	TxCnt[14]	Transmitted cell counter bit 14.
5	x	TxCnt[13]	Transmitted cell counter bit 13.
4	x	TxCnt[12]	Transmitted cell counter bit 12.
3	x	TxCnt[11]	Transmitted cell counter bit 11.
2	x	TxCnt[10]	Transmitted cell counter bit 10.
1	x	TxCnt[9]	Transmitted cell counter bit 9.
0	x	TxCnt[8]	Transmitted cell counter bit 8.

0x4E—UNCCNT (Uncorrected HEC Error Counter)

The UNCCNT counter tracks the number of uncorrected HEC errors.

Bit	Default	Name	Description
7	x	UncCnt[7]	Uncorrected HEC Error counter bit 7 (MSB).
6	x	UncCnt[6]	Uncorrected HEC Error counter bit 6.
5	x	UncCnt[5]	Uncorrected HEC Error counter bit 5.
4	x	UncCnt[4]	Uncorrected HEC Error counter bit 4.
3	x	UncCnt[3]	Uncorrected HEC Error counter bit 3.
2	x	UncCnt[2]	Uncorrected HEC Error counter bit 2.
1	x	UncCnt[1]	Uncorrected HEC Error counter bit 1.
0	x	UncCnt[0]	Uncorrected HEC Error counter bit 0 (LSB).

5.0 Electrical and Mechanical Specifications

This chapter describes the electrical and mechanical aspects of the RS825x. Included are timing diagrams, absolute maximum ratings, DC characteristics, and mechanical drawings.

5.1 Timing Specifications

This section provides timing diagrams and descriptions for the various interfaces of the RS825x. Table 5-1 describes the different types of timing relationships that appear in the timing diagrams. The timing relationship labels are numbered when they occur more than once in a diagram so that each label is unique. This numbering aids in identifying the appropriate label in Table 5-1. Signals are measured at the 50% point of the changing edge except for those involving high impedance transitions which are measured at 10% and 90%.

Table 5-1. Timing Diagram Nomenclature *(1 of 3)*

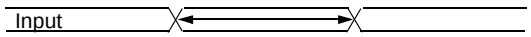
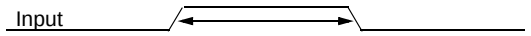
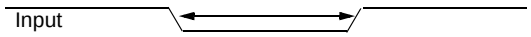
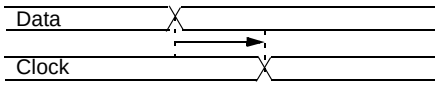
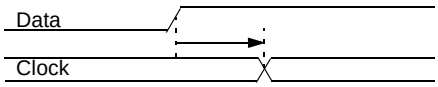
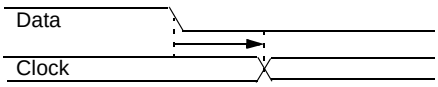
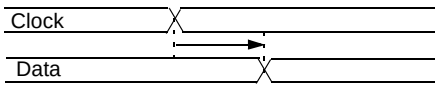
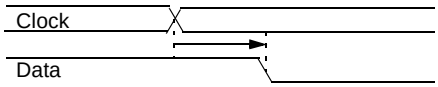
Symbol	Timing Relationship	Waveform
t_{pw}	Pulse Width	
t_{pwh}	Pulse Width High	
t_{pwl}	Pulse Width Low	
t_s	Setup Time	
t_{sh}	Setup High Time	
t_{sl}	Setup Low Time	
t_h	Hold Time	
t_{hh}	Hold High Time	

Table 5-1. Timing Diagram Nomenclature *(2 of 3)*

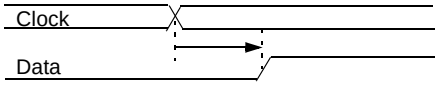
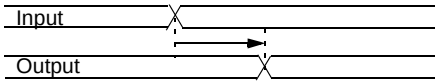
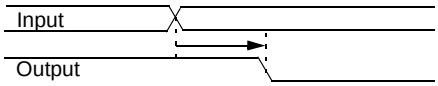
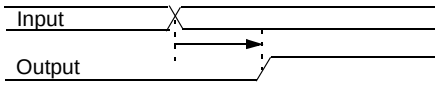
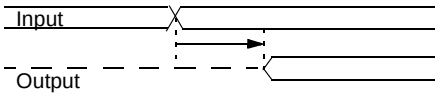
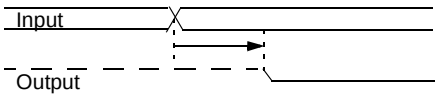
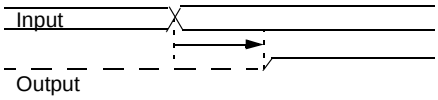
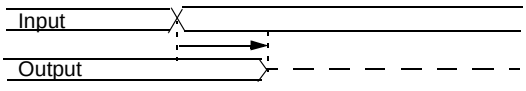
Symbol	Timing Relationship	Waveform
t_{hl}	Hold Low Time	
t_{pd}	Propagation Delay	
t_{pdhl}	Propagation Delay - High-to-Low	
t_{pdlh}	Propagation Delay - Low-to-High	
t_{en}	Enable Time	
t_{enzl}	Enable Time - High-impedance to Low Enable	
t_{enzh}	Enable Time - High-impedance to High Enable	
t_{dis}	Disable Time	

Table 5-1. Timing Diagram Nomenclature *(3 of 3)*

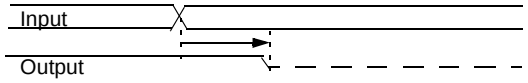
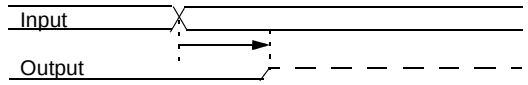
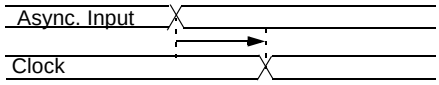
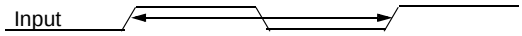
Symbol	Timing Relationship	Waveform
t_{dishz}	Disable Time - High Disable	
t_{dislz}	Disable Time - Low Disable	
t_{rec}	Recovery Time	
t_{per}	Period	
t_{cyc}	Cycle Time	—
f_{max}	Maximum Frequency	—
f_{min}	Minimum Frequency	—

Figure 5-1 illustrates how input waveforms are defined.

Figure 5-1. Input Waveform

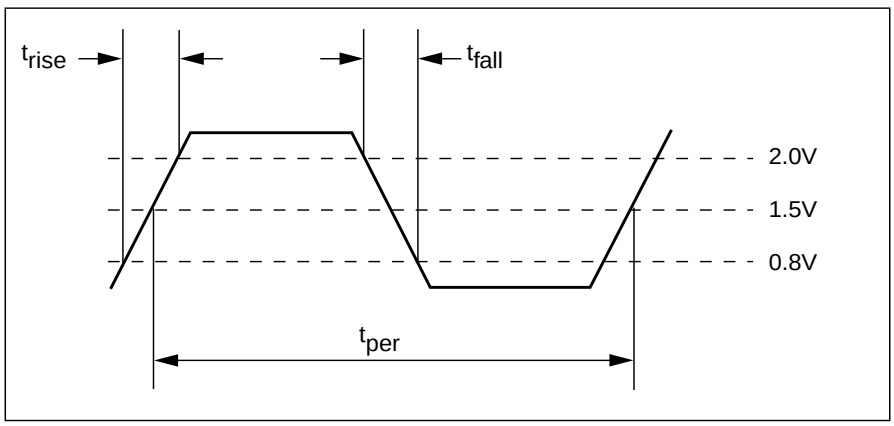
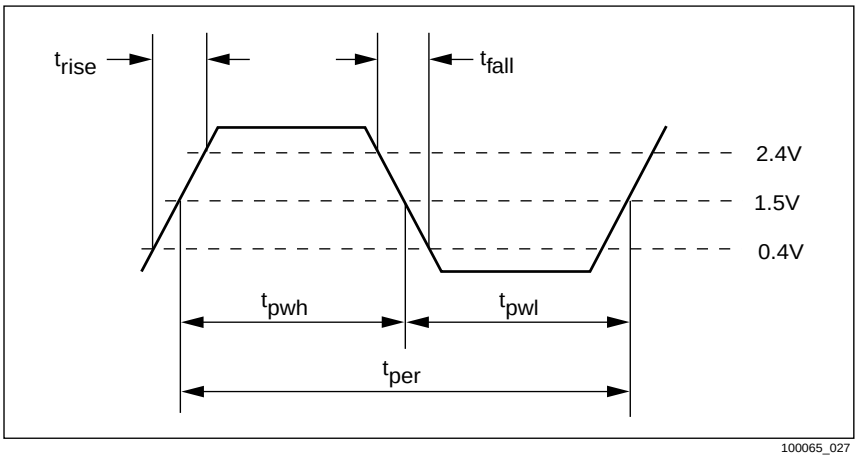


Figure 5-2 shows how output waveforms are defined.

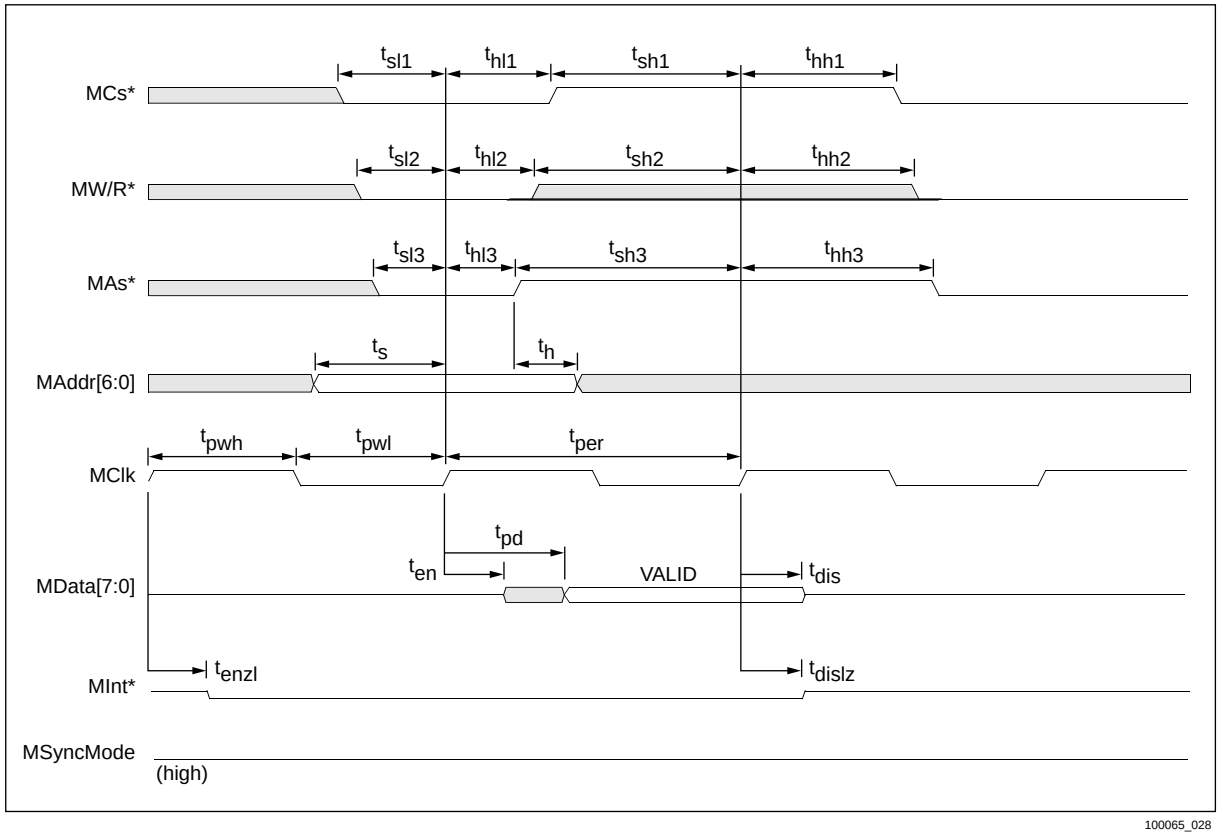
Figure 5-2. Output Waveform



5.1.1 Microprocessor Interface Timing

Figures 5-3 through 5-8 and Tables 5-2 through 5-7 define the timing requirements and characteristics of the microprocessor interface.

Figure 5-3. Synchronous Mode, Read Timing Diagram

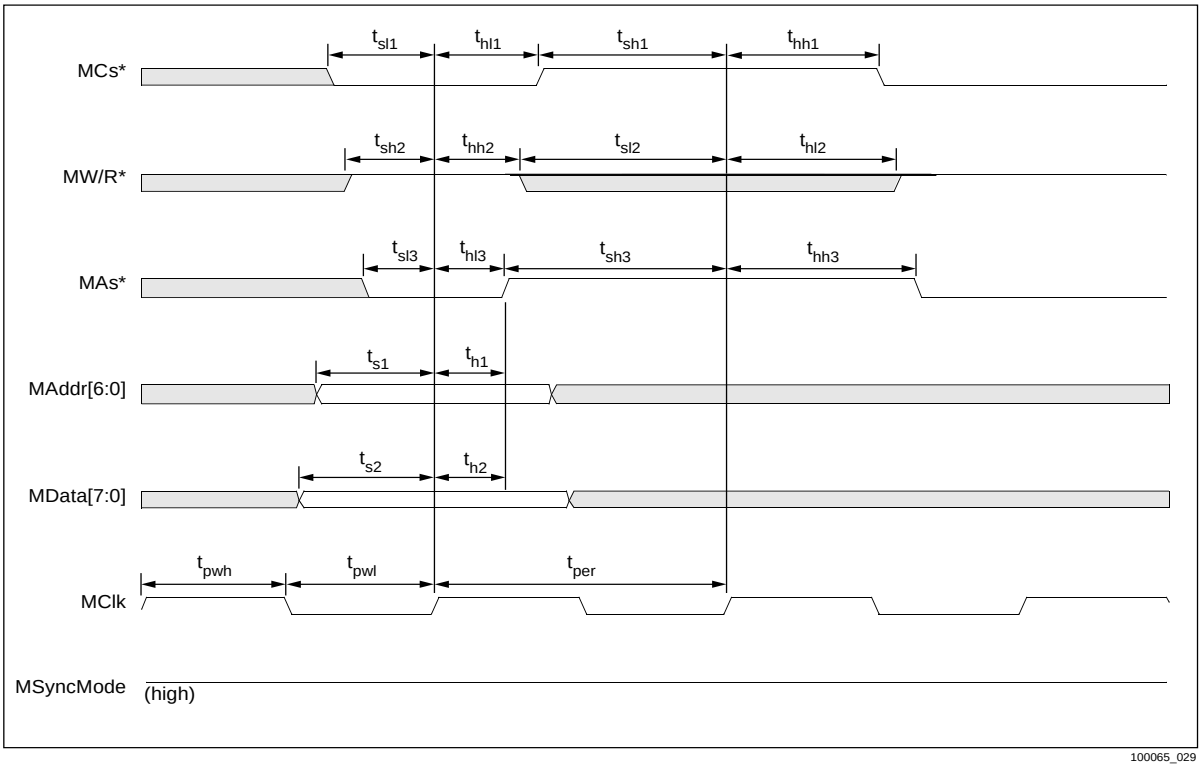


NOTE(S): MCs* and MW/R* must not change state while MAs* is asserted.

Table 5-2. Synchronous Mode, Read Timing Table

Label	Description	Min	Max	Unit
t_{pwh}	Pulse Width High, MClk	8	50	ns
t_{pwl}	Pulse Width Low, MClk	8	50	ns
t_{per}	Period, MClk	20	125	ns
t_{sl1}	Setup Low, MCs* to the rising edge of MClk	1	—	ns
t_{hl1}	Hold Low, MCs* from the rising edge of MClk	2.5	—	ns
t_{sh1}	Setup High, MCs* to the rising edge of MClk	1	—	ns
t_{hh1}	Hold High, MCs* from the rising edge of MClk	2.5	—	ns
t_{sl2}	Setup Low, MW/R* to the rising edge of MClk	1	—	ns
t_{hl2}	Hold Low, MW/R* from the rising edge of MClk	2.5	—	ns
t_{sh2}	Setup High, MW/R* to the rising edge of MClk	1	—	ns
t_{hh2}	Hold High, MW/R* from the rising edge of MClk	2.5	—	ns
t_{sl3}	Setup Low, MAs* to the rising edge of MClk	1	—	ns
t_{hl3}	Hold Low, MAs* from the rising edge of MClk	2.5	—	ns
t_{sh3}	Setup High, MAs* to the rising edge of MClk	1	—	ns
t_{hh3}	Hold High, MAs* from the rising edge of MClk	2.5	—	ns
t_{s}	Setup, MAddr[6:0] to the rising edge of MClk	1	—	ns
t_{h}	Hold, MAddr[6:0] from the rising edge of MAs*	2.5	—	ns
t_{en}	Enable, MData[7:0] from the rising edge of MClk	2	13	ns
t_{pd}	Propagation Delay, MData[7:0] from the rising edge of MClk	2	15	ns
t_{dis}	Disable, MData[7:0] from the rising edge of MClk	2	13	ns
t_{enzl}	Enable, MInt* from the rising edge of MClk	2	10	ns
t_{dislz}	Disable, MInt* from the rising edge of MClk	2	10	ns
Loading: Database = 60 pF, MInt* = 20 pF				

Figure 5-4. Synchronous Mode, Write Timing Diagram



NOTE(S): MCs* and MW/R* must not change state while MAs* is asserted.

Table 5-3. Synchronous Mode, Write Timing Table

Label	Description	Min	Max	Unit
t_{pwh}	Pulse Width High, MClk	8	50	ns
t_{pwl}	Pulse Width Low, MClk	8	50	ns
t_{per}	Period, MClk	20	125	ns
t_{sl1}	Setup Low, MCs* to the rising edge of MClk	1	—	ns
t_{hl1}	Hold Low, MCs* from the rising edge of MClk	2.5	—	ns
t_{sh1}	Setup High, MCs* to the rising edge of MClk	1	—	ns
t_{hh1}	Hold High, MCs* from the rising edge of MClk	2.5	—	ns
t_{sl2}	Setup Low, MW/R* to the rising edge of MClk	1	—	ns
t_{hl2}	Hold Low, MW/R* from the rising edge of MClk	2.5	—	ns
t_{sh2}	Setup High, MW/R* to the rising edge of MClk	1	—	ns
t_{hh2}	Hold High, MW/R* from the rising edge of MClk	2.	—	ns
t_{sl3}	Setup Low, MAs* to the rising edge of MClk	1	—	ns
t_{hl3}	Hold Low, MAs* from the rising edge of MClk	2.5	—	ns
t_{sh3}	Setup High, MAs* to the rising edge of MClk	1	—	ns
t_{hh3}	Hold High, MAs* from the rising edge of MClk	2.5	—	ns
t_{s1}	Setup, MAddr[6:0] to the rising edge of MClk	1	—	ns
t_{h1}	Hold, MAddr[6:0] from the rising edge of MClk	6.5	—	ns
t_{s2}	Setup, MData[7:0] to the rising edge of MClk	1	—	ns
t_{h2}	Hold, MData[7:0] from the rising edge of MAs*	6.5	—	ns
Output load = 60 pF on the data bus				

Figure 5-5. Asynchronous Mode, Read Timing (High-Performance Access Time)

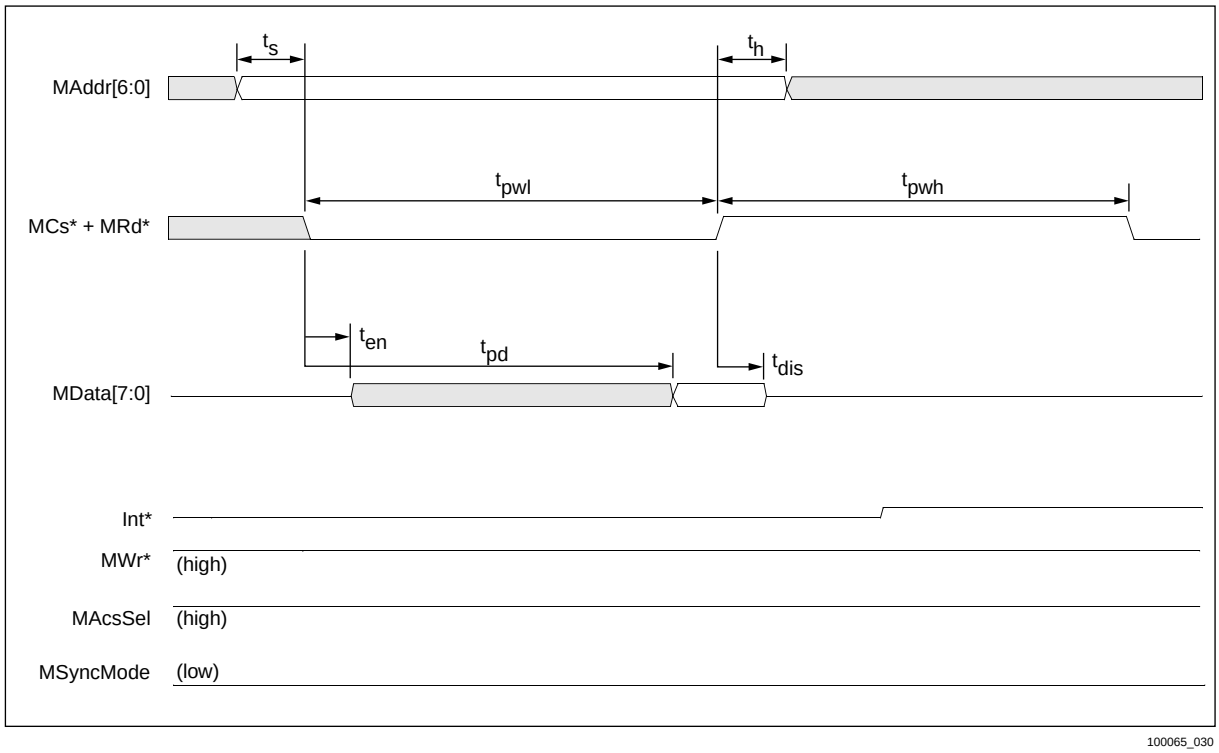


Table 5-4. Asynchronous Mode, Read Timing Table (High-Performance Access Time)

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, (MCs* + MRd*)(2)	2* Clk + 15 ns(1)	—	ns
t_{pwh}	Pulse Width High, (MCs* +MRd*)	Clk + 15 ns(1)	—	ns
t_s	Setup, MAddr[6:0] to the falling edge of (MCs* + MRd*)	2	—	ns
t_h	Hold, MAddr[6:0] from the rising edge of (MCs* + MRd*)	7	—	ns
t_{en}	Enable, MData[7:0] from the falling edge of (MCs* + MRd*)	2	13	ns
t_{pd}	Propagation Delay, MData[7:0] from the falling edge of (MCs* + MRd*)	—	2* Clk + 10(1)	ns
t_{dis}	Disable, MData[7:0] from the rising edge of (MCs* + MRd*)	2	13	ns

NOTE:

(1) Due to internal sampling mechanisms used, these times are specified in clock cycles rather than absolute values. For these calculations Clk equals the period of clock selected via the Clk pin (either 26 ns or 52 ns; see Section 2.8).

(2) Timing starts with either MCs* or MRd*, whichever occurs last.

Figure 5-6. Asynchronous Mode, Write Timing (High-Performance Access Time)

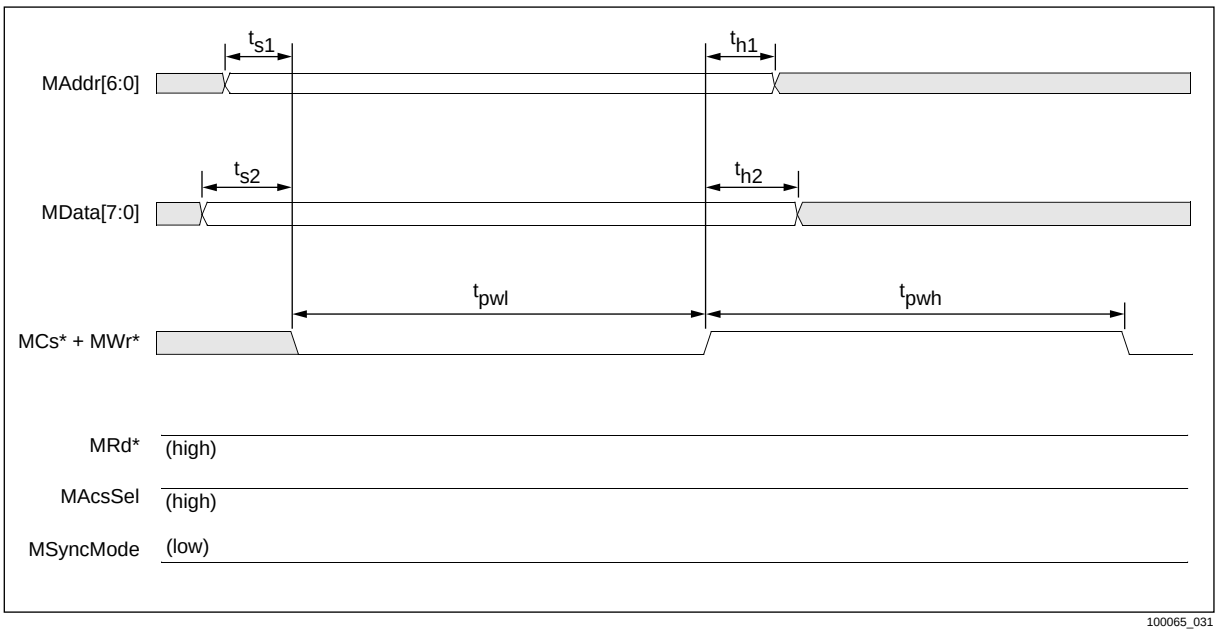


Table 5-5. Asynchronous Mode, Write Timing Table (High-Performance Access Time)

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, (MCs* + MWr*)(2)	2* Clk + 15 ns(1)	—	ns
t_{pwh}	Pulse Width High, (MCs* + MWr*)	Clk + 15 ns(1)	—	ns
t_{s1}	Setup, MAddr[6:0] to the falling edge of (MCs* + MWr*)	2	—	ns
t_{h1}	Hold, MAddr[6:0] from the rising edge of (MCs* + MWr*)	7	—	ns
t_{s2}	Setup, MData[7:0] from the falling edge of (MCs* + MWr*)	—	1 Clk(1)	ns
t_{h2}	Hold, MData[7:0] from the rising edge of (MCs* + MWr*)	7	—	ns

NOTE:

(1) Due to internal sampling mechanisms used, these times are specified in clock cycles rather than absolute values. For these calculations Clk equals the period of clock selected via the Clk pin (either 26 ns or 52 ns; see Section 2.8).

(2) Timing starts with either MCs* or MRd*, whichever occurs last.

Figure 5-7. Asynchronous Mode, Read Timing Diagram (Low-Power Access Time)

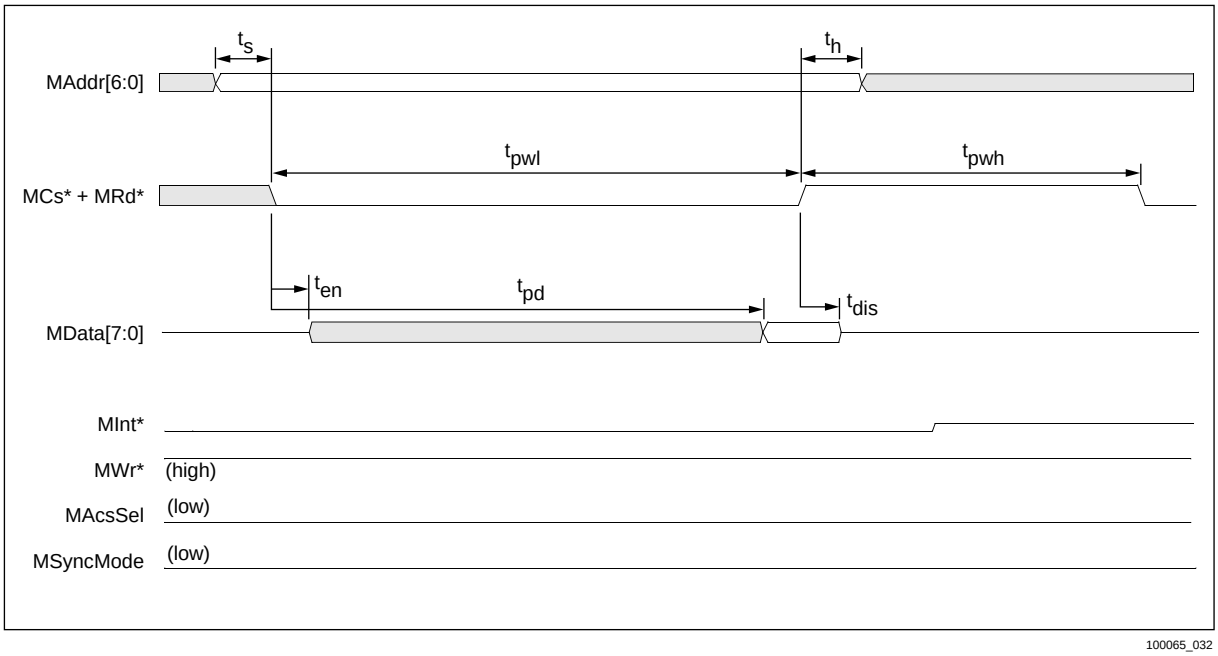


Table 5-6. Asynchronous Mode, Read Timing Table (Low-Power Access Time)

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, (MCs* + MRd*)	130	—	ns
t_{pwh}	Pulse Width High, (MCs* +MRd*)	130	—	ns
t_s	Setup, MAddr[6:0] to the falling edge of (MCs* + MRd*)	2	—	ns
t_h	Hold, MAddr[6:0] from the rising edge of (MCs* + MRd*)	7	—	ns
t_{en}	Enable, MData[7:0] from the falling edge of (MCs* + MRd*)	2	13	ns
t_{pd}	Propagation Delay, MData[7:0] from the falling edge of (MCs* + MRd*)	—	130	ns
t_{dis}	Disable, MData[7:0] from the rising edge of (MCs* + MRd*)	2	13	ns

Figure 5-8. Asynchronous Mode, Write Timing Diagram (Low-Power Access Time)

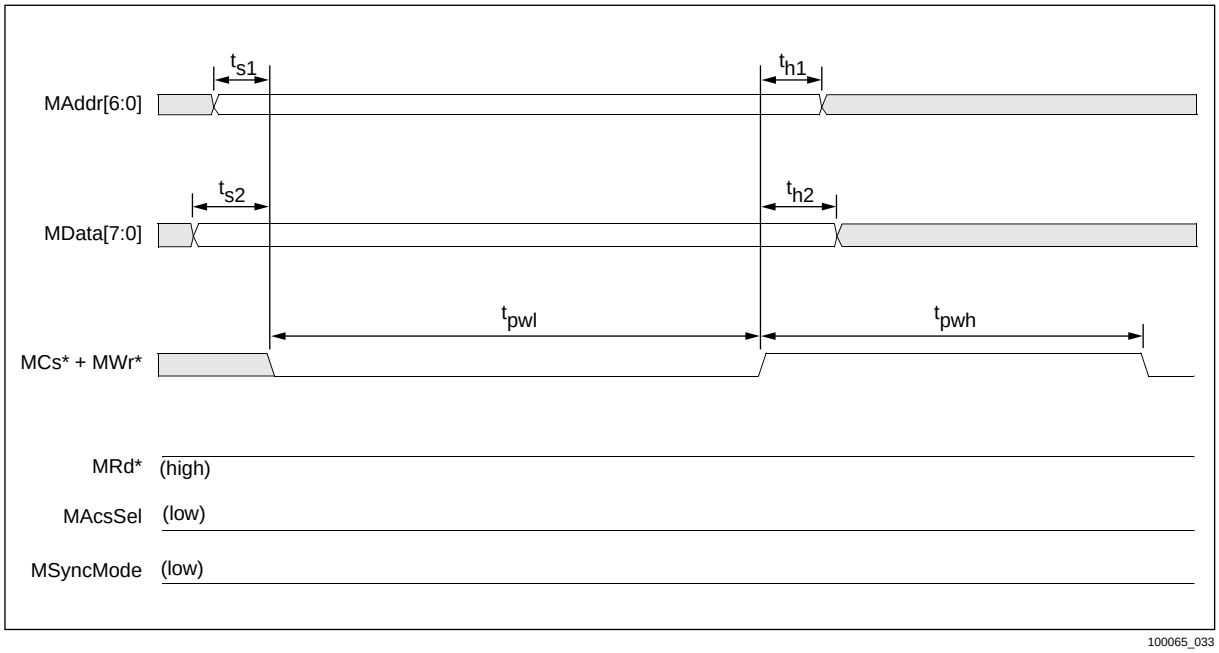


Table 5-7. Asynchronous Mode, Write Timing Table (Low-Power Access Time)

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, (MCs* + MWr*)	130	—	ns
t_{pwh}	Pulse Width High, (MCs* + MWr*)	130	—	ns
t_{s1}	Setup, MAddr[6:0] to the falling edge of (MCs* + MWr*)	2	—	ns
t_{h1}	Hold, MAddr[6:0] from the rising edge of (MCs* + MWr*)	7	—	ns
t_{s2}	Setup, MData[7:0] to the falling edge of (MCs* + MWr*)	2	—	ns
t_{h2}	Hold, MData[7:0] from the rising edge of (MCs* + MWr*)	7	—	ns

5.1.2 Transmit UTOPIA Interface Timing

Figure 5-9 and Table 5-8 define the timing requirements and characteristics of the transmit UTOPIA interface. All times provided are in nanoseconds. The output load for this interface is 50 pF.

NOTE: Figure 5-9 shows timing only, it does not imply function.

Figure 5-9. Transmit UTOPIA Interface Timing Diagram

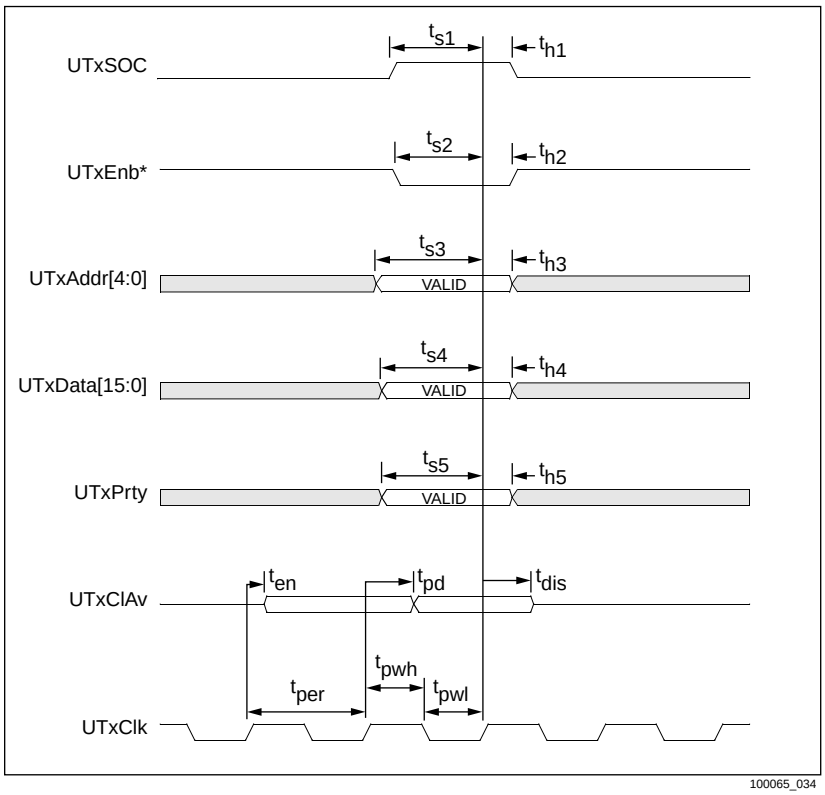


Table 5-8. Transmit UTOPIA Interface Timing Table

Label	Description	Min	Max	Unit
t_{s1}	Setup, UTxSOC to the rising edge of UTxClk	4	—	ns
t_{s2}	Setup, UTxEnb* to the rising edge of UTxClk	4	—	ns
t_{s3}	Setup, UTxAddr[4:0] to the rising edge of UTxClk	4	—	ns
t_{s4}	Setup, UTxData[15:0] to the rising edge of UTxClk	4	—	ns
t_{s5}	Setup, UTxPrty to the rising edge of UTxClk	4	—	ns
t_{h1}	Hold, UTxSOC from the rising edge of UTxClk	1	—	ns
t_{h2}	Hold, UTxEnb* from the rising edge of UTxClk	1	—	ns
t_{h3}	Hold, UTxAddr[4:0] from the rising edge of UTxClk	1	—	ns
t_{h4}	Hold, UTxData[15:0] from the rising edge of UTxClk	1	—	ns
t_{h5}	Hold, Prty from the rising edge of UTxClk	1	—	ns
t_{en}	Enable, UTxClAv from the rising edge of UTxClk	1	4	ns
t_{pd}	Propagation Delay, UTxClAv from the rising edge of UTxClk	1	9	ns
t_{dis}	Disable, UTxClAv from the rising edge of UTxClk	1	4	ns
t_{per}	Period, UTxClk	20	—	ns
t_{pwh}	Pulse width high, UTxClk	8	—	ns
t_{pwl}	Pulse width low, UTxClk	8	—	ns

5.1.3 Receive UTOPIA Interface Timing

Figure 5-10 and Table 5-9 define the timing requirements and characteristics of the receive UTOPIA interface. All times provided are in nanoseconds. The output load for this interface is 50 pF.

NOTE: Figure 5-10 shows timing only, it does not imply function.

Figure 5-10. Receive UTOPIA Interface Timing Diagram

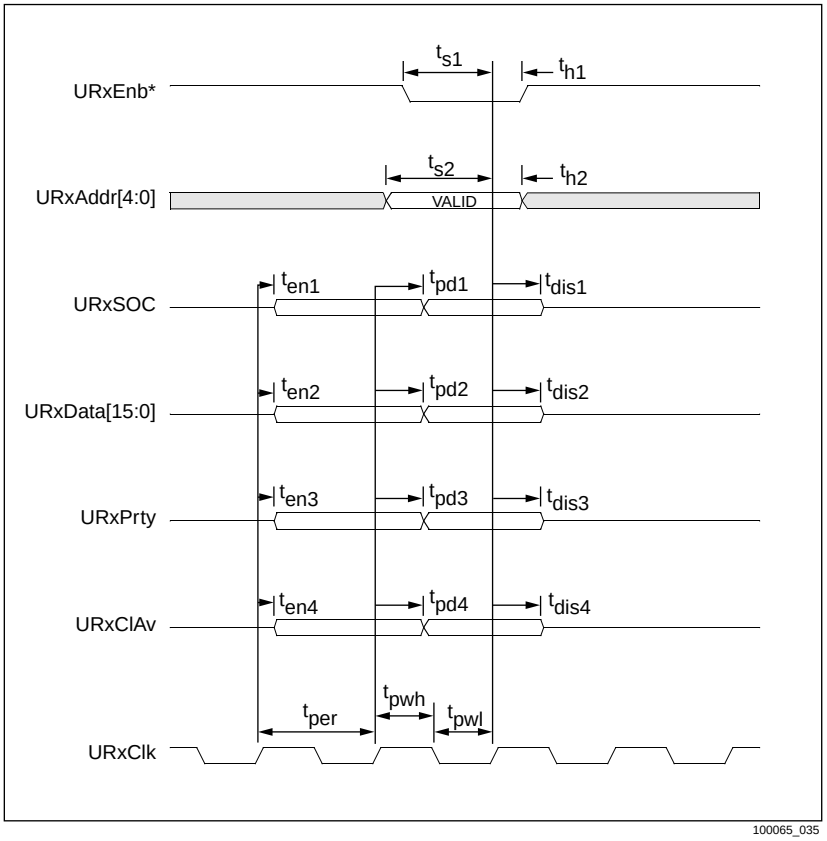


Table 5-9. Receive UTOPIA Interface Timing Table

Label	Description	Min	Max	Unit
t_{s1}	Setup, URxEnb* to the rising edge of URxClk	4	—	ns
t_{s2}	Setup, URxAddr[4:0] to the rising edge of URxClk	4	—	ns
t_{h1}	Hold, URxEnb* from the rising edge of URxClk	1	—	ns
t_{h2}	Hold, URxAddr[4:0] from the rising edge of URxClk	1	—	ns
t_{en1}	Enable, URxSOC from the rising edge of URxClk	2	10	ns
t_{pd1}	Propagation Delay, URxSOC from the rising edge of URxClk	1	14	ns
t_{dis1}	Disable, URxSOC from the rising edge of URxClk	2	10	ns
t_{en2}	Enable, URxData[15:0] from the rising edge of URxClk	2	10	ns
t_{pd2}	Propagation Delay, URxData[15:0] from the rising edge of URxClk	1	14	ns
t_{dis2}	Disable, URxData[15:0] from the rising edge of URxClk	2	10	ns
t_{en3}	Enable, URxPrty from the rising edge of URxClk	2	10	ns
t_{pd3}	Propagation Delay, URxPrty from the rising edge of URxClk	1	14	ns
t_{dis3}	Disable, URxPrty from the rising edge of URxClk	2	10	ns
t_{en4}	Enable, URxClAv from the rising edge of URxClk	1	8	ns
t_{pd4}	Propagation Delay, URxClAv from the rising edge of URxClk	1	10	ns
t_{dis4}	Disable, URxClAv from the rising edge of URxClk	1	8	ns
t_{per}	Period, URxClk	20	—	ns
t_{pwh}	Pulse width high, URxClk	8	—	ns
t_{pwl}	Pulse width low, URxClk	8	—	ns

5.1.4 JTAG Interface Timing

Figure 5-11 and Table 5-10 define the timing requirements and characteristics of the JTAG interface.

Figure 5-11. JTAG Timing Diagram

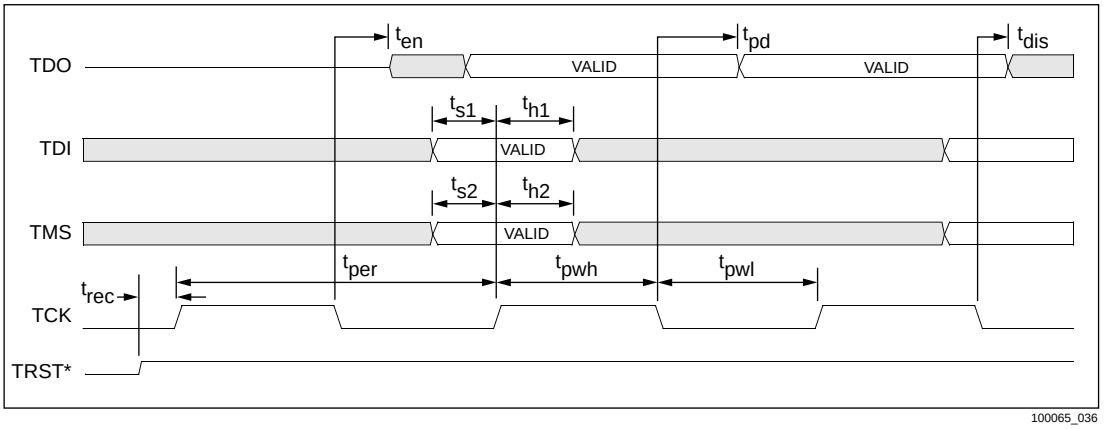


Table 5-10. JTAG Timing Table

Symbol	Description	Min	Max	Unit
t_{en}	Enable, TDO from the falling edge of TCK	0.8	5	ns
t_{pd}	Propagation Delay, TDO from the falling edge of TCK	0.8	5	ns
t_{s1}	Setup, TDI to the rising edge of TCK	2	—	ns
t_{s2}	Setup, TMS to the rising edge of TCK	2	—	ns
t_{h1}	Hold, TDI from the rising edge of TCK	6	—	ns
t_{h2}	Hold, TMS from the rising edge of TCK	6	—	ns
t_{pwh}	Pulse width high, TCK	16	—	ns
t_{pwl}	Pulse width low, TCK	16	—	ns
t_{dis}	Disable, TDO from the falling edge of TCK	0.8	5	ns
t_{rec}	Recovery time, TCK from the rising edge of TRST*	2.5	—	ns
t_{per}	Period, TCK	40	—	ns

5.1.5 One-second Interface Timing

Figure 5-12 and Table 5-11 show the timing requirements and characteristics of the One-second interface. These output values are measured into a 20 pF load.

Figure 5-12. One-second Timing Diagram

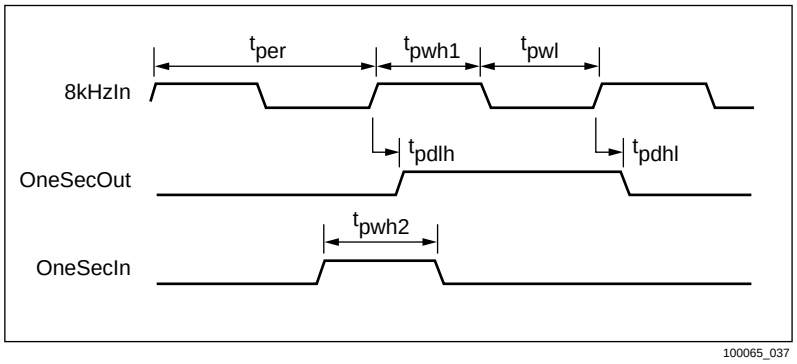


Table 5-11. One-second Timing Table

Symbol	Description	Min	Max	Unit
t_{per}	Period, 8kHzIn	125	125	µs
t_{pwh1}	Pulse Width High, 8kHzIn	10	—	ns
t_{pwl}	Pulse Width Low, 8kHzIn	10	—	ns
t_{pdlh}	Propagation Delay Low-to-high, OneSecOut from the rising edge of 8kHzIn	2	9	ns
t_{pdhl}	Propagation Delay High-to-low, OneSecOut from the rising edge of 8kHzIn	2	6	ns
t_{pwh2}	Pulse Width High, OneSecIn	22	—	ns

5.1.6 Data Link Timing

Figure 5-13 and Table 5-12 show the receive timing requirements and characteristics for the Data Link. Figure 5-14 and Table 5-13 show the transmit timing requirements and characteristics for the Data Link.

Figure 5-13. Data Link Receive Timing Diagram

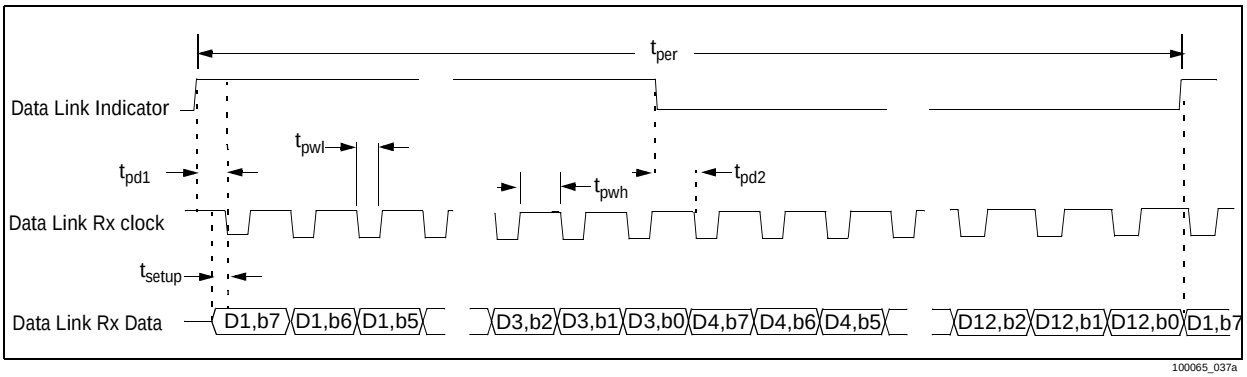


Table 5-12. Data Link Receive Timing Table

Symbol	Description	Min	Typical	Max	Unit
t_{pwh}	Time for clock output high (average)	—	1030	—	ns
t_{pwl}	Time for clock output low	—	50	—	ns
t_{pd1}	Propagation delay: Rising edge of sync to next falling edge of clock	—	825	—	ns
t_{pd2}	Propagation delay: Falling edge of sync to next falling edge of clock	—	852	—	ns
t_{setup}	Setup time: clock to data valid	—	50	—	ns
t_{per}	Period	—	125,000	—	ns

Figure 5-14. Data Link Transmit Timing Diagram

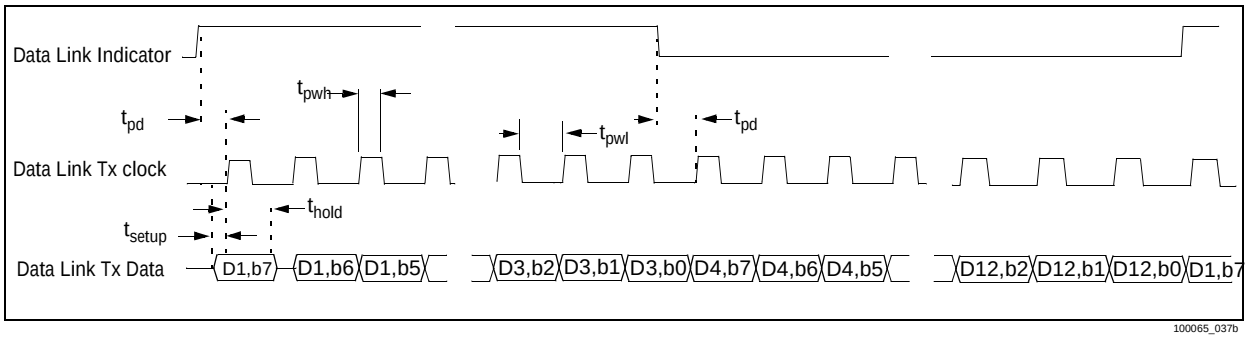


Table 5-13. Data Link Transmit Timing Table

Symbol	Description	Min	Typical	Max	Unit
t_{pwh}	Time for clock output high	—	50	—	ns
t_{pwl}	Time for clock output low	—	1030	—	ns
t_{pd1}	Propagation delay: edge of indicator to rising edge of clock	—	780	—	ns
t_{setup}	Setup time: data valid to rising edge of clock	—	15	—	ns
t_{hold}	Hold time: clock edge to data invalid	—	15	—	ns

5.2 Absolute Maximum Ratings

The absolute maximum ratings listed in Table 5-12 are the maximum stresses that the device can tolerate without risking permanent damage. These ratings are not typical of normal operation of the device. Exposure to absolute maximum rating conditions for extended periods of time may affect the device's reliability. This device should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Table 5-14. Absolute Maximum Ratings

Parameter	Value
Supply Voltage	–0.5 to +4.6 V
V_{GG} Pin	+6.0 V
Storage Temperature	–40 °C to 125 °C
Lead Temperature	+240 °C for 10 sec.
Junction Temperature	+150 °C
Static Discharge Voltage	±2500 V
Latch-up Current	±300 mA @ 25 °C ±150 mA @ 125 °C
FIT Rate	25

5.3 DC Characteristics

This section describes the DC characteristics of the RS8251. Table 5-15 lists general DC characteristics.

Table 5-15. DC Characteristics (–40 ≤ T_A ≤ +85, VDD = 3.3 V ± 5%, VDD ≤ VGG ≤ 5.5 V)

Parameter	Min	Typical	Max	Unit	Conditions
Input Low Voltage (VIL)	—	—	—	—	—
5 V-Tolerant TTL	0	—	0.8	VDC	—
5 V-Tolerant HYS	0	—	0.3*VDD	VDC	—
—	—	—	—	—	—
Input High Voltage (VIH)	—	—	—	—	—
5 V-Tolerant TTL	2.0	—	5.25	VDC	—
5 V-Tolerant HYS	0.7*VDD	—	5.25	VDC	—
—	—	—	—	—	—
Input Hysteresis - 5 V-Tolerant	0.3	—	—	VDC	—
TTL Output Low Voltage (VOL)	—	—	0.4	VDC	I_{OH} = 4.0 mA
TTL Output High Voltage (VOH)	2.4	—	—	VDC	I_{OH} = 1500 µA
Pullup Resistance (Rpu)	15	—	75	k Ω	
Input Leakage Current	-10	—	10	µA	Vin = PWR or GND
Three-state Output Leakage Current	-10	—	10	µA	Vout = PWR or GND
Input Capacitance	—	—	7	pF	—
Output Capacitance	—	—	7	pF	—
Bidirectional Capacitance	—	—	7	pF	—
Operating Power Consumption Processing Cells (RS8250/1)	—	470	—	mW	Transmitter driving 50 Ω PECL load UTOPIA Tx/Rx Clock at 22 MHz
Operating Current	—	143	—	mA	—
NOTE(S): All outputs are TTL drive levels and can be used with 3 V CMOS or 5 V TTL logic. Operating Power Consumption for Quad Devices is 4 x 470 mW, or 1.88 W, typical.					

5.3.1 PECL - Input

The PECL input DC characteristics are shown in Table 5-16.

Table 5-16. PECL-Input DC Characteristics (–40 ≤ T_A ≤ +85, VDD = 3.3 V ± 5%, VDD ≤ VGG ≤ 5.5 V)

Symbol	Parameter	Min.	Typical	Max.	Conditions
V_{ref}	Mid-point of V_{ih} and V_{il}	—	2.0 V	—	—
V_{ih}	Input Voltage (high level)	V_{ref} + 60 mV	—	—	—
V_{il}	Input Voltage (low level)	—	—	V_{ref} – 60 mV	—
I_{ih}	Input Current (high level)	—	—	+10 µA	V_{in} = VDD
I_{il}	Input Current (low level)	–10 µA	—	—	V_{in} = VSS
NOTE(S): All PECL voltages are referenced to ground.					

5.3.2 PECL - Output

The PECL output DC characteristics are shown in Table 5-17.

Table 5-17. PECL-Output DC Characteristics (–40 ≤ T_A ≤ +85, VDD = 3.3 V ± 5%, VDD ≤ VGG ≤ 5.5 V)

Symbol	Parameter	Min.	Typical	Max.	Conditions
I_{nn}	Output leakage current	—	+10 µA	—	$0 \le V_{OH} \le V_{DD}$
I_{oh}	Output High current	—	16 mA	—	—
V_{ol}	Static DC LOW level	1.54 V	1.70 V	1.86 V	(1)
V_{oh}	Static DC HIGH level	2.21 V	2.51 V	2.78 V	(1)
NOTE(S): Use 82/130 Ω resistor network to V_{DD}.					

5.4 RS8250 Electrical and Mechanical Description

This section describes how the RS8250's electrical and mechanical characteristics differ from the RS8251 single device. The timing, absolute maximum ratings, and DC characteristics are the same for the single, dual, and quad versions of this product.

5.4.1 RS8250 Mechanical Drawing

The various views of the RS8250 mechanical drawing are shown in Figure 5-15, Figure 5-16, and Figure 5-17.

Figure 5-15. 156-Pin Ball Gate Array (BGA) Package—Top and Side Views

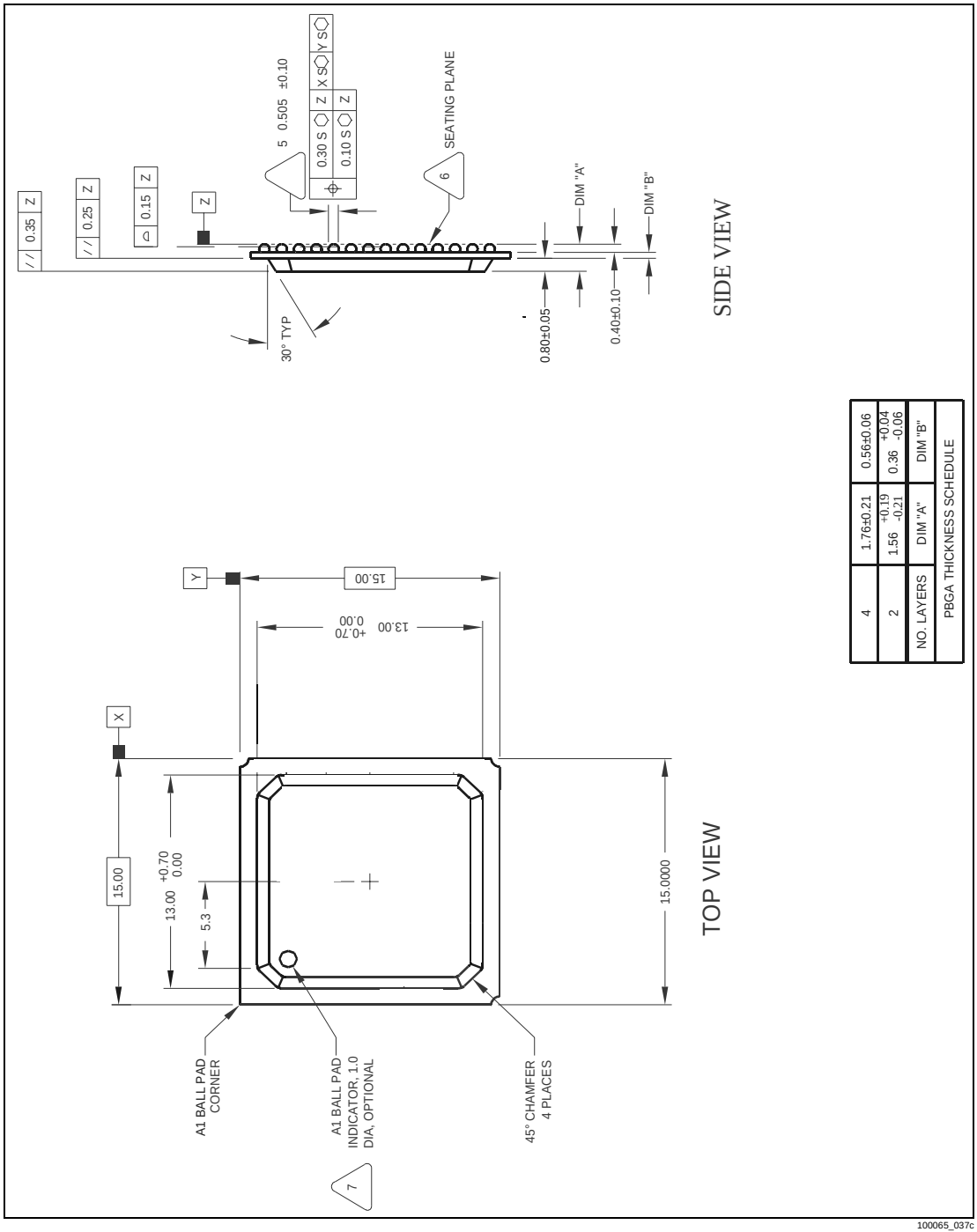


Figure 5-16. 156-Pin Ball Gate Array (BGA) Package—Bottom View

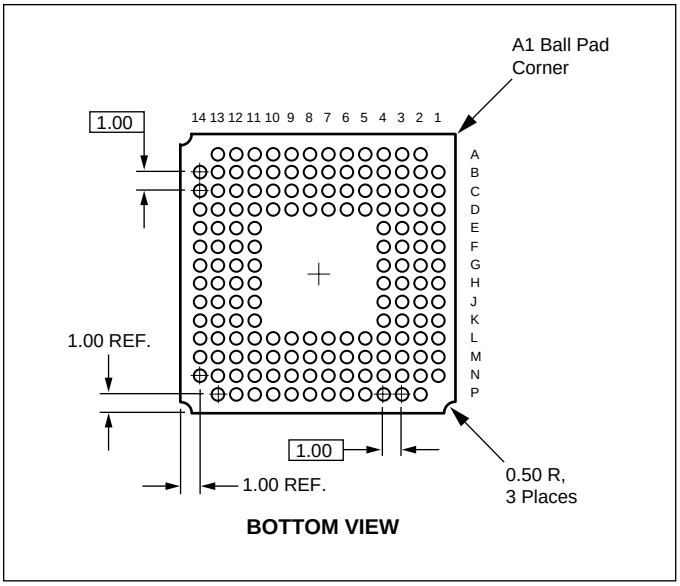
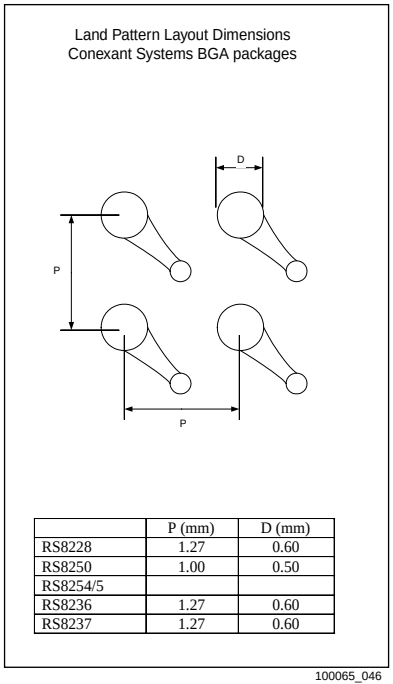


Figure 5-17. Land Patterns for the RS8250



	P (mm)	D (mm)
RS8228	1.27	0.60
RS8250	1.00	0.50
RS8254/5		
RS8236	1.27	0.60
RS8237	1.27	0.60

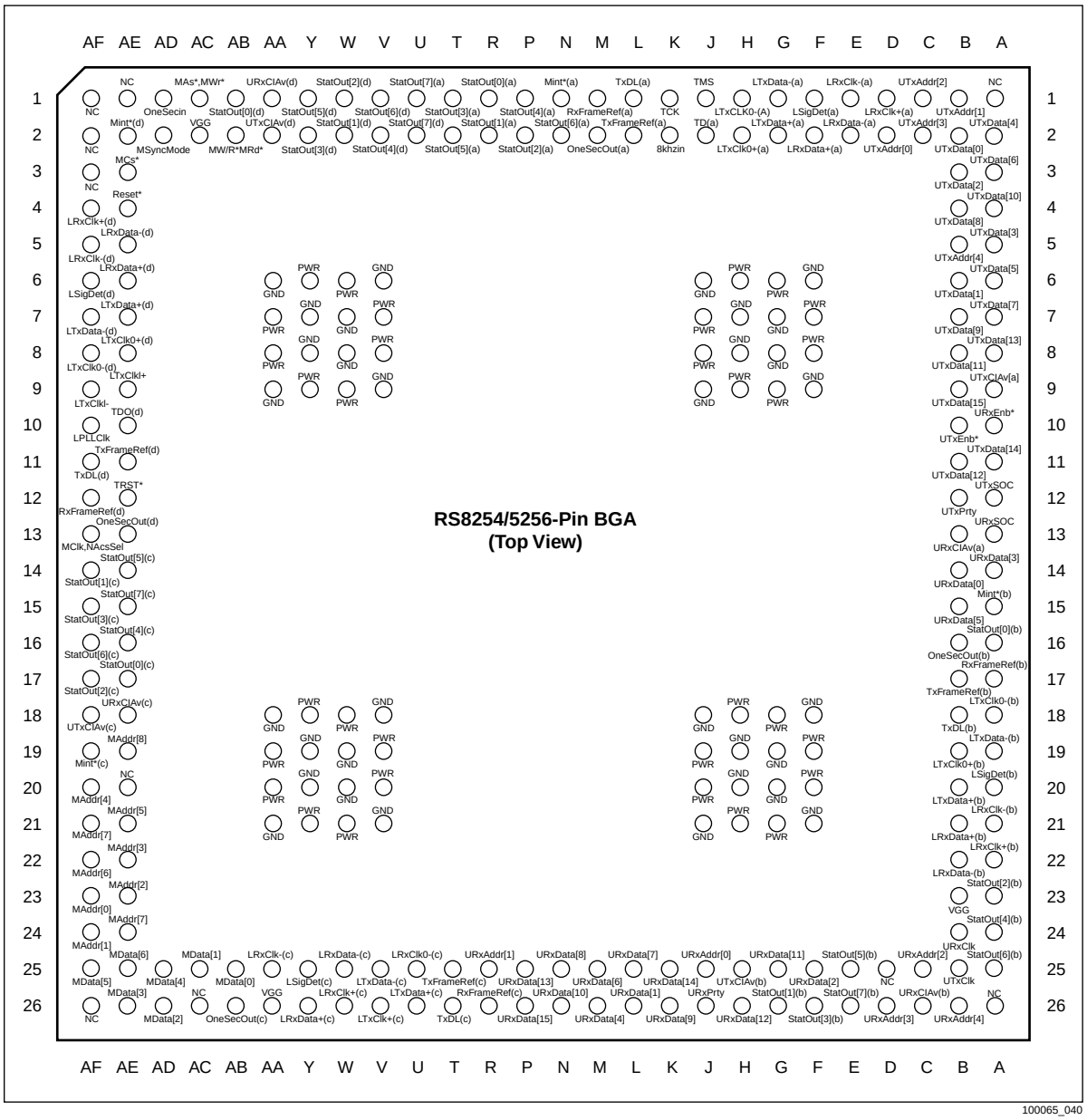
Appendix A RS8254/5 Quad PHY Device

This appendix describes the RS8254/5 Quad PHY and how it differs from the RS8251 PHY.

A.1 RS8254/5 Pinout and Pin Descriptions

Figure A-1 is the pinout diagram for the RS8254/5 ATM Transmitter/Receiver. It is a quad CMOS integrated circuit packaged in a 256-pin BGA. All unused input pins should be connected to ground. Unused outputs should be left unconnected.

Figure A-1. RS8254/5 Pinout Diagram: Top View



Pin names and numbers are listed in Table A-1. An asterisk (*) following a pin label indicates that the pin logic level is active low.

Table A-1. RS8254/5 Pin Definitions *(1 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Clock and Control	Reset*	Device Reset	B4	TTL	I	This pin is used to reset the device when asserted low.
	OneSecIn	One-Second Strobe	C1	TTL	I	This input is used to latch device status, typically at 1-second intervals.
	OneSecOut (a) (b) (c) (d)	One-Second Output (PHY a) (PHY b) (PHY c) (PHY d)	 R2 AE16 E26 B13	TTL	O	This pin is a 1-second count derived from the 8khzIn input (pin 37).
	TxFrameRef (a) (b) (c) (d)	Transmit Frame Clock (PHY a) (PHY b) (PHY c) (PHY d)	 T2 AE17 L25 B11	TTL	O	This pin can be either an 8 kHz output derived from the Transmit SDH frame or a 19.44 MHz output derived from the transmit clock, as selected by bit 1 of the TXSEC (0xOC) register.
	RxFrameRef (a) (b) (c) (d)	Receive Frame Clock (PHY a) (PHY b) (PHY c) (PHY d)	 R1 AF17 M26 A12	TTL	O	This pin can be either an 8 kHz output derived from the Receive SDH frame or a 19.44 MHz output derived from the recovered (receive) clock as selected by bit 1 of the RXSEC (0x45) register.
	8kHzIn	8 kHz Reference Clock Input	U2	TTL	I	This pin is an 8 kHz clock input used to derive OneSecOut (pin 34). The 155.52 MHz transmit clock can be synthesized from this clock.
PMD Line Interface	LTxClkI–	Line Transmit Clock Input Negative Polarity	A9	PECL	I	This pin transmits the timing source directly to the LTxClkO pin if an external source is selected by bits 3 and 4 in the CLKREC register (0x01). This pin is intended to operate at 155.52 MHz. The source must be accurate to 20 PPM.
	LTxClkI+	Line Transmit Clock Input Positive Polarity	B9	PECL	I	This pin transmits the timing source directly to the LTxClkO pin if an external source is selected by bits 3 and 4 in the CLKREC register (0x01). This pin is intended to operate at 155.52 MHz. The source must be accurate to 20 PPM.
	LTxClkO– (a) (b) (c) (d)	Line Transmit Clock Output Negative Polarity (PHY a, b, c, d)	 W1 AF18 K25 A8	PECL	O	This pin is a 155.52 MHz output derived from one of four clock sources: LPLLClk, 8kHzIn, Loop-timed, or LTxClkI+/-. The clock source is selected in bits 3 and 4 of the CLKREC register (0x01). It is generally used for diagnostic purposes.

Table A-1. RS8254/5 Pin Definitions *(2 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
PMD Line Interface (cont.)	LTxClkO+ (a) (b) (c) (d)	Line Transmit Clock Output Positive Polarity (PHY a, b, c, d)	 W2 AE19 J26 B8	PECL	O	This pin is a 155.52 MHz output derived from one of four clock sources: LPLLClk, 8kHzIn, Loop-timed, or LTxClkI+/-. The clock source is selected in bits 3 and 4 of the CLKREC register (0x01). It is generally used for diagnostic purposes.
	LTxData– (a) (b) (c) (d)	Line Transmit Output Negative Polarity (PHY a, b, c, d)	 Y1 AF19 J25 A7	PECL	O	This pin transfers SDH-framed data from the RS8251 to the PMD in differential serial NRZ format.
	LTxData+ (a) (b) (c) (d)	Line Transmit Output Positive Polarity (PHY a, b, c, d)	 Y2 AE20 K26 B7	PECL	O	This pin transfers SDH-framed data from the RS8251 to the PMD in differential serial NRZ format.
	LRxClk– (a) (b) (c) (d)	Line Receive Clock Negative (PHY a, b, c, d)	 AB1 AF21 F25 A5	PECL	I	This pin is the receive clock.
	LRxClk+ (a) (b) (c) (d)	Line Receive Clock Positive (PHY a, b, c, d)	 AC1 AF22 H26 A4	PECL	I	This pin is the receive clock.
	LRxData– (a) (b) (c) (d)	Line Receive Input Negative (PHY a, b, c, d)	 AB2 AE22 H25 B5	PECL	I	This pin receives differential serial NRZ data from the PMD.
	LRxData+ (a) (b) (c) (d)	Line Receive Input Positive (PHY a, b, c, d)	 AA2 AE21 G26 B6	PECL	I	This pin receives differential serial NRZ data from the PMD.
	LSigDet (a) (b) (c) (d)	Line Signal Detection (PHY a, b, c, d)	 AA1 AF20 G25 A6	TTL	I	This pin is high when the PMD is receiving a valid signal. Conexant recommends that a comparator be used (see Figure 2-3).
	LPLLClk	Line Phase Loop Lock Clock	A10	TTL	I	This pin is a 19.44 MHz clock input. The transmit synthesizer (PLL) uses this clock to generate 155.52 MHz LTxClkO output when bits 3 and 4 of the CLKREC register (0x01) are set to 0. ***NOTE:*** The transmit synthesizer PLL and clock recovery PLL use this input as a reference clock regardless of the timing source selection.

Table A-1. RS8254/5 Pin Definitions *(3 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Microprocessor Interface	MClk, MAcsSel	Microprocessor Clock, Access Time Select	A13	TTL	I	When MSyncMode is set to a logic 1, the MClk pin is a clock signal that samples the microprocessor interface pins (MCs*, MW/R*, MAs*, MAddr[6:0], MData[7:0]) on its rising edge. Additionally, the rising edge of MClk may cause the microprocessor interface output pins (MData[7:0], MInt*) to change states. When MSyncMode is set to a logic 0, the AcsSel pin selects the asynchronous interface access time. A logic 0 selects a power-saving access mode (130 ns) while a logic 1 selects the high-performance access mode (80 ns).
	MSyncMode	Microprocessor Synchronous/ Asynchronous Bus Mode Select	C2	TTL	I	A logic 1 selects the synchronous bus mode compatible with Bt8230 and Bt8233. In this mode, the microprocessor pins are defined as follows: MClk (pin 30), MW/R* (pin 7), MAs* (pin 9), MCs* (pin 8), MInt* (pin 6), MAddr (pins 12-18), and MData (pins 20-28). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MAcsSel (pin 30), MRd* (pin 7), MWr* (pin 9), MCs* (pin 8), MInt* (pin 6), MAddr (pins 12-18), and MData (pins 20-28).
	MCs*	Microprocessor Chip Select	B3	TTL	I	When MCs* is set to a logic 0, the device is enabled for read and write accesses. When MCs* is set to a logic 1, the device does not respond to input signal transitions on MClk,MAcsSel; MW/R*,MRd*; or MAs*,MWr*. Additionally, when MCs* is set to a logic 1, the MData[7:0] pins are in a high-impedance state but the Int* pin remains operational.
	MW/R*, MRd*	Microprocessor Write/Read, Read Control	E2	TTL	I	When MSyncMode is set to a logic 1, this pin is a read/write control pin. In this mode, when MW/R* is set to a logic 1, a write access is enabled and the MData[7:0] pin values is written to the memory location indicated by the MAddr[6:0] pins. Also in this mode, when MW/R* is set to a logic 0, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read and its value placed on the MData[7:0] pins. Both read and write accesses assume the device is chip selected (MCs* = 0), the address is valid (MAs* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is set to a logic 0, this pin is a read control pin. In this mode, when MRd* is set to a logic 0, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read and its value placed on the MData[7:0] pins. The read access assumes the device is chip selected (MCs* = 0), a write access is not being requested (MWr* = 1), and the device is not being reset (Reset* = 1).

Table A-1. RS8254/5 Pin Definitions *(4 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Microprocessor Interface (cont.)	MAs*,MWr*	Microprocessor Address Strobe, Write Control	D1	TTL	I	When MSyncMode is set to a logic 1, this pin is an address strobe pin. When the MAs* pin is set to a logic 0, it indicates a valid address, MAddr[6:0]. This signal is used to qualify read and write accesses. When MSyncMode is set to a logic 0, this pin is a write control pin. When MWr* is set to a logic 0, a write access is enabled, and the MData[7:0] pin values are written to the memory location indicated by the MAddr[6:0] pins. The write access assumes the device is chip selected (MCs* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1).
	MAddr[8]	Microprocessor Address Bus	B19	TTL	I	These seven bits are an address input for identifying the register that is accessed.
	MAddr[7]		A21	TTL	I	
	MAddr[6]		A22	TTL	I	
	MAddr[5]		B21	TTL	I	
	MAddr[4]		A20	TTL	I	
	MAddr[3]		B22	TTL	I	
	MAddr[2]		B23	TTL	I	
	MAddr[1]		A24	TTL	I	
	MAddr[0]		A23	TTL	I	
	MData[7]	Microprocessor Data Bus	B24	TTL	I/O	These eight bits are a bidirectional data bus for transferring the read and write data.
	MData[6]		B25	TTL	I/O	
	MData[5]		A25	TTL	I/O	
	MData[4]		C25	TTL	I/O	
	MData[3]		B26	TTL	I/O	
	MData[2]		C26	TTL	I/O	
	MData[1]		D25	TTL	I/O	
	MData[0]		E25	TTL	I/O	
	MInt* (a) (b) (c) (d)	Microprocessor Interrupt	 P1 AF15 A19 B2	TTL	O	When a logic 0 is read on this pin, the device needs servicing. It remains asserted until the pending interrupt is acknowledged. This pin is an open drain output for an external wired OR logic implementation.

Table A-1. RS8254/5 Pin Definitions *(5 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
JTAG (See IEEE 1149.1a-1993)	TRST*	Test Reset	B12	TTL	I	When this pin is asserted, the internal boundary-scan logic is reset. This pin has a pullup resistor.
	TCK	Test Clock	U1	TTL	I	This pin samples the value of TMS and TDI on its rising edge in order to control the boundary scan operations.
	TMS	Test Mode Select	V1	TTL	I	This pin controls the boundary-scan Test Access Port (TAP) controller operation.
	TDI(a)	Test Data Input (PHY a)	V2	TTL	I	This pin is the serial test data input.
	TDO(d)	Test Data Output (PHY d)	B10	TTL	O	This pin is the serial test data output.

Table A-1. RS8254/5 Pin Definitions *(6 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Status	StatOut[7] (a) (b) (c) (d)	Status Outputs[7:0] (PHY a, b, c, d)	K1 AB26 B15 K2	TTL	O	This pin reflects either the value in bit 7 of the OUTSTAT register (0x41) or LOS, as selected by bit 2 of register GEN (0x00). If selected by bit 0 or 1 of RXLIN (0x46), this pin will be the D1-D3 or D4-D12 receive data link serial clock output (RS8254 only).
	StatOut[6] (a) (b) (c) (d)		P2 AF25 A16 J1	TTL	O	This pin reflects either the value in bit 6 of the OUTSTAT register (0x41) or OOF, as selected by bit 2 of register GEN (0x00). If selected by bit 0 or 1 of RXLIN (0x46), this pin will be the D1-D3 or D4-D12 receive data link serial data output (RS8254 only).
	StatOut[5] (a) (b) (c) (d)		L2 AB25 B14 G1	TTL	O	This pin reflects either the value in bit 5 of the OUTSTAT register (0x41) or LOP, as selected by bit 2 of register GEN (0x00). For RS8254 only: if selected by bit 0 or 1 of RXLIN (0x46), this pin will be the D1-D3 or D4-D12 receive data link indication output. This output is high during the time that clock/data outputs contain pulses for D1-D3 octets. It is low during the time that clock/data outputs obtain pulses for D4-D12 octets.
	StatOut[4] (a) (b) (c) (d)		N1 AF24 B16 J2	TTL	O	This pin reflects either the value in bit 4 of the OUTSTAT register (0x41) or AIS-L, as selected by bit 2 of register GEN (0x00). If selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin will be the D1-D3 or D4-D12 transmit data link serial clock output (RS8254 only).
	StatOut[3] (a) (b) (c) (d)		L1 AA26 A15 G2	TTL	O	This pin reflects either the value in bit 3 of the OUTSTAT register (0x41) or RDI-L, as selected by bit 2 of register GEN (0x00). For RS8254 only: if selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin will be the D1-D3 or D4-D12 transmit data link indication output. This output is high during the time that clock/data inputs are expected for D1-D3 octets, and low for D4-D12 octets.
	StatOut[2] (a) (b) (c) (d)		N2 AF23 A17 H1	TTL	O	This pin reflects either the value in bit 2 of the OUTSTAT register (0x41) or AIS-P, as selected by bit 2 of register GEN (0x00). For RS8254 only: if selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin will output a pulse at the beginning of every cell slot time (both idle and data cells), synchronized to the UTOPIA transmit side.
	StatOut[1] (a) (b) (c) (d)		M2 Y26 A14 H2	TTL	O	This pin reflects either the value in bit 1 of the OUTSTAT register (0x41) or RDI-P, as selected by bit 2 of register GEN (0x00).
	StatOut[0] (a) (b) (c) (d)		M1 AF16 B17 E1	TTL	O	This pin reflects either the value in bit 0 of the OUTSTAT register (0x41) or LOCD, as selected by bit 2 of register GEN (0x00).

Table A-1. RS8254/5 Pin Definitions *(7 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Data Link	TxDL (RS8254 Only) (a) (b) (c) (d)	Transmit Data Link Input (PHY a) (PHY b) (PHY c) (PHY d)	 T1 AE18 L26 A11	TTL	I	This pin is used to input data for D1-D3, D4-D12. (It exists on the RS8254 WAN device but not the RS8255 LAN device. These pins must be tied to GND on the RS8255.)
UTOPIA Transmit	UTxClk	UTOPIA Transmit Clock	AE25	TTL	I	The data transfer/interface byte clock is provided by the ATM layer to the PHY layer for synchronizing transfers on UTxData.
	UTxEnb*	UTOPIA Transmit Enable	AE10	TTL	I	The enable data transfers signal is active low. It is asserted by the ATM layer during cycles when UTxData contains valid cell data.
	UTxAddr[0]	LSB	AC2	TTL	I	These pins are the address of the PHY device being selected. The address is driven from the ATM to the multi-PHY layer to poll and select the appropriate multi-PHY device. Each multi-PHY device must maintain its address. Address 31 indicates a null PHY port.
	UTxAddr[1]		AE1	TTL	I	
	UTxAddr[2]	UTOPIA Transmit Address	AD1	TTL	I	
	UTxAddr[3]		AD2	TTL	I	
	UTxAddr[4]	MSB	AE5	TTL	I	
	UTxData[0]	UTOPIA Transmit Data	AE2	TTL	I	The data bus is driven from the ATM layer to the PHY. UTxData[15] is the MSB of the high octet and UTxData[7] is the MSB of the lower octet.
	UTxData[1]		AE6	TTL	I	
	UTxData[2]		AE3	TTL	I	
	UTxData[3]		AF5	TTL	I	
	UTxData[4]		AF2	TTL	I	
	UTxData[5]		AF6	TTL	I	
	UTxData[6]		AF3	TTL	I	
	UTxData[7]		AF7	TTL	I	
	UTxData[8]		AE4	TTL	I	
	UTxData[9]		AE7	TTL	I	
	UTxData[10]		AF4	TTL	I	
	UTxData[11]		AE8	TTL	I	
	UTxData[12]		AE11	TTL	I	
	UTxData[13]		AF8	TTL	I	
	UTxData[14]		AF11	TTL	I	
	UTxData[15]		AE9	TTL	I	
	UTxPrty	UTOPIA Transmit Parity Input	AE12	TTL	I	The transmit data bus checks for odd parity over UTxData [7:0] coming from the ATM layer. In 16-bit mode, it checks for odd parity over UTxData[15:0].

Table A-1. RS8254/5 Pin Definitions *(8 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Transmit (cont.)	UTxSOC	UTOPIA Transmit Start of Cell	AF12	TTL	I	The Start of Cell signal is active high. It is asserted by the ATM layer during cycles when UTxData contains the first valid byte of the cell.
	UTxClAv (a) (b) (c) (d)	UTOPIA Transmit Cell Available (PHY a, b, c, d)	 AF9 W25 A18 F2	TTL	O	This signal indicates FIFO full or Cell Buffer Available. For octet-level flow control, this signal is active low from the PHY layer to the ATM layer. It is asserted to indicate that a maximum of four more transmit data writes will be accepted. For cell-level flow control in an multi-PHY environment, UTxClAv is an active high signal with high impedance potential going from the multi-PHY layer to the ATM layer. A polled multi-PHY device drives this signal only during each cycle following one with its address on the UTxAddr lines. The polled multi-PHY device asserts UTxClAv high to indicate it can accept the transfer of a complete cell, otherwise it deasserts the signal.(1)
UTOPIA Receive	URxClk	UTOPIA Receive Clock	AE24	TTL	I	The data transfer/interface byte clock is provided by the ATM layer to the PHY layer for synchronizing transfers on URxData.
	URxEnb*	UTOPIA Receive Enable	AF10	TTL	I	The enable receive data signal is active low. It is asserted by the ATM layer to indicate that URxData and URxSOC will be sampled at the end of the next cycle. In support of multiple PHY configurations, when URxEnb* is asserted, the URxData and URxSOC PHY layer outputs change to a high-impedance state. URxData and URxSOC must be enabled only in cycles following those with URxEnb* asserted.
	URxAddr[0]	UTOPIA Receive Address	V25	TTL	I	This is the address of the PHY device being selected. It is driven from the ATM to the multi-PHY layer to poll and select the appropriate multi-PHY device. URxAddr [4] is the MSB. Each multi-PHY device must maintain its address. Address 31 indicates a null PHY port.
	URxAddr[1]		M25	TTL	I	
	URxAddr[2]		AD25	TTL	I	
	URxAddr[3]		AC26	TTL	I	
	URxAddr[4]		AE26	TTL	I	

Table A-1. RS8254/5 Pin Definitions *(9 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Receive (cont.)	URxData[0]	UTOPIA Receive Data Bus	AE14	TTL	O	The data bus is driven from the ATM layer to the PHY layer. URxData[15] is the MSB of the high octet and URxData[7] is the MSB of the lower octet. To support multiple PHY configurations, URxData can be placed in a high-impedance state which is enabled only when URxEnb* is asserted.
	URxData[1]		T26	TTL	O	
	URxData[2]		AA25	TTL	O	
	URxData[3]		AF14	TTL	O	
	URxData[4]		R26	TTL	O	
	RxData[5]		AE15	TTL	O	
	URxData[6]		R25	TTL	O	
	URxData[7]		T25	TTL	O	
	URxData[8]		P25	TTL	O	
	URxData[9]		U26	TTL	O	
	URxData[10]		P26	TTL	O	
	URxData[11]		Y25	TTL	O	
	URxData[12]		W26	TTL	O	
	URxData[13]		N25	TTL	O	
	URxData[14]		U25	TTL	O	
	URxData[15]		N26	TTL	O	
	URxPrty	UTOPIA Receive Parity	V26	TTL	O	The data bus parity is odd parity for URxData[7:0], driven by the PHY layer. In 16-bit mode, this is the odd parity bit over URxData[15:0]. To support multiple PHY configurations, URxPrty can be placed in a high-impedance state which is enabled only in cycles following those with URxEnb* asserted.(1)
	URxSOC	UTOPIA Receive Start of Cell	AF13	TTL	O	The Start of Cell signal is active high. It is asserted by the PHY layer when RxData contains the first valid byte of the cell. In support of multiple PHY configurations, when URxEnb* is asserted, the URxData and URxSOC PHY layer outputs change to a high-impedance state. URxData and URxSOC must be enabled only in cycles following those with URxEnb* asserted.(1)

NOTE(S):

(1) RS8254/5 defaults to UTOPIA Level 2 when reset causing the TxClAv, RxClAv, RxSOC, and RxPrty signals to be in high-impedance state. This may cause initialization problems for ATM layer UTOPIA Level 1 devices. Therefore, it is recommended that pulldown resistors be used for these devices.

Table A-1. RS8254/5 Pin Definitions *(10 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Receive (cont.)	URxClAv (a) (b) (c) (d)	UTOPIA Receive Cell Available (PHY a, b, c, d)	 AE13 AD26 B18 F1	TTL	O	This signal indicates FIFO empty or Cell Buffer Available. For octet-level flow control, this signal is active low from the PHY layer to the ATM layer. It is asserted to indicate that in the current cycle there is no valid data for delivery to the ATM layer. For cell-level flow control in an multi-PHY environment, URxClAv is an active high signal with high impedance potential going from the multi-PHY layer to the ATM layer. A polled multi-PHY device drives this signal only during each cycle following one with its address on the URxAddr lines. The polled multi-PHY device asserts URxClAv high to indicate it has a complete cell available for transfer to the ATM layer, otherwise it deasserts the signal.(1)
Supply Voltage	PWR	Supply Voltage	G6 H6 W6 Y6 F7 J7 V7 AA7 F8 J8 V8 AA8 G9 H9 W9 Y9 G18 H18 W18 Y18 F19 J19 V19 AA19 F20 J20 V20 AA20 G21 H21 W21 Y21	—	—	These pins are power supply connections.
	Analog PWR	Analog Supply Voltage	—	—	—	This pin is an analog power supply connection.

NOTE(S):
(1) RS8254/5 defaults to UTOPIA Level 2 when reset causing the TxClAv, RxClAv, RxSOC, and RxPrty signals to be in high-impedance state. This may cause initialization problems for ATM layer UTOPIA Level 1 devices. Therefore, it is recommended that pulldown resistors be used for these devices.

Table A-1. RS8254/5 Pin Definitions *(11 of 11)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Supply Voltage (cont.)	GND	Ground	F6 J6 V6 AA6 G7 H7 W7 Y7 G8 H8 W8 Y8 F9 J9 V9 AA9 F18 J18 V18 AA18 G19 H19 W19 Y19 G20 H20 W20 Y20 F21 J21 V21 AA21	—	—	These pins are ground connections.
	Analog GND	Analog Ground	(2)	—	—	This pin is an analog ground connection.
	V_{GG}	Electrostatic Discharge (ESD) Supply Voltage	D2 F26 AE23	—	—	This pin is an ESD supply connection. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using in a 3.3 V system only, leave this pin unconnected.

NOTE(S):

(1) RS8254/5 defaults to UTOPIA Level 2 when reset, causing the TxClAv, RxClAv, RxSOC, and RxPrty signals to be in high-impedance state. This may cause initialization problems for ATM layer UTOPIA Level 1 devices. Therefore, it is recommended that pulldown resistors be used for these devices.

(2) The BGA package does not have separate analog and ground pins. All power and ground balls are connected to common power and ground planes in the substrate.

A.2 RS8254/5 Register Map

There are seven primary address pins, Addr[6:0], which designate the 128 address locations on each port of the device. To accommodate multiple PHY parts; i.e., RS8254/5, a total of nine pins are allocated for addressing. The 8th and 9th address bits determine which port is being accessed. The remaining address bits point to the same register on each device. The following formula is used to determine an address on a specific port:

multi-phy address = single address + 0x80 (register map size) x n (port number)

where: n = 0 for a single device
n = 0–1 for a dual device
n = 0–3 for a quad device

Addressing for the various PHY parts is further described in Table A-2.

Table A-2. Multi-PHY Addressing

Part Number	Port Number	Hex Address Range	Address Range
RS8250/1/2/3/4/5	First Port (0)	00 – 7F	000000000 – 001111111
RS8254/5	Second Port (1)	80 – FF	010000000 – 011111111
RS8254/5	Third Port (2)	100 – 17F	100000000 – 101111111
RS8254/5	Fourth Port (3)	180 – 1FF	110000000 – 111111111

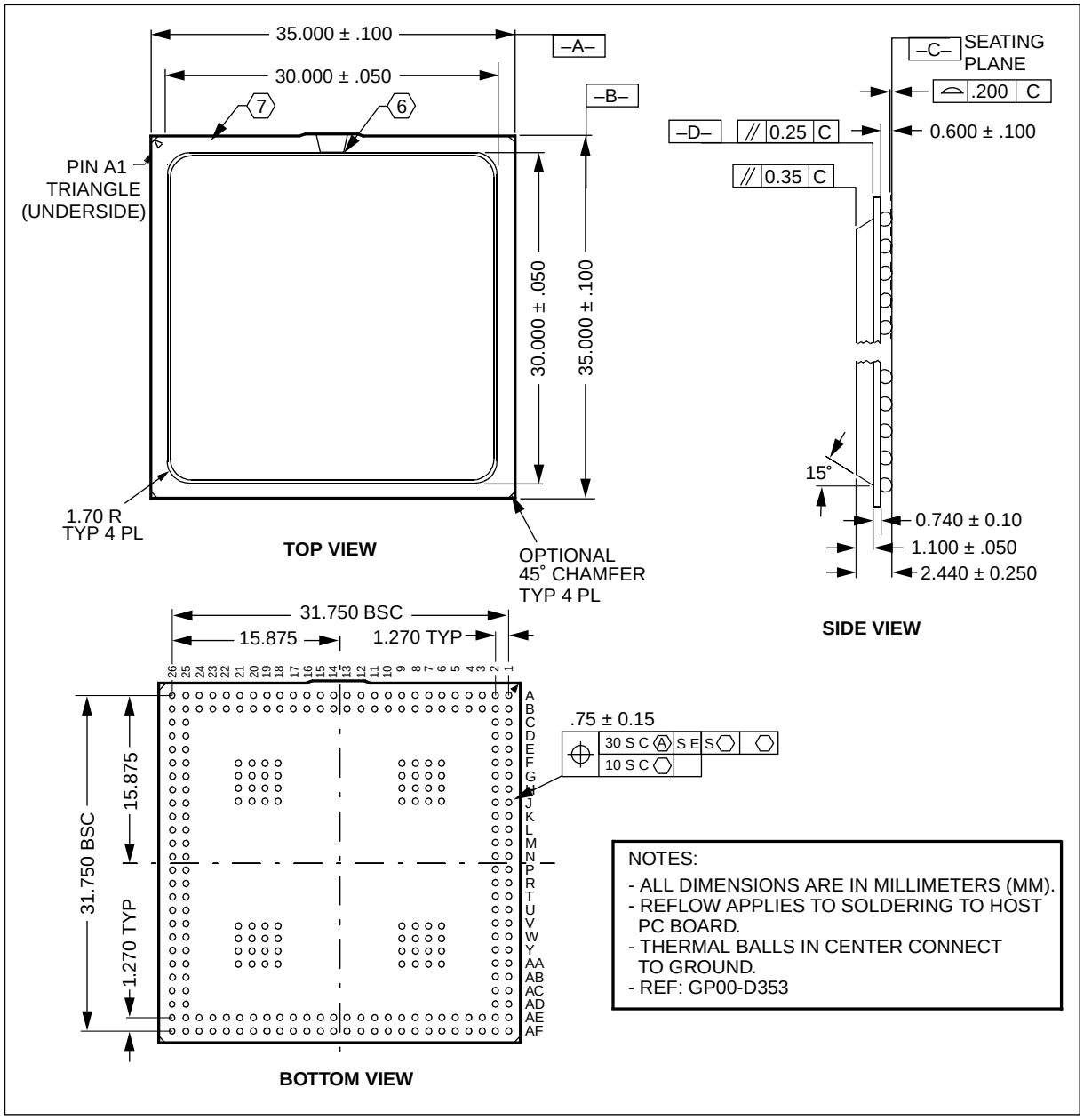
A.3 RS8254/5 Electrical and Mechanical Description

The section describes how the RS8254/5's electrical and mechanical characteristics differ from the RS8251 single device. The timing, absolute maximum ratings, and DC characteristics are the same for the single, dual and quad versions of this product.

A.3.1 RS8254/5 Mechanical Drawing

The RS8254/5 mechanical drawing is shown in Figure A-2.

Figure A-2. 256-Pin Ball Gate Array Package (BGA) for the RS8254/5



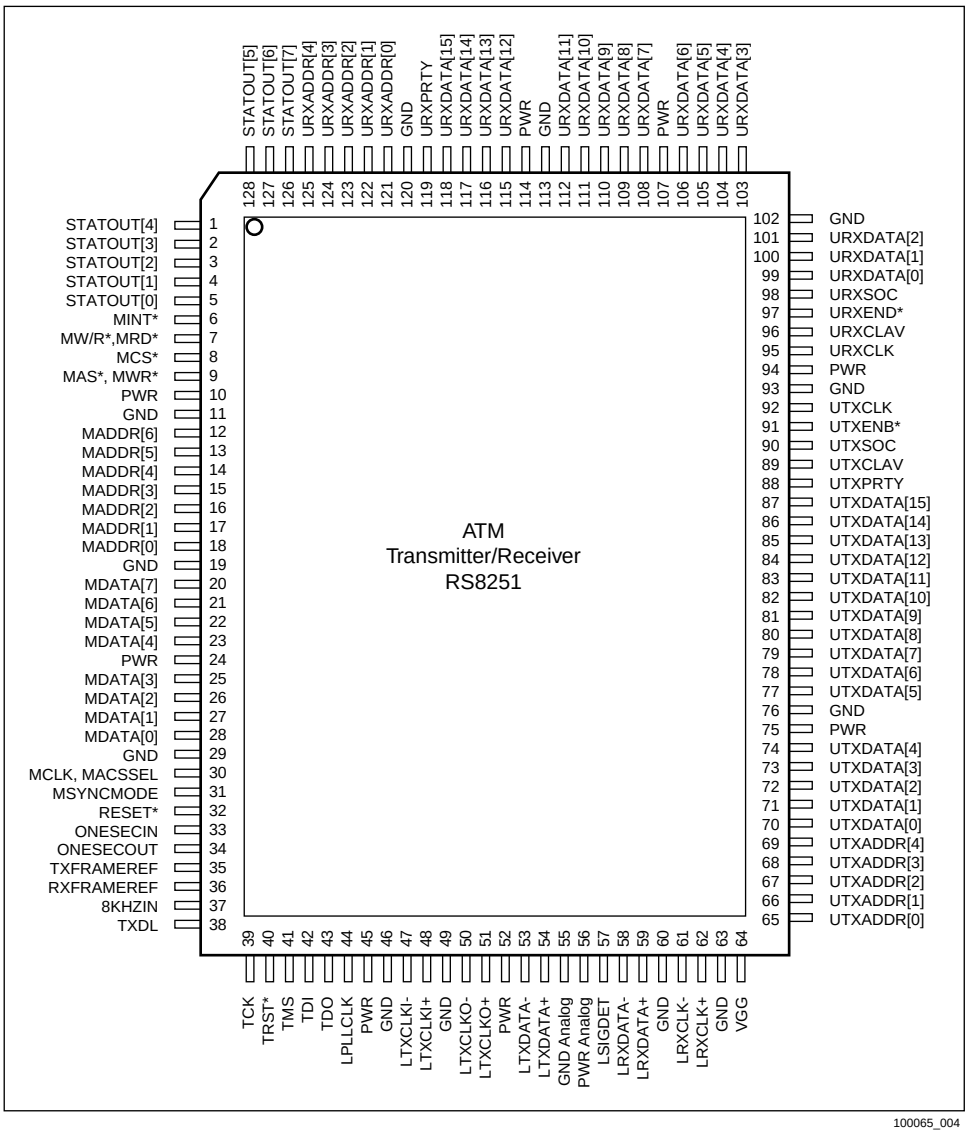
Appendix B RS8250 PHY Device

This appendix describes the RS8250 PHY and how it differs from the RS8251 PHY.

B.1 Pin Diagram and Definitions

Figure B-1 is a pinout diagram for the RS8251 ATM Transmitter/Receiver. It is a single CMOS integrated circuit packaged in a 128-pin TQFP. All unused input pins must be connected to ground. Unused outputs must be left unconnected.

Figure B-1. RS8251 Pinout Diagram



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Pin names and numbers are listed in Table B-1. An asterisk (*) following a pin label indicates that the pin logic level is active low.

Table B-1. RS8251 Pin Definitions *(1 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Clock and Control	Reset*	Device Reset	32	TTL-H	I	This pin is used to reset the device when asserted low.
	OneSecIn	One-Second Strobe	33	TTL	I	This input is used to latch device status, typically at 1-second intervals.
	OneSecOut	One-Second Output	34	TTL	O	This pin is a 1-second count derived from the 8khzIn input (pin 37).
	TxFrameRef	Transmit Frame Clock	35	TTL	O	This pin can be either an 8 kHz output derived from the Transmit SDH frame or a 19.44 MHz output derived from the transmit clock, as selected by bit 1 of the TXSEC (0xOC) register.
	RxFrameRef	Receive Frame Clock	36	TTL	O	This pin can be either an 8 kHz output derived from the Receive SDH frame or a 19.44 MHz output derived from the recovered (receive) clock as selected by bit 1 of the RXSEC (0x45) register.
	8kHzIn	8 kHz Reference Clock Input	37	TTL-H	I	This pin is an 8 kHz clock input used to derive OneSecOut (pin 34).
PMD Line Interface	LTxClkI-	Line Transmit Clock Input Negative Polarity	47	PECL	I	This pin allows use of an externally generated 155.52 MHz clock as selected by bits 3 and 4 in the CLKREC register (0x01). The external source must be accurate to 20 PPM.
	LTxClkI+	Line Transmit Clock Input Positive Polarity	48	PECL	I	This pin allows use of an externally generated 155.52 MHz clock as selected by bits 3 and 4 in the CLKREC register (0x01). The external source must be accurate to 20 PPM.
	LTxClkO-	Line Transmit Clock Output Negative Polarity	50	PECL	O	This pin is a 155.52 MHz output derived from one of four clock sources: LPLLClk, 8kHzIn, Loop-timed, or LTxClkI+/-. The clock source is selected in bits 3 and 4 of the CLKREC register (0x01). It is generally used for diagnostic purposes.
	LTxClkO+	Line Transmit Clock Output Positive Polarity	51	PECL	O	This pin is a 155.52 MHz output derived from one of four clock sources: LPLLClk, 8kHzIn, Loop-timed, or LTxClkI+/-. The clock source is selected in bits 3 and 4 of the CLKREC register (0x01). It is generally used for diagnostic purposes.

Table B-1. RS8251 Pin Definitions *(2 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
PMD Line Interface (Continued)	LTxData-	Line Transmit Output Negative Polarity	53	PECL	O	This pin transfers SDH-framed data from the RS825x to the PMD in differential serial NRZ format.
	LTxData+	Line Transmit Output Positive Polarity	54	PECL	O	This pin transfers SDH-framed data from the RS825x to the PMD in differential serial NRZ format.
	LRxClk-	Line Receive Clock Negative	61	PECL	I	This pin is the receive clock input used if internal clock recovery is bypassed.
	LRxClk+	Line Receive Clock Positive	62	PECL	I	This pin is the receive clock input used if internal clock recovery is bypassed.
	LRxData-	Line Receive Input Negative	58	PECL	I	This pin receives differential serial NRZ data from the PMD.
	LRxData+	Line Receive Input Positive	59	PECL	I	This pin receives differential serial NRZ data from the PMD.
	LSigDet	Line Signal Detection	57	TTL or PECL	I	This pin is normally connected to the Signal Valid output of the PMD and must be asserted high when the PMD is receiving a valid signal. Designs that do not use a Signal Valid from the PMD must tie this intput high. Conexant recommends that a comparator be used when interfacing to PMDs with PECL outputs in Rev. 13 or older devices.
	LPLLClk	Line Phase Locked Loop Clock	44	TTL-H	I	This pin is a 19.44 MHz clock input. The transmit synthesizer (PLL) uses this clock to generate 155.52 MHz LTxClkO output when bits 3 and 4 of the CLKREC register (0x01) are set to 0. ***NOTE:*** The transmit synthesizer PLL and clock recovery PLL use this input as a reference clock regardless of the timing source selection.

Table B-1. RS8251 Pin Definitions *(3 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Microprocessor Interface	MSyncMode	Microprocessor Synchronous/Asynchronous Bus Mode Select	31	TTL	I	A logic 1 selects the synchronous bus mode compatible with Bt8230 and Bt8233. In this mode, the microprocessor pins are defined as follows: MClk (pin 30), MW/R* (pin 7), MAs* (pin 9), MCs* (pin 8), MInt* (pin 6), MAddr (pins 12-18), and MData (pins 20-28). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MAcsSel (pin 30), MRd* (pin 7), MWr* (pin 9), MCs* (pin 8), MInt* (pin 6), MAddr (pins 12-18), and MData (pins 20-28).
	MClk, MAcsSel	Microprocessor Clock, Access Time Select	30	TTL-H	I	When MSyncMode is set to a logic 1, the MClk pin is a clock signal that samples the microprocessor interface pins (MCs*, MW/R*, MAs*, MAddr[6:0], MData[7:0]) on its rising edge. Additionally, the rising edge of MClk may cause the microprocessor interface output pins (MData[7:0], MInt*) to change states. When MSyncMode is set to a logic 0, the MAcsSel pin selects the asynchronous interface access time. A logic 0 selects a power-saving access mode (130 ns) while a logic 1 selects the high-performance access mode (80 ns).
	MCs*	Microprocessor Chip Select	8	TTL-H	I	When MCs* is set to a logic 0, the device is enabled for read and write accesses. When MCs* is set to a logic 1, the device does not respond to input signal transitions on MClk, MAcsSel; MW/R*, MRd*; or MAs*, MWr*. Additionally, when MCs* is set to a logic 1, the MData[7:0] pins are in a high-impedance state, but the MInt* pin remains operational.
	MW/R*, MRd*	Microprocessor Write/Read, Read Control	7	TTL-H	I	When MSyncMode is set to a logic 1, this pin is a read/write control pin. In this mode, when MW/R* is set to a logic 1, a write access is enabled, and the MData[7:0] pin values are written to the memory location indicated by the MAddr[6:0] pins. Also in this mode, when MW/R* is set to a logic 0, a read access is enabled, and the memory location indicated by the MAddr[6:0] pins is read and its value placed on the MData[7:0] pins. Both read and write accesses assume the device is chip selected (MCs* = 0), the address is valid (MAs* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is set to a logic 0, this pin is a read control pin. In this mode, when MRd* is set to a logic 0, a read access is enabled and the memory location indicated by the MAddr[6:0] pins is read and its value placed on the MData[7:0] pins. The read access assumes the device is chip selected (MCs* = 0), a write access is not being requested

Table B-1. RS8251 Pin Definitions *(4 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Microprocessor Interface (Continued)	MAs*,MWr*	Microprocessor Address Strobe, Write Control	9	TTL-H	I	When MSyncMode is set to a logic 1, this pin is an address strobe pin. When the MAs* pin is set to a logic 0, it indicates a valid address, MAddr[6:0]. This signal is used to qualify read and write accesses. When MSyncMode is set to a logic 0, this pin is a write control pin. When MWr* is set to a logic 0, a write access is enabled and the MData[7:0] pin values is written to the memory location indicated by the MAddr[6:0] pins. The write access assumes the device is chip selected (MCs* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1).
	MAddr[6]	Microprocessor Address Bus	12	TTL	I	These 7 bits are an address input for identifying the register that will be accessed.
	MAddr[5]		13	TTL	I	
	MAddr[4]		14	TTL	I	
	MAddr[3]		15	TTL	I	
	MAddr[2]		16	TTL	I	
	MAddr[1]		17	TTL	I	
	MAddr[0]		18	TTL	I	
	MData[7]	Microprocessor Data Bus	20	TTL	I/O	These 8 bits are a bidirectional data bus for transferring the read and write data.
	MData[6]		21	TTL	I/O	
	MData[5]		22	TTL	I/O	
	MData[4]		23	TTL	I/O	
	MData[3]		25	TTL	I/O	
	MData[2]		26	TTL	I/O	
	MData[1]		27	TTL	I/O	
	MData[0]		28	TTL	I/O	
	MInt*	Microprocessor Interrupt	6	TTL	O	When a logic 0 is read on this pin, the device needs servicing. It remains asserted until the pending interrupt is acknowledged. This pin is an open drain output for an external wired OR logic implementation.

Table B-1. RS8251 Pin Definitions *(5 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
JTAG (See IEEE 1149.1a-1993)	TRST*	Test Reset	40	TTL	I	When this pin is asserted, the internal boundary-scan logic is reset. This pin has a pullup resistor.
	TCK	Test Clock	39	TTL	I	This pin samples the value of TMS and TDI on its rising edge in order to control the boundary scan operations.
	TMS	Test Mode Select	41	TTL pullup	I	This pin controls the boundary-scan Test Access Port (TAP) controller operation.
	TDI	Test Data Input	42	TTL pullup	I	This pin is the serial test data input.
	TDO	Test Data Output	43	TTL	O	This pin is the serial test data output.

Table B-1. RS8251 Pin Definitions *(6 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
Status	StatOut[7]	Status Outputs	126	TTL	O	This pin reflects either the value in bit 7 of the OUTSTAT register (0x41), or LOS, as selected by bit 2 of register GEN (0x00). If selected by bit 0 or 1 of RXLIN (0x46), this pin is the D1-D3 or D4-D12 receive data link serial clock output (RS8250 only).
	StatOut[6]		127	TTL	O	This pin reflects either the value in bit 6 of the OUTSTAT register (0x41), or OOF, as selected by bit 2 of register GEN (0x00). If selected by bit 0 or 1 of RXLIN (0x46), this pin is the D1-D3 or D4-D12 receive data link serial data output (RS8250 only).
	StatOut[5]		128	TTL	O	This pin reflects either the value in bit 5 of the OUTSTAT register (0x41), or LOP, as selected by bit 2 of register GEN (0x00). For RS8250 only: if selected by bit 0 or 1 of RXLIN (0x46), this pin is the D1-D3 or D4-D12 receive data link indication output. This output is high during the time that clock/data outputs contain pulses for D1-D3 octets. It is low during the time that clock/data outputs contain pulses for D4-D12 octets.
	StatOut[4]		1	TTL	O	This pin reflects either the value in bit 4 of the OUTSTAT register (0x41), or AIS-L, as selected by bit 2 of register GEN (0x00). If selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin is the D1-D3 or D4-D12 transmit data link serial clock output (RS8250 only).
	StatOut[3]		2	TTL	O	This pin reflects either the value in bit 3 of the OUTSTAT register (0x41), or RDI-L, as selected by bit 2 of register GEN (0x00). For RS8250 only: if selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin is the D1-D3 or D4-D12 transmit data link indication output. This output is high during the time that clock/data inputs are expected for D1-D3 octets, and low for D4-D12.
	StatOut[2]		3	TTL	O	This pin reflects either the value in bit 2 of the OUTSTAT register (0x41), or AIS-P, as selected by bit 2 of register GEN (0x00). For RS8250 only: if selected by bit 4 of TXLIN (0x0D) or bit 6 of TXSEC (0x0C), this pin outputs a pulse at the beginning of every cell slot time (both idle and data cells), synchronized to the UTOPIA transmit side.
	StatOut[1]		4	TTL	O	This pin reflects either the value in bit 1 of the OUTSTAT register (0x02), or RDI-P, as selected by bit 2 of the GEN register (0x00).
	StatOut[0]		5	TTL	O	This pin reflects either the value in bit 0 of the OUTSTAT register (0x02), or LOCD, as selected by bit 2 of the GEN register (0x00).

Table B-1. RS8251 Pin Definitions *(7 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Transmit	UTxClk	UTOPIA Transmit Clock	92	TTL-H	I	The data transfer/interface clock is provided by the ATM layer to the PHY layer for synchronizing transfers on UTxData.
	UTxEnb*	UTOPIA Transmit Enable	91	TTL	I	The enable data transfers signal is active low. It is asserted by the ATM layer during cycles when UTxData contains valid cell data.
	UTxAddr[0]	LSB	65	TTL	I	These pins are the address of the PHY device being selected. The address is driven from the ATM to the multi-PHY layer to poll and select the appropriate multi-PHY device. Each multi-PHY device must maintain its address. Address 31 indicates a null PHY port.
	UTxAddr[1]		66	TTL	I	
	UTxAddr[2]	UTOPIA Transmit Address	67	TTL	I	
	UTxAddr[3]		68	TTL	I	
	UTxAddr[4]	MSB	69	TTL	I	
	UTxData[0]	UTOPIA Transmit Data	70	TTL	I	The data bus is driven from the ATM layer to the PHY. UTxData[15] is the MSB of the high octet, and UTxData[7] is the MSB of the lower octet.
	UTxData[1]		71	TTL	I	
	UTxData[2]		72	TTL	I	
	UTxData[3]		73	TTL	I	
	UTxData[4]		74	TTL	I	
	UTxData[5]		77	TTL	I	
	UTxData[6]		78	TTL	I	
	UTxData[7]		79	TTL	I	
	UTxData[8]		80	TTL	I	
	UTxData[9]		81	TTL	I	
	UTxData[10]		82	TTL	I	
	UTxData[11]		83	TTL	I	
	UTxData[12]		84	TTL	I	
	UTxData[13]		85	TTL	I	
	UTxData[14]		86	TTL	I	
	UTxData[15]		87	TTL	I	
	UTxPrty	UTOPIA Transmit Parity Input	88	TTL	I	The transmit data bus checks for odd parity over UTxData [7:0] coming from the ATM layer. In 16-bit mode, it checks for odd parity over UTxData[15:0].

Table B-1. RS8251 Pin Definitions *(8 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Transmit (cont.)	UTxSOC	UTOPIA Transmit Start of Cell	90	TTL	I	The Start of Cell signal is active high. It is asserted by the ATM layer during cycles when UTxData contains the first valid byte of the cell.
	UTxClAv	UTOPIA Transmit Cell Available	89	TTL	O	This signal indicates FIFO full or Cell Buffer Available. For octet-level flow control, this signal is active low from the PHY layer to the ATM layer. It is asserted to indicate that a maximum of four more transmit data writes are accepted. For cell-level flow control in a multi-PHY environment, UTxClAv is an active high signal with high impedance potential going from the multi-PHY layer to the ATM layer. A polled multi-PHY device drives this signal only during each cycle following one with its address on the UTxAddr lines. The polled multi-PHY device asserts UTxClAv high to indicate it can accept the transfer of a complete cell; otherwise, it deasserts the signal.(1)
UTOPIA Receive	URxClk	UTOPIA Receive Clock	95	TTL-H	I	The data transfer/interface clock is provided by the ATM layer to the PHY layer for synchronizing transfers on URxData.
	URxEnb*	UTOPIA Receive Enable	97	TTL	I	The Enable receive data signal is active low. It is asserted by the ATM layer to indicate that URxData and URxSOC are sampled at the end of the next cycle. In support of multiple PHY configurations, when URxEnb* is asserted, the URxData and URxSOC PHY layer outputs change to a high-impedance state. URxData and URxSOC must be enabled only in cycles following those with URxEnb* asserted.
	URxAddr[0]	UTOPIA Receive Address	121	TTL	I	This is the address of the PHY device being selected. It is driven from the ATM to the multi-PHY layer to poll and select the appropriate multi-PHY device. URxAddr [4] is the MSB. Each multi-PHY device must maintain its address. Address 31 indicates a null PHY port.
	URxAddr[1]		122	TTL	I	
	URxAddr[2]		123	TTL	I	
	URxAddr[3]		124	TTL	I	
	URxAddr[4]		125	TTL	I	

Table B-1. RS8251 Pin Definitions *(9 of 10)*

	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Receive (cont.)	URxData[0]	UTOPIA Receive Data Bus	99	TTL	O	The data bus is driven from the ATM layer to the PHY layer. URxData[15] is the MSB of the high octet, and URxData[7] is the MSB of the lower octet. To support multiple PHY configurations, URxData can be placed in a high-impedance state that is enabled only when URxEnb* is asserted.
	URxData[1]		100	TTL	O	
	URxData[2]		101	TTL	O	
	URxData[3]		103	TTL	O	
	URxData[4]		104	TTL	O	
	RxData[5]		105	TTL	O	
	URxData[6]		106	TTL	O	
	URxData[7]		108	TTL	O	
	URxData[8]		109	TTL	O	
	URxData[9]		110	TTL	O	
	URxData[10]		111	TTL	O	
	URxData[11]		112	TTL	O	
	URxData[12]		115	TTL	O	
	URxData[13]		116	TTL	O	
	URxData[14]		117	TTL	O	
	URxData[15]		118	TTL	O	
	URxPrty	UTOPIA Receive Parity	119	TTL	O	The data bus parity is odd parity for URxData[7:0], driven by the PHY layer. In 16-bit mode, this is the odd parity bit over URxData[15:0]. To support multiple PHY configurations, URxPrty can be placed in a high-impedance state which is enabled only in cycles following those with URxEnb* asserted.(1)
	URxSOC	UTOPIA Receive Start of Cell	98	TTL	O	The Start of Cell signal is active high. It is asserted by the PHY layer when URxData contains the first valid byte of the cell. In support of multiple PHY configurations, when URxEnb* is asserted, the URxData and URxSOC PHY layer outputs change to a high-impedance state. URxData and URxSOC must be enabled only in cycles following those with URxEnb* asserted.(1)

Table B-1. RS8251 Pin Definitions *(10 of 10)*

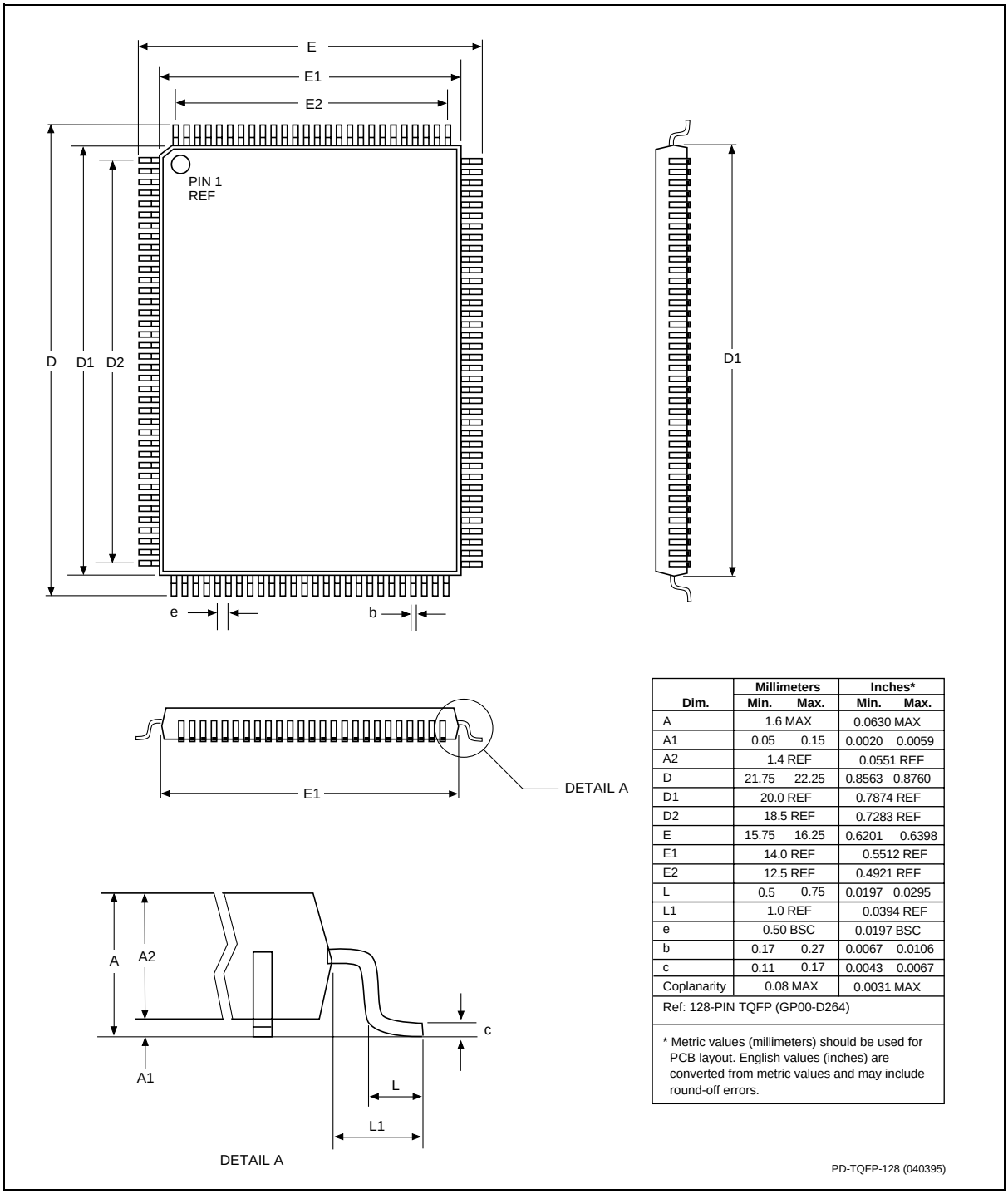
	Pin Label	Signal Name	No.	Type	I/O	Description
UTOPIA Receive (cont.)	URxClAv	UTOPIA Receive Cell Available	96	TTL	O	This signal indicates FIFO empty or Cell Buffer Available. For octet-level flow control, this signal is active low from the PHY layer to the ATM layer. It is asserted to indicate that in the current cycle there is no valid data for delivery to the ATM layer. For cell-level flow control in a multi-PHY environment, URxClAv is an active high signal with high impedance potential going from the multi-PHY layer to the ATM layer. A polled multi-PHY device drives this signal only during each cycle following one with its address on the URxAddr lines. The polled multi-PHY device asserts URxClAv high to indicate it has a complete cell available for transfer to the ATM layer; otherwise, it deasserts the signal.(1)
Supply Voltage	PWR	Supply Voltage	10 24 45 52 75 94 107 114	—	—	These pins are power supply connections.
	Analog PWR	Analog Supply Voltage	56	—	—	This pin is an analog power supply connection.
	GND	Ground	11 19 29 46 49 60 63 76 93 102 113 120	—	—	These pins are ground connections.
	Analog GND	Analog Ground	55	—	—	This pin is an analog ground connection.
	V_{GG}	Electrostatic Discharge (ESD) Supply Voltage	64	—	—	This pin is an ESD supply connection. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using in a 3.3 V system only, leave this pin unconnected.

NOTE(S):
(1) RS825x defaults to UTOPIA Level 2 when reset causing the TxClAv, RxClAv, RxSOC, and RxPrty signals to be in high-impedance state. This may cause initialization problems for ATM layer UTOPIA Level 1 devices. Therefore, it is recommended that pulldown resistors be used for these devices.
(2) TTL-H indicates that the pin has hysteresis.

B.2 Mechanical Drawing

The RS8251 is a 128-pin TQFP. A mechanical drawing of the device is provided in Figure B-2.

Figure B-2. RS8251 Mechanical Drawing



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	21.75	22.25	0.8563	0.8760
D1		20.0 REF		0.7874 REF
D2		18.5 REF		0.7283 REF
E	15.75	16.25	0.6201	0.6398
E1		14.0 REF		0.5512 REF
E2		12.5 REF		0.4921 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.50 BSC		0.0197 BSC
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.08 MAX		0.0031 MAX

Ref: 128-PIN TQFP (GP00-D264)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-128 (040395)

100065_045

Appendix C Related Standards

The following is a list of standards relevant to the RS8251/2/3/4/5.

- ATM Forum UNI Specification 94/0317:
- ATM Forum—ATM User Network Interface Spec. V3.1, Sept. 1994
- ATM Forum Utopia Level 1 Specification, Ver. 2.01, af-phy-0017.000
- ATM Forum Utopia Level 2 Specification, Ver. 1.0, af-phy-0039.000
- ATM Forum—ATM-PHY/95-0766R2: WIRE Specification
- Bellcore Specification T1S1/92-185
- Bellcore Spec. GR-253-CORE: Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, Issue 1, Dec. 1994
- ITU Recommendation I.432, "B-ISDN User Network Interface—Physical Interface Specification," June 1990
- ITU Recommendation G.709, "Synchronous Multiplexing Structure," 1990
- ITU Recommendation G.804, "ATM Cell Mapping into Pleisiochronous Digital Hierarchy (PDH)"
- ITU Recommendation Q.921: ISDN User-Network Interface Data Link Layer Specification, 03/93
- ANSI T1.105: Synchronous Optical Network (SONET)—Basic Description Including Multiplex Structure, Rates and Formats, 1995
- ANSI T1.627-1993: Broadband ISDN—ATM Layer Functionality and Specification
- I.610: B-ISDN Operation and maintenance Principles and Functions
- GR-1248: Generic Requirements for Operation of ATM Network Elements

All of these documents can be obtained from the following companies:

Bellcore
Customer Service
8 Corporate Place - Room 3C-183
Piscataway, NJ 08854-4156
1-800-521-CORE

For *ITU* documents:
Omnicom
Phillips Business Information
1201 Seven Locks Road,
Suite 300
Potomac, MD 20854
1-800 OMNICOM (666-4266)

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
1-800-433-5177
1-503-797-4207

ATM FORUM
The ATM Forum
303 Vintage Park Drive
Foster City, CA 94404-1138

ANSI
11 West 42nd Street
New York, NY 10036
1-212-642-4900

Appendix D Register Summary

This appendix is a quick reference to the RS825x registers. It lists all of the registers and the bits that are contained in each one.

Table D-1. RS825x Register Summary *(1 of 8)*

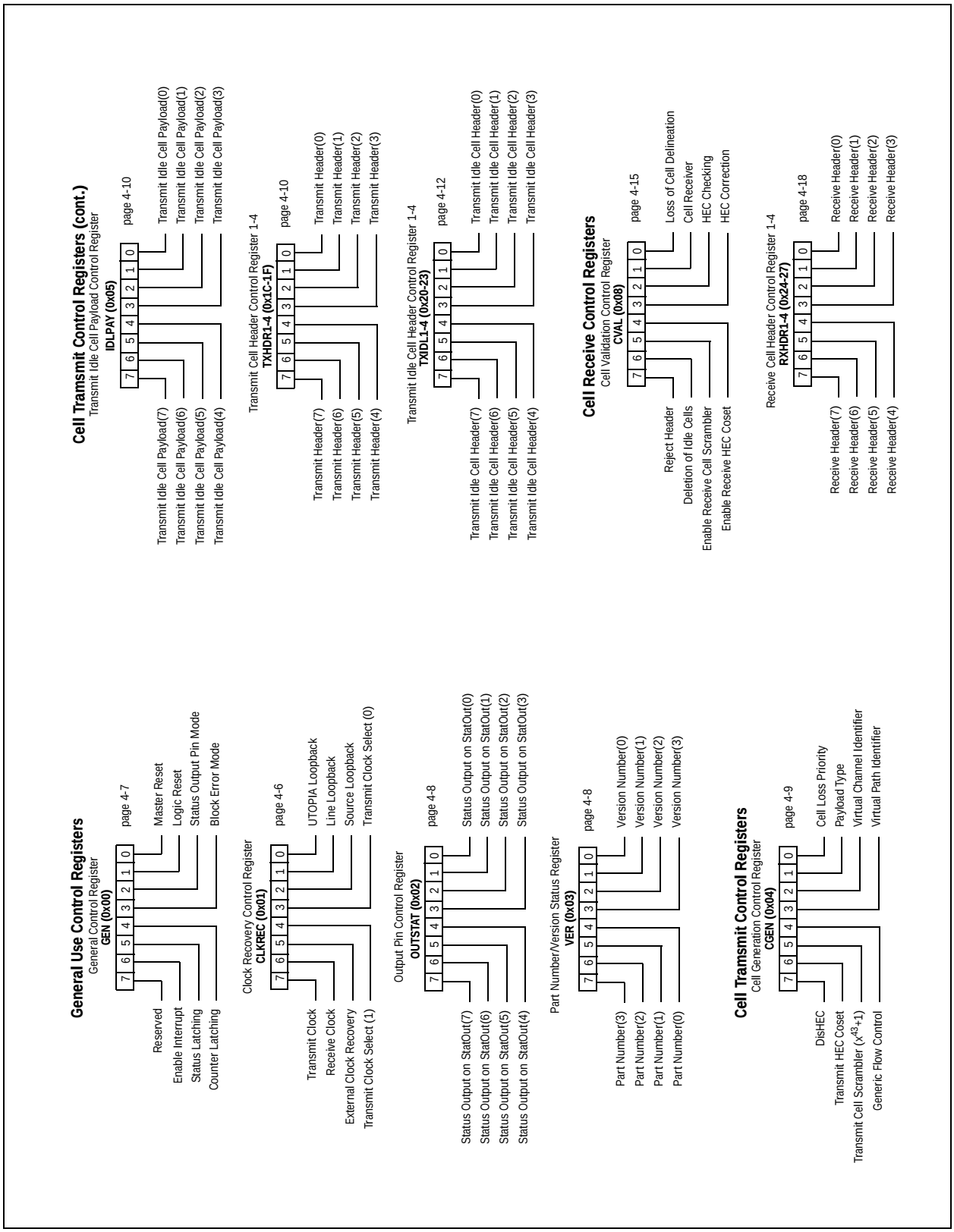


Table D-1. RS825x Register Summary *(2 of 8)*

Table D-1. RS825x Register Summary *(3 of 8)*

Table D-1. RS825x Register Summary *(4 of 8)*

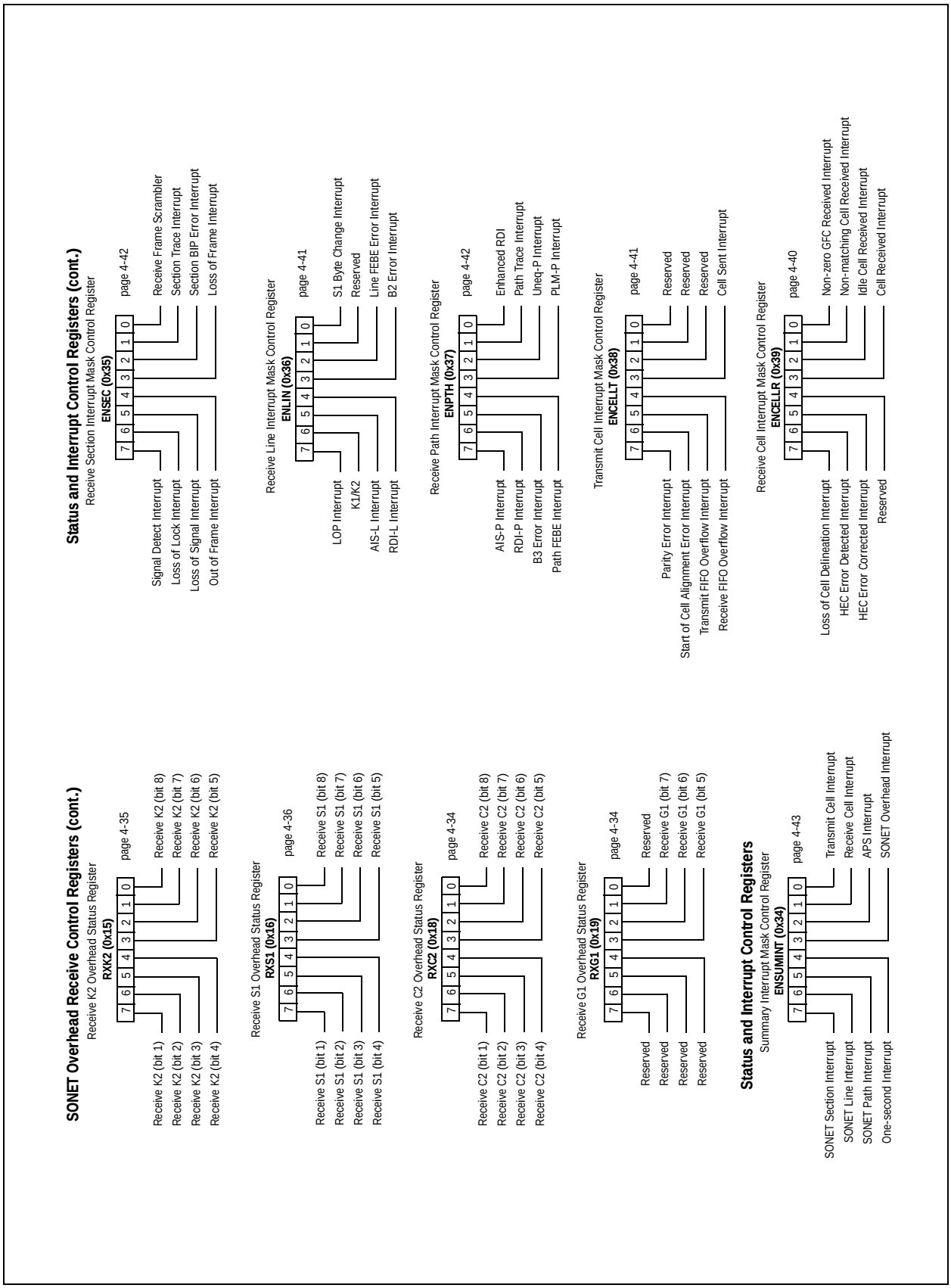


Table D-1. RS825x Register Summary *(5 of 8)*

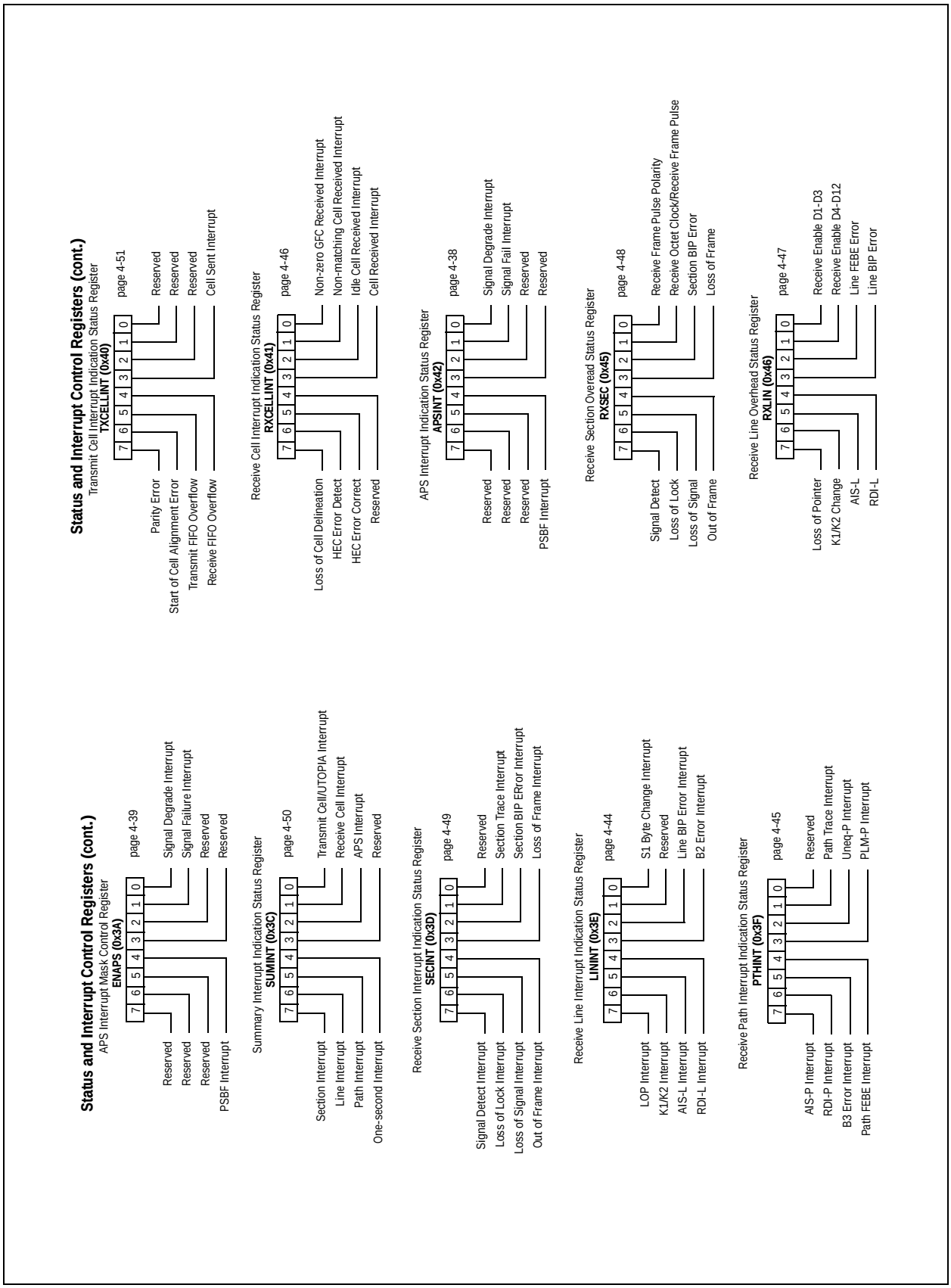


Table D-1. RS825x Register Summary *(6 of 8)*

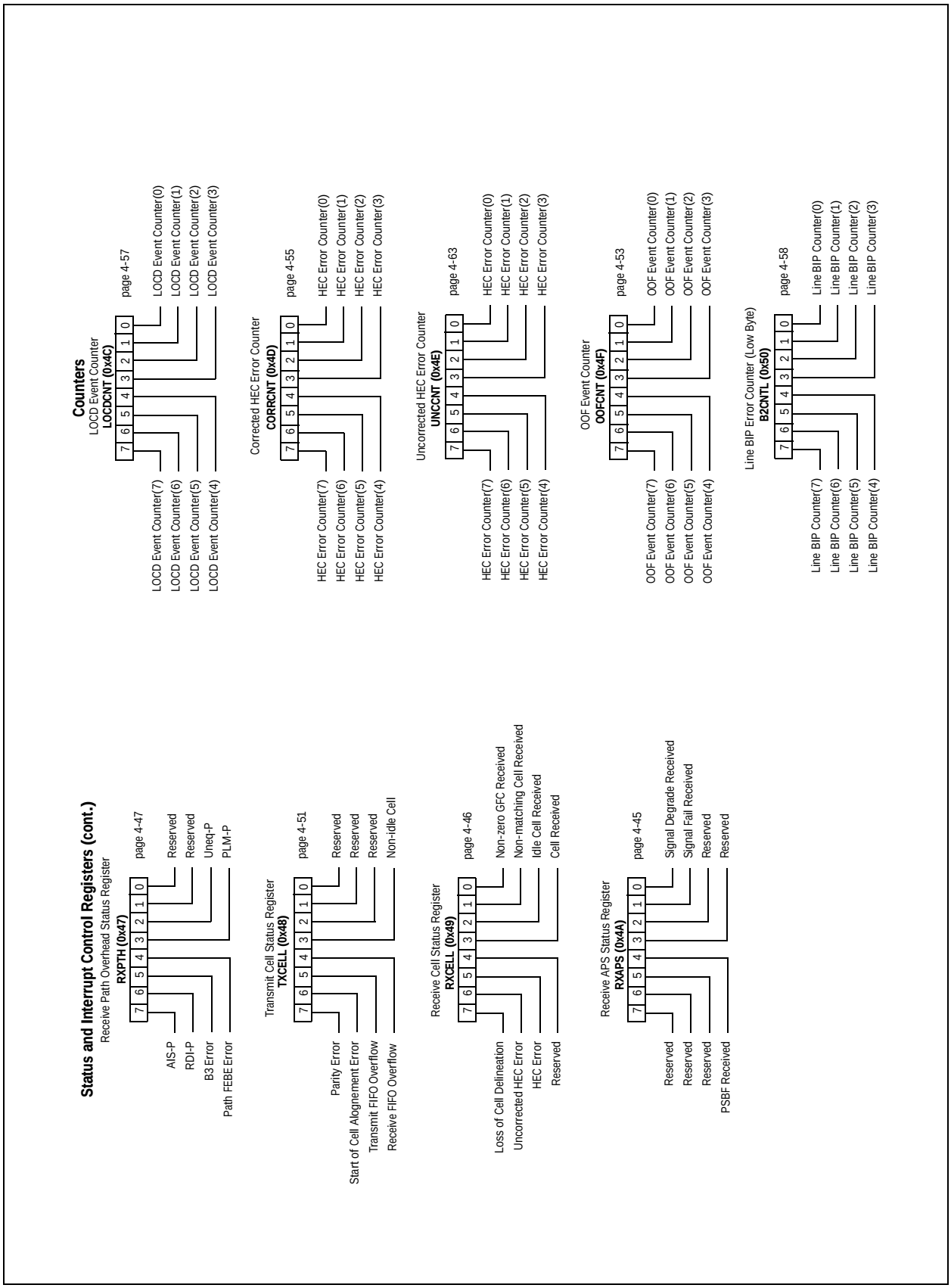


Table D-1. RS825x Register Summary *(7 of 8)*

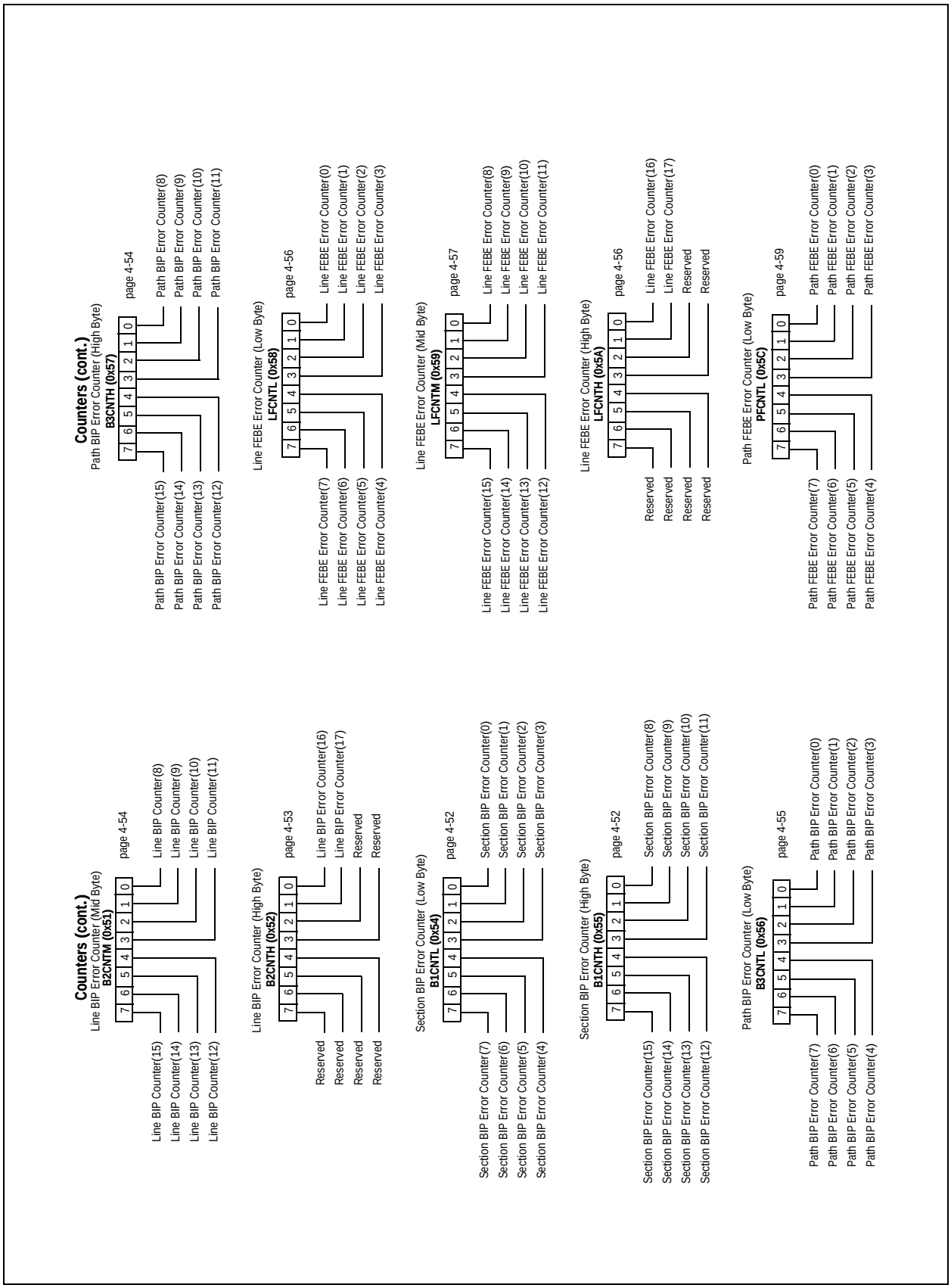
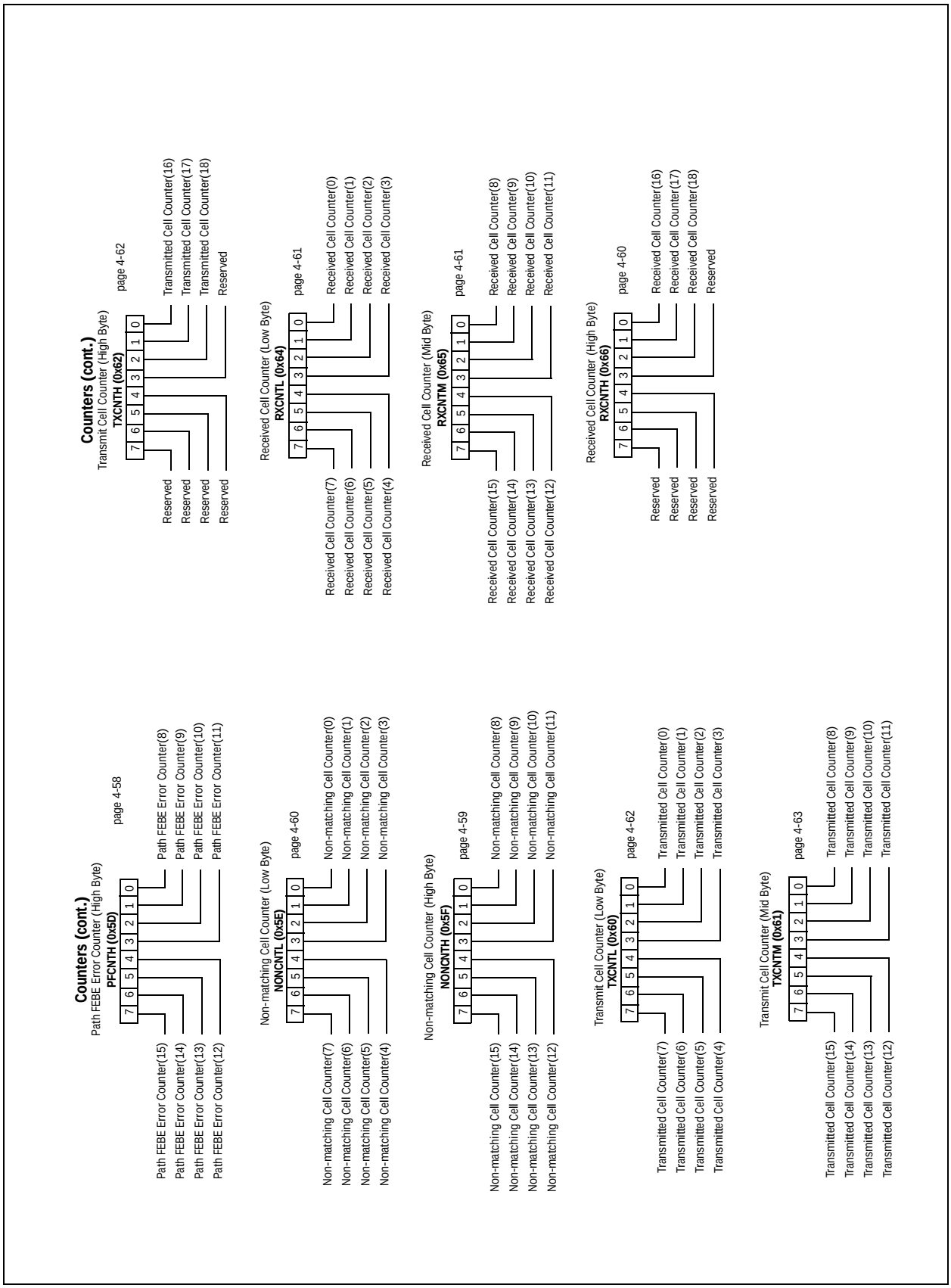


Table D-1. RS825x Register Summary *(8 of 8)*



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