



iMC002FLKA 2-MBYTE FLASH MEMORY CARD

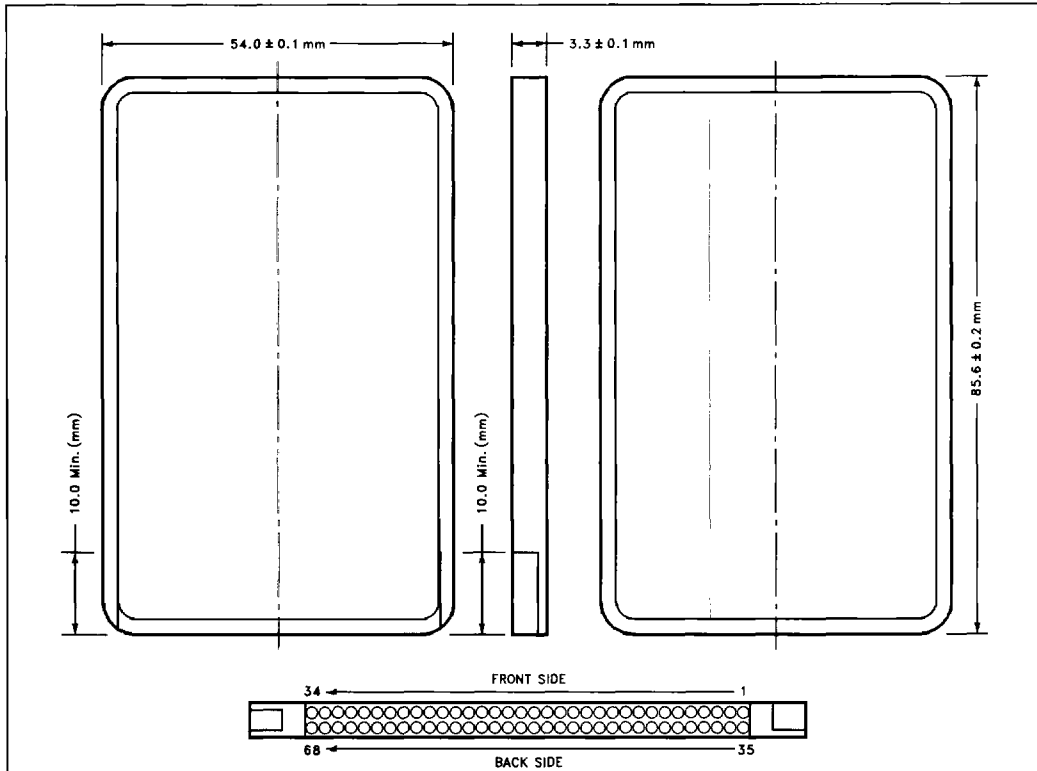
- **Inherent Nonvolatility (Zero Retention Power)**
 - No Batteries Required for Back-up
- **High-Performance Read**
 - 200 ns Maximum Access Time
- **CMOS Low Power Consumption**
 - 25 mA Typical Active Current (X8)
 - 400 μ A Typical Standby Current
- **Flash Electrical Zone-Erase**
 - 2 Seconds Typical per 256 Kbyte Zone
 - Multiple Zone-Erase
- **Random Writes to Erased Zones**
 - 10 μ s Typical Byte Write
- **Write Protect Switch to Prevent Accidental Data Loss**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **ETOX™ II Flash Memory Technology**
 - 5V Read, 12V Erase/Write
 - High-Volume Manufacturing Experience
- **PCMCIA/JEIDA 68-Pin Standard**
 - Byte- or Word-wide Selectable
- **Independent Software & Hardware Vendor Support**
 - Integrated System Solution Using Flash Filing Systems

Intel's iMC002FLKA Flash Memory Card is the removable solution for storing and transporting important user data and application code. The combination of rewritability and nonvolatility make the Intel Flash Memory Card ideal for data acquisition and updatable firmware applications. Designing with Intel's Flash Memory Card enables OEM system manufacturers to produce portable and dedicated function systems that are higher performance, more rugged, and consume less power.

The iMC002FLKA conforms to the PCMCIA 1.0 international standard, providing standardization at the hardware and data interchange level. OEMs may opt to write the Card Information Structure (CIS) at the memory card's address 00000H with a format utility. This information provides data interchange functional capability. The 200 ns access time allows for "execute-in-place" capability, for popular low-power microprocessors. Intel's 2-MByte Flash Memory Card operates in a byte-wide and word-wide configuration providing performance/power options for different systems.

Intel's Flash Memory card employs Intel's ETOX II Flash Memories. Filing systems, such as Microsoft's* Flash File System (FFS), facilitate data file storage and card erasure using a purely nonvolatile medium in the DOS environment. Flash filing systems, coupled with the Intel Flash Memory Card, effectively create an all-silicon nonvolatile read/write random access memory system that is more reliable and higher performance than disk-based memory systems.

*Microsoft is a trademark of Microsoft Corp.



290412-1

1	GND
2	D ₃
3	D ₄
4	D ₅
5	D ₆
6	D ₇
7	CE ₁ #
8	A ₁₀
9	OE#
10	A ₁₁
11	A ₉
12	A ₈
13	A ₁₃
14	A ₁₄
15	WE#
16	NC
17	V _{CC}

18	V _{PP1}
19	A ₁₆
20	A ₁₅
21	A ₁₂
22	A ₇
23	A ₆
24	A ₅
25	A ₄
26	A ₃
27	A ₂
28	A ₁
29	A ₀
30	D ₀
31	D ₁
32	D ₂
33	WP
34	GND

35	GND
36	CD ₁ #
37	D ₁₁
38	D ₁₂
39	D ₁₃
40	D ₁₄
41	D ₁₅
42	CE ₂ #
43	NC
44	NC
45	NC
46	A ₁₇
47	A ₁₈
48	A ₁₉
49	A ₂₀
50	NC
51	V _{CC}

52	V _{PP2}
53	NC
54	NC
55	NC
56	NC
57	NC
58	NC
59	NC
60	NC
61	REG#
62	BVD ₂ # ²
63	BVD ₁ # ²
64	D ₈
65	D ₉
66	D ₁₀
67	CD ₂ #
68	GND

6

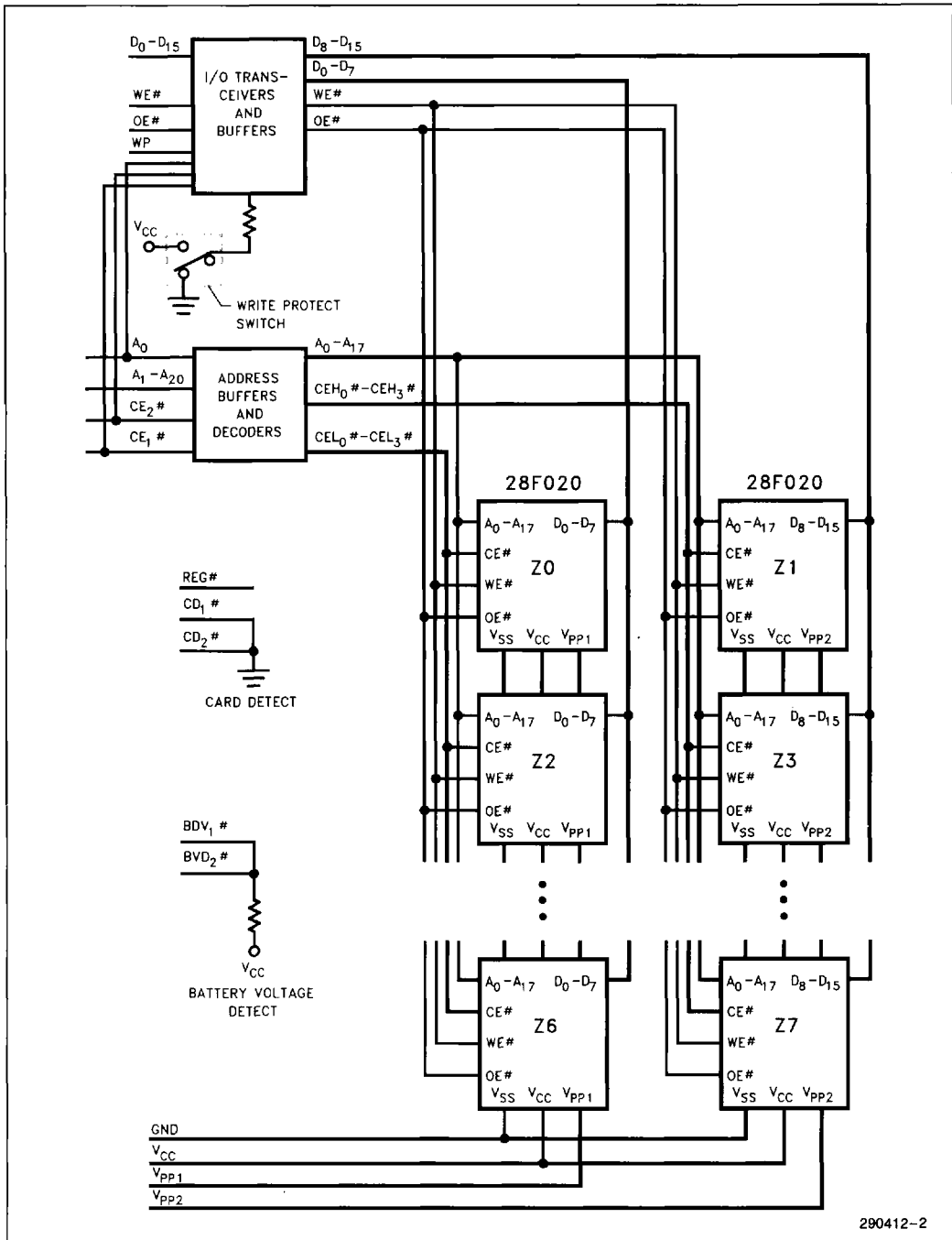
NOTES:

1. REG# = register memory select = No Connect (NC), unused. When REG# is brought low, PCMCIA/JEIDA standard card information structure data is expected. This is accomplished by formatting the card with this data.
2. BVD# = battery detect voltage = Pulled High through Pull-Up Resistor.

Figure 1. iMC002FLKA Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A ₀ -A ₂₀	I	ADDRESS INPUTS for memory locations. Addresses are internally latched during a write cycle.
D ₀ -D ₁₅	I/O	DATA INPUT/OUTPUT: Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the card is deselected or the outputs are disabled. Data is internally latched during a write cycle.
CE ₁ #, CE ₂ #	I	CARD ENABLE: Activates the card's high and low byte control logic, input buffers, zone decoders, and associated memory devices. CE # is active low; CE # high deselects the memory card and reduces power consumption to standby levels.
OE #	I	OUTPUT ENABLE: Gates the cards output through the data buffers during a read cycle. OE # is active low.
WE #	I	WRITE ENABLE controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the WE # pulse. NOTE: With V _{PP} ≤ 6.5V, memory contents cannot be altered.
V _{PP1} , V _{PP2}		ERASE/WRITE POWER SUPPLY for writing the command register, erasing the entire array, or writing bytes in the array.
V _{CC}		DEVICE POWER SUPPLY (5V ± 5%).
GND		GROUND
CD ₁ #, CD ₂ #	O	CARD DETECT. The card is detected at CD _{1/2} # = ground.
WP	O	WRITE PROTECT. All write operations are disabled with WP = active high.
NC		NO INTERNAL CONNECTION to device. Pin may be driven or left floating.
BVD ₁ #, BVD ₂ #	O	BATTERY VOLTAGE DETECT. NOT REQUIRED.



6

Figure 2. IMC002FLKA Block Diagram

290412-2

APPLICATIONS

The iMC002FLKA Flash Memory Card allows for the storage of data and application programs on a purely solid-state removable medium. System resident flash filing systems, such as Microsoft's Flash File System, allow Intel's ETOX II highly reliable Flash Memory Card to effectively function as a physical disk drive.

User application software stored on the flash memory card substantially reduces the slow disk-DRAM download process. Replacing the disk results in a dramatic enhancement of read performance and substantial reduction of active power consumption, size, and weight—considerations particularly important in portables and dedicated systems. The iMC002FLKA's high performance read access time and command register microprocessor write interface allows for use of the flash memory system in an "execute-in-place" architecture. This configuration eliminates the need for the redundancy associated with DRAM and Disk memory system architectures. ROM based operating systems, such as Microsoft's MS-DOS ROM Version allow for "instant-on" capability. This enables the design of systems that boot, operate, store data files, and execute application code from/to purely nonvolatile memory.

The PCMCIA/JEIDA 68-pin interface with flash filing systems enables the end-user to transport data and application code between portables and host systems. Intel Flash Memory Cards provide durable nonvolatile memory storage protecting valuable user code and data.

For systems currently using a static RAM/battery configuration for data acquisition, the iMC002FLKA's inherent nonvolatility eliminates the need for battery backup. The concern of battery failure no longer exists, an important consideration for portable computers and medical instruments, both requiring continu-

ous operation. The iMC002FLKA consumes no power when the system is off. In addition, the iMC002FLKA offers a considerable cost and density advantage over memory cards based on static RAM with battery backup.

The flash memory card's electrical zone-erasure, byte writability, and complete nonvolatility fit well with data accumulation and recording needs. Electrical zone-erasure gives the designer the flexibility to selectively rewrite zones of data while saving other zones for infrequently updated look-up tables, for example.

PRINCIPLES OF OPERATION

Intel's Flash Memory Card combines the functionality of two mainstream memory technologies: the rewritability of RAM and the nonvolatility of EPROM. The flash memory card consists of an array of individual memory devices, each of which defines a physical zone. The iMC002FLKA's memory devices erase as individual blocks, equivalent in size to the 256 Kbyte zone. Multiple zones can be erased simultaneously provided sufficient current for the appropriate number of zones (memory devices). Note, multiple zone erasure requires higher current from both the V_{PP} and V_{CC} power supplies. Erased zones can then be written in bit- or byte-at-a-time fashion and read randomly like RAM. Bit level write capability also supports disk emulation.

In the absence of high voltage on the $V_{PP1/2}$ pins, the iMC002FLKA remains in the read-only mode. Manipulation of the external memory card-control pin yields the standard read, standby, and output disable operations.

The same read, standby, and output disable operations are available when high voltage is applied to the $V_{PP1/2}$ pins. In addition, high voltage on $V_{PP1/2}$

enables erasure and rewriting of the accessed zone(s). All functions associated with altering zone contents—erase, erase verify, write, and write verify—are accessed via the command register.

Commands are written to the internal memory register(s), decoded by zone size, using standard microprocessor write timings. Register contents for a given zone serve as input to that zone's internal state-machine which controls the erase and rewrite circuitry. Write cycles also internally latch addresses and data needed for write and erase operations. With the appropriate command written to the register(s), standard microprocessor read timings output zone data, or output data for erase and write verification.

Byte-wide or Word-wide Selection

The flash memory card can be read, erased, and written in a byte-wide or word-wide mode. In the word-wide configuration V_{PP1} and/or $CE_1\#$ control the LO-Byte while V_{PP2} and $CE_2\#$ control the HI-Byte ($A_0 = \text{don't care}$).

Read, Write, and Verify operations are byte- or word-oriented, thus zone independent. Erase Setup and Begin Erase Commands are zone dependent such that commands written to any address within a 256 Kbyte zone boundary initiate the erase operation in that zone (or two 256 Kbyte zones under word-wide operation).

Conventional x8 operation uses $CE_1\#$ active-low, with $CE_2\#$ high, to read or write data through the D_0 – D_7 only. “Even bytes” are accessed when A_0 is low, corresponding to the low byte of the complete x16 word. When A_0 is high, the “odd byte” is accessed by transposing the high byte of the complete x16 word onto the D_0 – D_7 outputs. This odd byte corresponds to data presented on D_8 – D_{15} pins in x16 mode.

Note that two zones logically adjacent in x16 mode are multiplexed through D_0 – D_7 in x8 mode and are toggled by the A_0 address. Thus, zone specific erase operations must be kept discrete in x8 mode by addressing even bytes only for one-half of the zone pair, then addressing odd bytes only for the other half.

Card Detection

The flash memory card features two card detect pins ($CD_{1/2}\#$) that allow the host system to determine if the card is properly loaded. Note that the two pins are located at opposite ends of the card. Each $CD\#$ output should be read through a port bit. Should only one of the two bits show the card to be present, then the system should instruct the user to re-insert the card squarely into the socket. Card detection can also tell the system whether or not to redirect drives in the case of system booting. $CD_{1/2}\#$ is active low, internally tied to ground.

Write Protection

The flash memory card features three types of write protection. The first type features a mechanical Write Protect Switch that disables the circuitry that control Write Enable to the flash devices. When the switch is activated, the $WE\#$ internal to the card is forced high, which disables any writes to the Command Register. The second type of write protection is based on the PCMCIA/JEIDA socket. Unique pin length assignments provide protective power supply sequencing during hot insertion and removal. The third type operates via software control through the Command Register when the card resides in its connector. The Command Register of each zone is only active when $V_{PP1/2}$ is at high voltage. Depending upon the application, the system designer may choose to make $V_{PP1/2}$ power supply switchable—available only when writes are desired. When $V_{PP1/2} = V_{PPH}$, the contents of the register default to the read command, making the iMC002FLKA a read-only memory card. In this mode, the memory contents cannot be altered.

The system designer may choose to leave $V_{PP1/2} = V_{PPH}$, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage, V_{LKO} . (See the section on Power Up/Down Protection.) The iMC002FLKA is designed to accommodate either design practice, and to encourage optimization of the processor-memory card interface.

BUS OPERATIONS

Read

The iMC002FLKA has two control functions, both of which must be logically active, to obtain data at the outputs. Card Enable (CE#) is the power control and should be used for high and/or low zone(s) selection. Output Enable (OE#) is the output control and should be used to gate data from the output pins, independent of accessed zone selection. In the byte-wide configuration, only one CE# is required. The word-wide configuration requires both CE#'s active low.

When $V_{PP1/2}$ is high (V_{PPH}), the read operations can be used to access zone data and to access data for write/erase verification. When $V_{PP1/2}$ is low (V_{PPL}), only read accesses to the zone data are allowed.

Output Disable

With Output Enable at a logic-high level (V_{IH}), output from the card is disabled. Output pins are placed in a high-impedance state.

Standby

With one Card Enable at a logic-high level, the standby operation disables one-half of the x16 output's read/write buffer. Further, only the zone corresponding to the selected address within the upper or lower CE_{1/2}# bank is active at a time. (NOTE: A₀ must be low to select the low half of the x16 word when CE₂# = 1 and CE₁# = 0.) All other zones are deselected, substantially reducing card power consumption. For deselected banks, the outputs are placed in a high-impedance state, independent of the Output Enable signal. If the iMC002FLKA is deselected during erasure, writing, or write/erase verification, the accessed zone draws active current until the operation is terminated.

Intelligent Identifier Command

The manufacturer- and device-codes can be read via the Command Register, for instances where the iMC002FLKA is erased and rewritten in a universal reader/writer. Following a write of 90H to a zone's Command Register, a read from address location 00000H on any zone outputs the manufacturer code (89H). A read from address 0002H outputs the memory device code (BDH).

Write

Zone erasure and rewriting are accomplished via the Command Register, when high voltage is applied to $V_{PP1/2}$. The contents of the register serve as input to that zone's internal state-machine. The state-machine outputs dictate the function of the targeted zone.

The Command Register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The Command Register is written by bringing Write Enable to a logic-low level (V_{IL}), while Card Enable(s) is/are low. Addresses are latched on the falling edge of Write Enable, while data is latched on the rising edge of the Write Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Write Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin(s), the contents of the zone Command Register(s) default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin(s) enable(s) read/write operations. Zone operations are selected by writing specific data patterns into the Command Register. Tables 3 and 4 define these iMC002FLKA register commands for both byte-wide and word-wide configurations.

All commands written to the Command Register require that the zone address be valid or the incorrect zone will receive the command. Any Command/Data Write or Data Read requires the correct valid address.

Table 2. Bus Operations

Pins		Notes	[1, 7]	[1, 7]	A0	CE ₂ #	CE ₁ #	OE #	WE #	D ₈ -D ₁₅	D ₀ -D ₇
Operation			V _{PP2}	V _{PP1}							
READ-ONLY	Read (x8)	8	V _{PP_L}	V _{PP_L}	V _{IL}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	Tri-state	Data Out-Even
	Read (x8)	9	V _{PP_L}	V _{PP_L}	V _{IH}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	Tri-state	Data Out-Odd
	Read (x8)	10	V _{PP_L}	V _{PP_L}	X	V _{IL}	V _{IH}	V _{IL}	V _{IH}	Data Out	Tri-state
	Read (x16)	11	V _{PP_L}	V _{PP_L}	X	V _{IL}	V _{IL}	V _{IL}	V _{IH}	Data Out	Data Out
	Output Disable		V _{PP_L}	V _{PP_L}	X	X	X	V _{IH}	V _{IH}	Tri-state	Tri-state
	Standby		V _{PP_L}	V _{PP_L}	X	V _{IH}	V _{IH}	X	X	Tri-state	Tri-state
READ/WRITE	Read (x8)	3, 8	V _{PP_X}	V _{PP_H}	V _{IL}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	Tri-state	Data Out-Even
	Read (x8)	3, 9	V _{PP_H}	V _{PP_X}	V _{IH}	V _{IH}	V _{IL}	V _{IL}	V _{IH}	Tri-state	Data Out-Odd
	Read (x8)	10	V _{PP_H}	V _{PP_X}	X	V _{IL}	V _{IH}	V _{IL}	V _{IH}	Data Out	Tri-state
	Read (x16)	3, 11	V _{PP_H}	V _{PP_H}	X	V _{IL}	V _{IL}	V _{IL}	V _{IH}	Data Out	Data Out
	Write (x8)	5, 8	V _{PP_X}	V _{PP_H}	V _{IL}	V _{IH}	V _{IL}	V _{IH}	V _{IL}	Tri-state	Data In-Even
	Write (x8)	9	V _{PP_H}	V _{PP_X}	V _{IH}	V _{IH}	V _{IL}	V _{IH}	V _{IL}	Tri-state	Data In-Odd
	Write (x8)	10	V _{PP_H}	V _{PP_X}	X	V _{IL}	V _{IH}	V _{IH}	V _{IL}	Data In	Tri-state
	Write (x16)	11	V _{PP_H}	V _{PP_H}	X	V _{IL}	V _{IL}	V _{IH}	V _{IL}	Data In	Data In
	Standby	4	V _{PP_H}	V _{PP_H}	X	V _{IH}	V _{IH}	X	X	Tri-state	Tri-state
	Output Disable		V _{PP_H}	V _{PP_H}	X	X	X	V _{IH}	V _{IL}	Tri-state	Tri-state

NOTES:

1. Refer to DC Characteristics. When V_{PP1/2} = V_{PP_L} memory contents can be read but not written or erased.
2. Manufacturer and device codes may be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. Read operations with V_{PP1/2} = V_{PP_H} may access array data or the Intelligent Identifier codes.
4. With V_{PP1/2} at high voltage, the standby current equals I_{CC} + I_{PP} (standby).
5. Refer to Table 3 for valid Data-In during a write operation.
6. X can be V_{IL} or V_{IH}.
7. V_{PP_X} = V_{PP_H} or V_{PP_L}.
8. This x8 operation reads or writes the low byte of the x16 word on DQ₀₋₇, i.e., A₀ low reads "even" byte in x8 mode.
9. This x8 operation reads or writes the high byte of the x16 word on DQ₀₋₇ (transposed from DQ₈₋₁₅), i.e., A₀ high reads "odd" byte in x8 mode.
10. This x8 operation reads or writes the high byte of the x16 on DQ₈₋₁₅. A₀ is "don't care."
11. A₀ is "don't care," unused in x16 mode. High and low bytes are presented simultaneously.

Table 3. Command Definitions Byte-Wide Mode

Command	Notes	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
			Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	2	1	Write	RA	00H			
Read Intelligent ID Codes	4	3	Write	IA	90HT	Read		
Set-up Erase/Erase	5	2	Write	ZA	20H	Write	ZA	20H
Erase Verify	5	2	Write	EA	A0H	Read	EA	EVD
Set-up Write/Write	6	2	Write	WA	40H	Write	WA	WD
Write Verify	6	2	Write	WA	C0H	Read	WA	WVD
Reset	2, 7, 8	2	Write	ZA	FFH	Write	ZA	FFH

Table 4. Command Definitions Word-Wide Mode

Command	Notes	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
			Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	2	1	Write	RA	0000H			
Read Intelligent ID Codes	4	3	Write	IA	9090H	Read		
Set-up Erase/Erase	5	2	Write	ZA	2020H	Write	ZA	2020H
Erase Verify	5	2	Write	EA	A0A0H	Read	EA	EVD
Set-up Write/Write	6	2	Write	WA	4040H	Write	WA	WD
Write Verify	6	2	Write	WA	C0C0H	Read	WA	WVD
Reset	2, 7, 8	2	Write	ZA	FFFFH	Write	ZA	FFFFH

NOTES:

- Bus operations are defined in Table 2.
- IA = Identifier address: 00H for manufacturer code, 01H for device code.
EA = Address of memory location to be read during erase verify.
RA = Read Address
WA = Address of memory location to be written.
ZA = Address of 256 Kbyte zones involved in erase or Reset operations.
Addresses are latched on the falling edge of the Write Enable pulse.
- ID = Data read from location IA during device identification. (Mfr = 89H, Device = BDH).
EVD = Data read from location EA during erase verify.
WD = Data to be written at location WA. Data is latched on the rising edge of Write Enable.
WVD = Data read from location WA during write verify. WA is latched on the Write command.
- Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
- Figure 5 illustrates the Erase Algorithm.
- Figure 6 illustrates the Write Algorithm.
- The second bus cycle must be followed by the desired command register write.
- The Reset command operates on a zone basis. To reset the entire card requires reset write cycles to each zone.



Read Command

While $V_{PP1/2}$ is high, for erasure and writing, zone memory contents can be accessed via the read command. The read operation is initiated by writing 00H (0000H for the word-wide configuration) into the zone Command Register(s). Microprocessor read cycles retrieve zone data. The accessed zone remains enabled for reads until the Command Register(s) contents are altered.

The default contents of each zone's register(s) upon $V_{PP1/2}$ power-up is 00H (0000H for word-wide). This default value ensures that no spurious alteration of memory card contents occurs during the $V_{PP1/2}$ power transition. Where the $V_{PP1/2}$ supply is left at V_{PPH} , the memory card powers-up and remains enabled for reads until the command Register contents of targeted zones are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Intelligent Identifier Command

Each zone of the iMC002FLKA contains an Intelligent Identifier to identify memory card device characteristics. The operation is initiated by writing 90H (9090H for word-wide) into the Command Register(s) with zone address. Following the command write, a read cycle from address 00000H retrieves the manufacturer code 89H (8989H for word-wide). A read cycle from address 0002H returns the device code BDH (BDBDH for word-wide). To terminate the operation, it is necessary to write another valid command into the register(s).

Set-up Erase/Erase Commands

Set-up Erase stages the targeted zone(s) for electrical erasure of all bytes in the zone. The set-up erase operation is performed by writing 20H to the Command Register (2020H for word-wide) with zone address.

To commence zone-erasure, the erase command (20H or 2020H) must again be written to the register(s) with zone address. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command with zone address).

This two-step sequence of set-up followed by execution ensures that zone memory contents are not accidentally erased. Also, zone-erasure can only occur when high voltage is applied to the $V_{PP1/2}$ pins. In the absence of this high voltage, zone memory con-

tents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all of the bytes of the zone in parallel. After each erase operation, all bytes in the zone must be individually verified. In byte-mode operations, zones are segregated by A_0 in odd and even banks; erase and erase verify operations must be done in complete passes of even-bytes-only then odd-bytes-only. See the Erase Algorithm for byte-wide mode. The erase verify operation is initiated by writing A0H (AOA0H for word-wide) into the Command Register(s). The address for the byte(s) to be verified must be supplied as it is latched on the falling edge of the Write Enable pulse. The register write terminates the erase operation with the rising edge of its Write Enable pulse.

The enabled zone applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased. Similarly, reading FFFFH from the addressed word indicates that all bits in the word are erased.

The erase-verify command must be written to the Command Register prior to each byte (word) verification to latch its address. The process continues for each byte (word) in the zone(s) until a byte (word) does not return FFH (FFFFH) data, or the last address is accessed.

In the case where the data read is not FFH (FFFFH), another erase operation is performed. (Refer to Set-up Erase/Erase.) Verification then resumes from the address of the last-verified byte (word). Once all bytes (words) in the zone(s) have been verified, the erase step is complete. The accessed zone can now be written. At this point, the verify operation is terminated by writing a valid command (e.g., Write Set-up) to the Command Register. The Erase algorithms for byte-wide and word-wide configurations illustrate how commands and bus operations are combined to perform electrical erasure of the iMCC002FLKA. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Write/Write Commands

Set-up write is a command-only operation that stages the targeted zone for byte writing. Writing 40H (4040H) into the Command Register(s) performs the set-up operation.

Once the write set-up operation is performed, the next Write Enable pulse causes a transition to an active write operation. Addresses are internally latched on the falling edge of the Write Enable pulse. Data is internally latched on the rising edge of the Write Enable pulse. The rising edge of Write Enable also begins the write operation. The write operation terminates with the next rising edge of Write Enable, which is used to write the verify command. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Write Verify Command

The iMC002FLKA is written on a byte-by-byte or word-by-word basis. Byte or word writing may occur sequentially or at random. Following each write operation, the byte or word just written must be verified.

The write-verify operation is initiated by writing C0H (C0C0H) into the Command Register(s) with correct address. The register write(s) terminate(s) the write operation with the rising edge of its Write Enable pulse. The write-verify operation stages the accessed zone(s) for verification of the byte or word last written. The zone(s) apply(ies) an internally-generated margin voltage to the byte or word. A micro-processor read cycle outputs the data. A successful comparison between the written byte or word and true data means that the byte or word is successfully written. The write operation then proceeds to the next desired byte or word location. The Write algorithms for byte-wide and word-wide configurations illustrate how commands are combined with bus operations to perform byte and word writes. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or write-command sequences. Following either set-up command (erase or write) with

two consecutive writes of FFH (FFFFH for word-wide) will safely abort the operation. Zone memory contents will not be altered. A valid command must then be written to place the accessed zone in the desired state.

EXTENDED ERASE/WRITE CYCLING

Intel has designed extended cycling capability into its ETOX II flash memory technology enabling a flash memory card with a MTBF that is many times more reliable than rotating disk technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field minimizes the probability of oxide defects in the region. The lower electric field greatly reduces oxide stress and the probability of failure.

WRITE ALGORITHMS

The write algorithm(s) use write operations of 10 μ s duration. Each operation is followed by a byte or word verification to determine when the addressed byte or word has been successfully written. The algorithm(s) allows for up to 25 write operations per byte or word, although most bytes and words verify on the first or second operation. The entire sequence of writing and byte/word verification is performed with V_{PP} at high voltage.

ERASE ALGORITHM

The Erase algorithm(s) yield(s) fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the write algorithm, to simultaneously remove charge from all bits in the accessed zone(s).

Erasures begins with a read of memory zone contents. Reading FFH (FFFFH) data from the accessed zone(s) can be immediately followed by writing to the desired zone(s).



For zones being erased and rewritten, uniform and reliable erasure is ensured by first writing all bits in the accessed zone to their charged state (data = 00H byte-wide, 00000H word-wide). This is accomplished, using the write algorithm, in approximately four seconds per zone.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH byte-wide, FFFFH word-wide) begins at address 00000H and continues through the zone to the last address, or until data other than FFH (FFFFH) is encountered.

(Note: byte-wide erase operation requires separate even- and odd-address passes to handle the individual 256 Kbyte zones.) With each erase operation, an increasing number of bytes or words verify to the erased state. Erase efficiency may be improved by storing the address of the last byte or word verified in a register(s). Following the next erase operation, verification starts at the stored address location. Follow this procedure until all bytes in the zone are erased. Then, re-start the procedure for the next zone or word-wide zone pair. Erasure typically occurs in two seconds per zone.

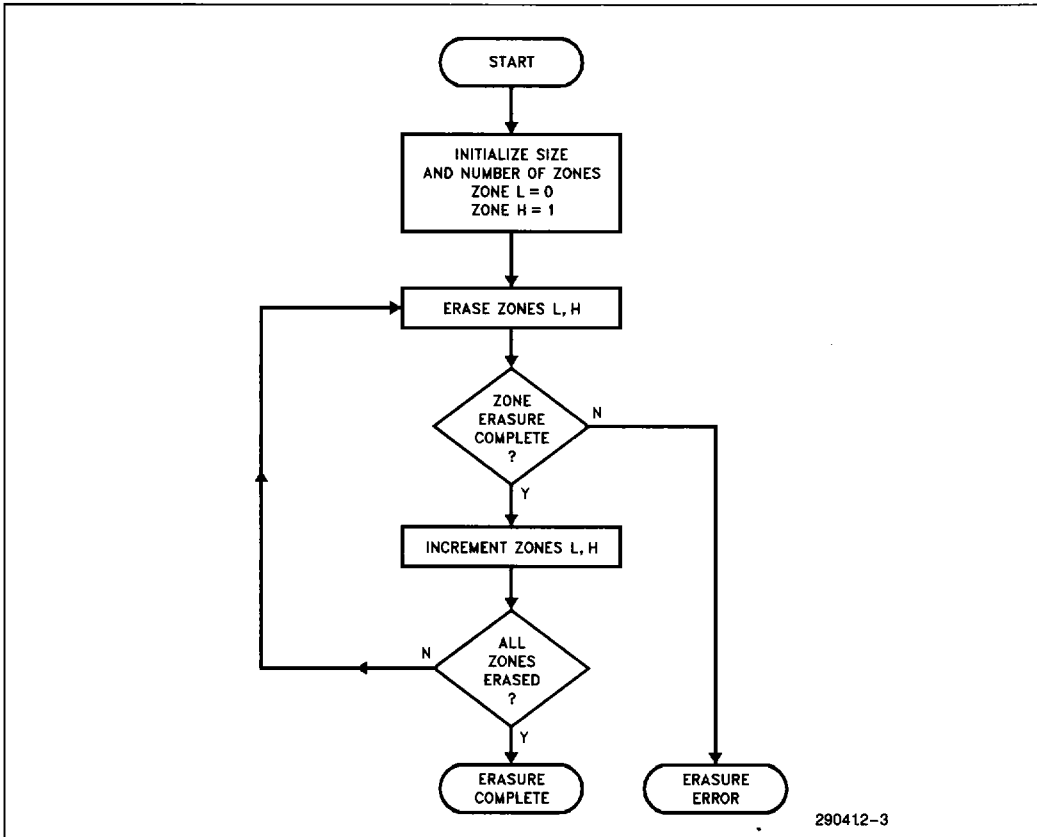
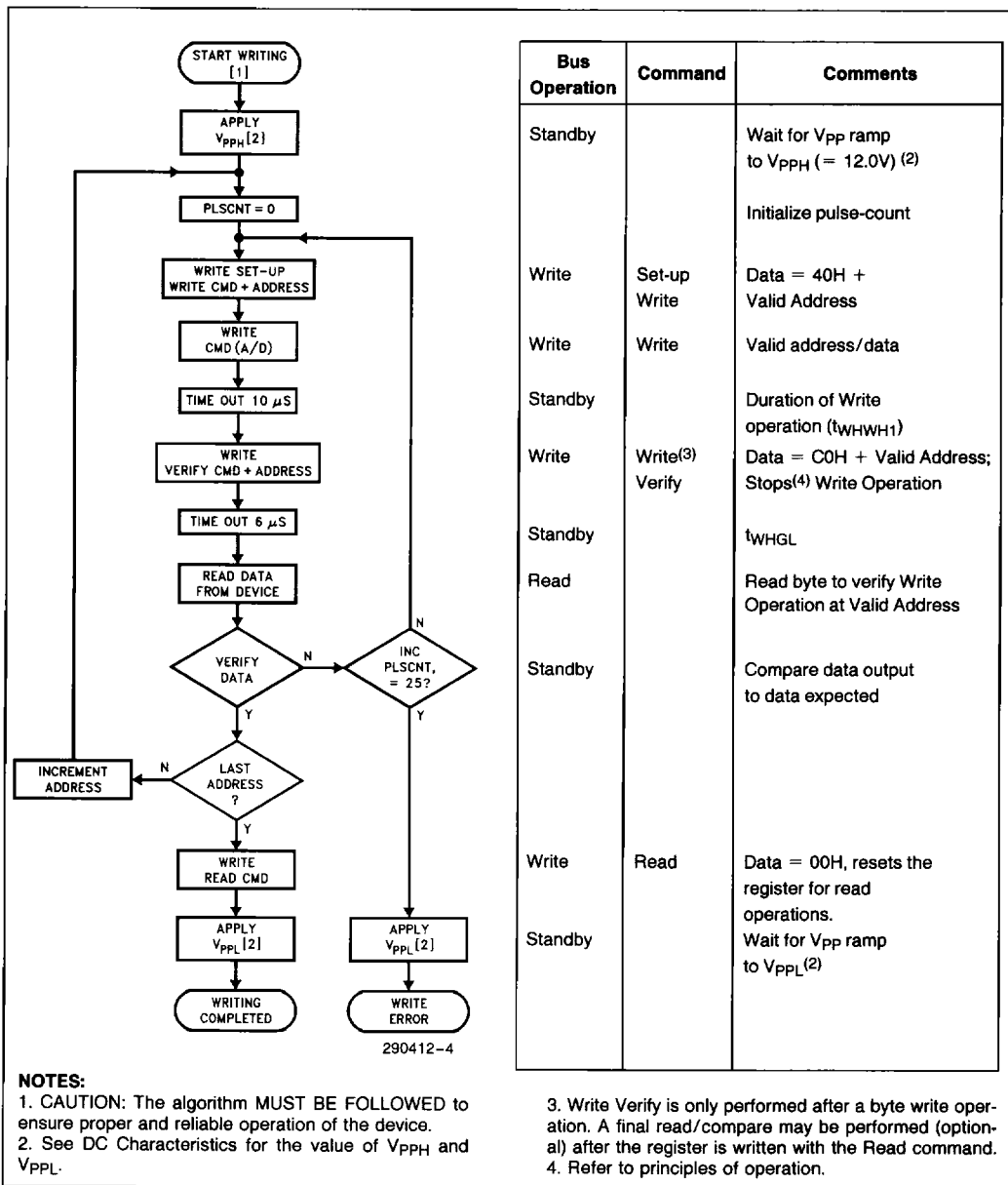


Figure 3. Full Card Erase Flow



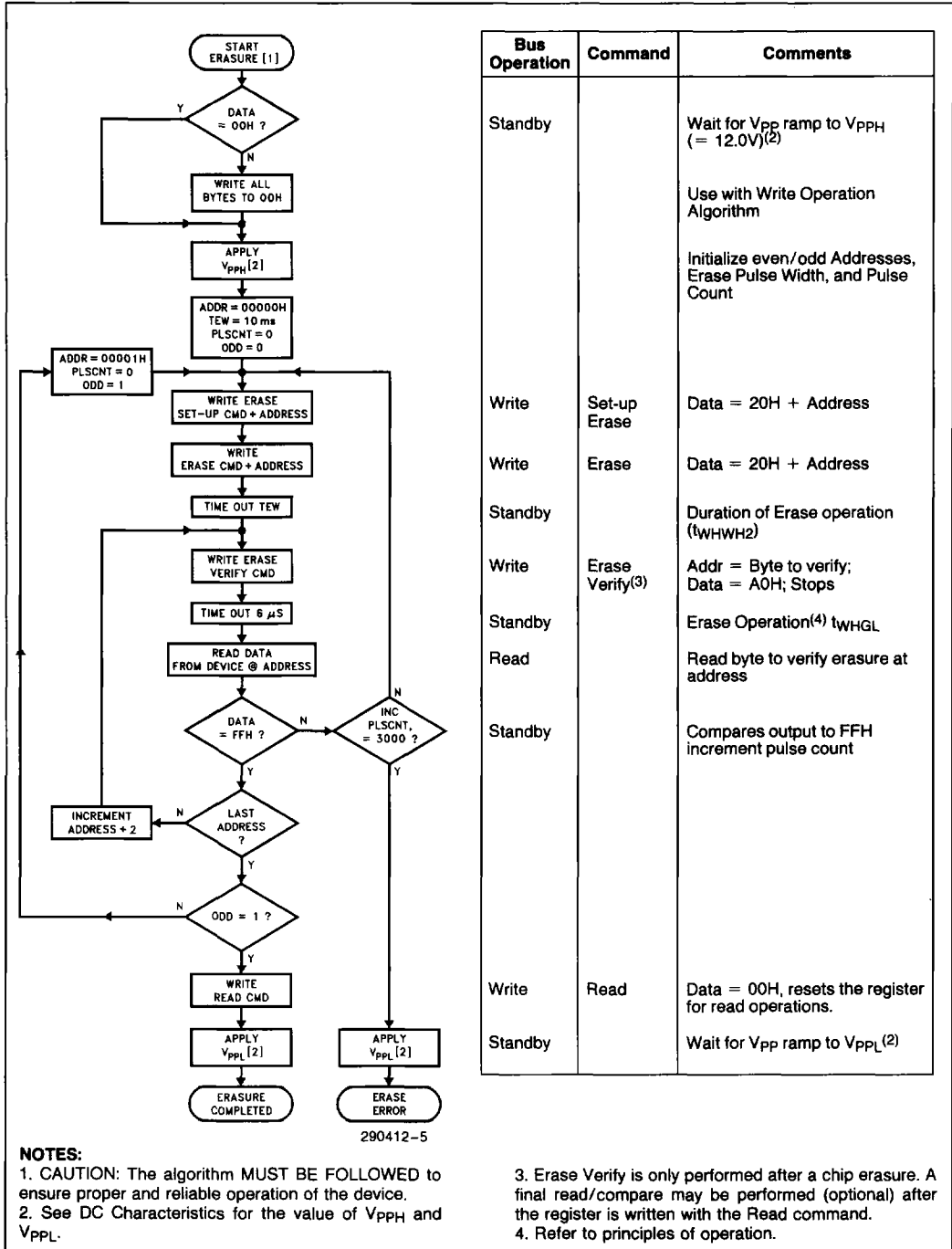
Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) (2) Initialize pulse-count
Write	Set-up Write	Data = 40H + Valid Address
Write	Write	Valid address/data
Standby		Duration of Write operation (t_{WHWH1})
Write	Write(3) Verify	Data = C0H + Valid Address; Stops(4) Write Operation
Standby		t_{WHGL}
Read		Read byte to verify Write Operation at Valid Address
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (2)

NOTES:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V_{PPH} and V_{PPL} .

3. Write Verify is only performed after a byte write operation. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

Figure 4. Write Algorithm for Byte-Wide Mode



Bus Operation	Command	Comments
Standby		Wait for V _{pp} ramp to V _{ppH} (= 12.0V) ⁽²⁾
		Use with Write Operation Algorithm
		Initialize even/odd Addresses, Erase Pulse Width, and Pulse Count
Write	Set-up Erase	Data = 20H + Address
Write	Erase	Data = 20H + Address
Standby		Duration of Erase operation (t _{WHWH2})
Write	Erase Verify ⁽³⁾	Addr = Byte to verify; Data = A0H; Stops
Standby		Erase Operation ⁽⁴⁾ t _{WHGL}
Read		Read byte to verify erasure at address
Standby		Compares output to FFH increment pulse count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V _{pp} ramp to V _{ppL} ⁽²⁾

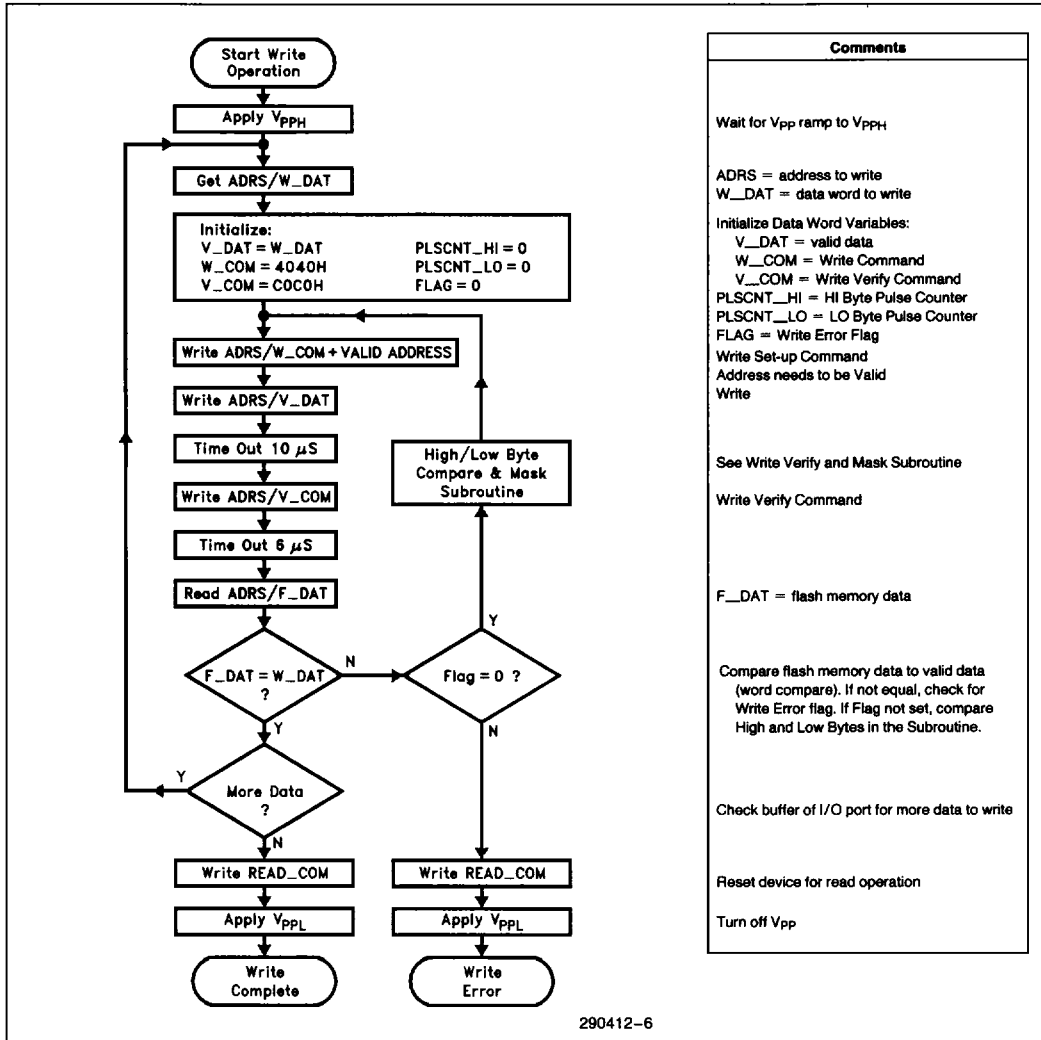
6

NOTES:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of V_{ppH} and V_{ppL}.

3. Erase Verify is only performed after a chip erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

Figure 5. Erase Algorithm for Byte-Wide Mode



Comments

Wait for Vpp ramp to VppH

ADRS = address to write
W_DAT = data word to write

Initialize Data Word Variables:
V_DAT = valid data
W_COM = Write Command
V_COM = Write Verify Command
PLSCNT_HI = HI Byte Pulse Counter
PLSCNT_LO = LO Byte Pulse Counter
FLAG = Write Error Flag

Write Set-up Command
Address needs to be Valid
Write

See Write Verify and Mask Subroutine

Write Verify Command

F_DAT = flash memory data

Compare flash memory data to valid data (word compare). If not equal, check for Write Error flag. If Flag not set, compare High and Low Bytes in the Subroutine.

Check buffer of I/O port for more data to write

Reset device for read operation

Turn off Vpp

290412-6

Figure 6. Write Algorithm for Word-Wide Mode

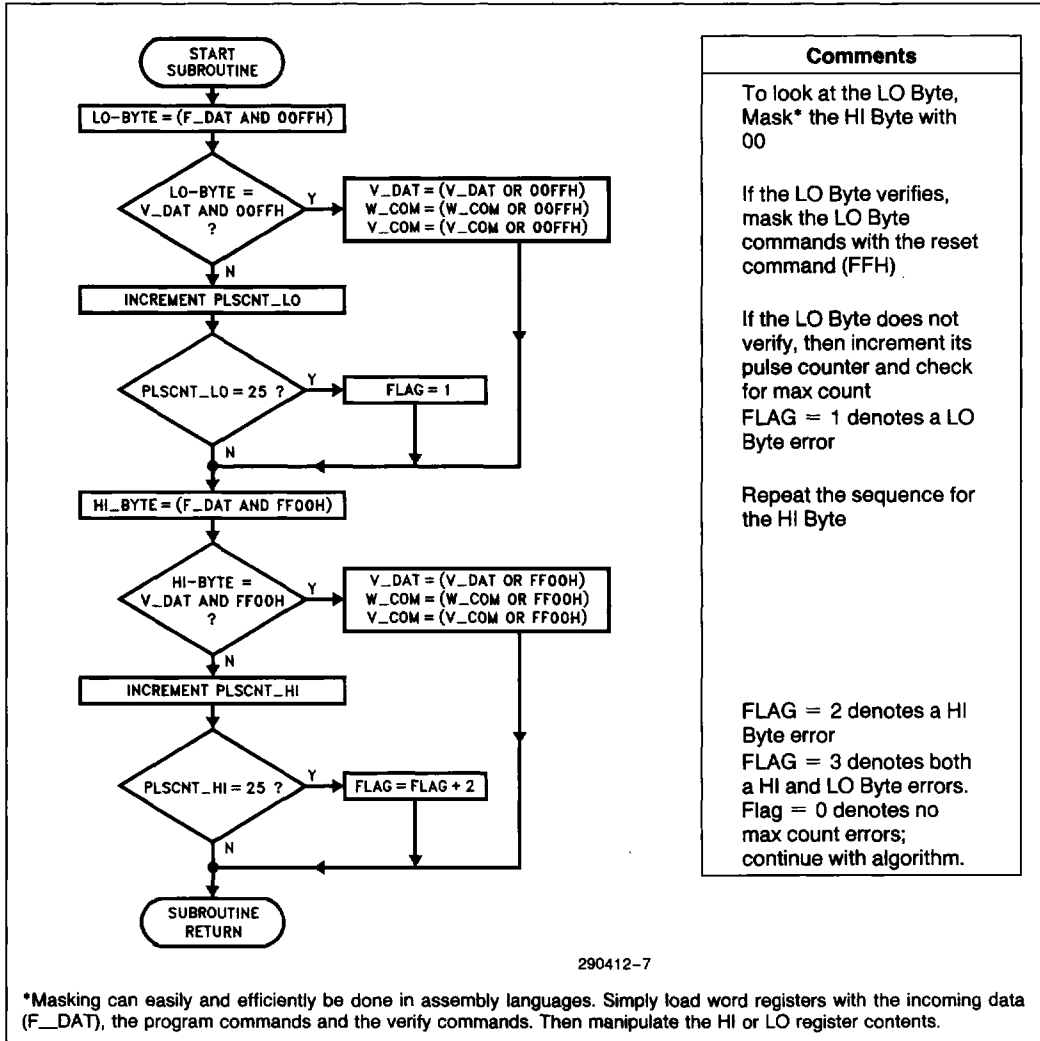


Figure 7. Write Verify and Mask Subroutine for Word-Wide Mode

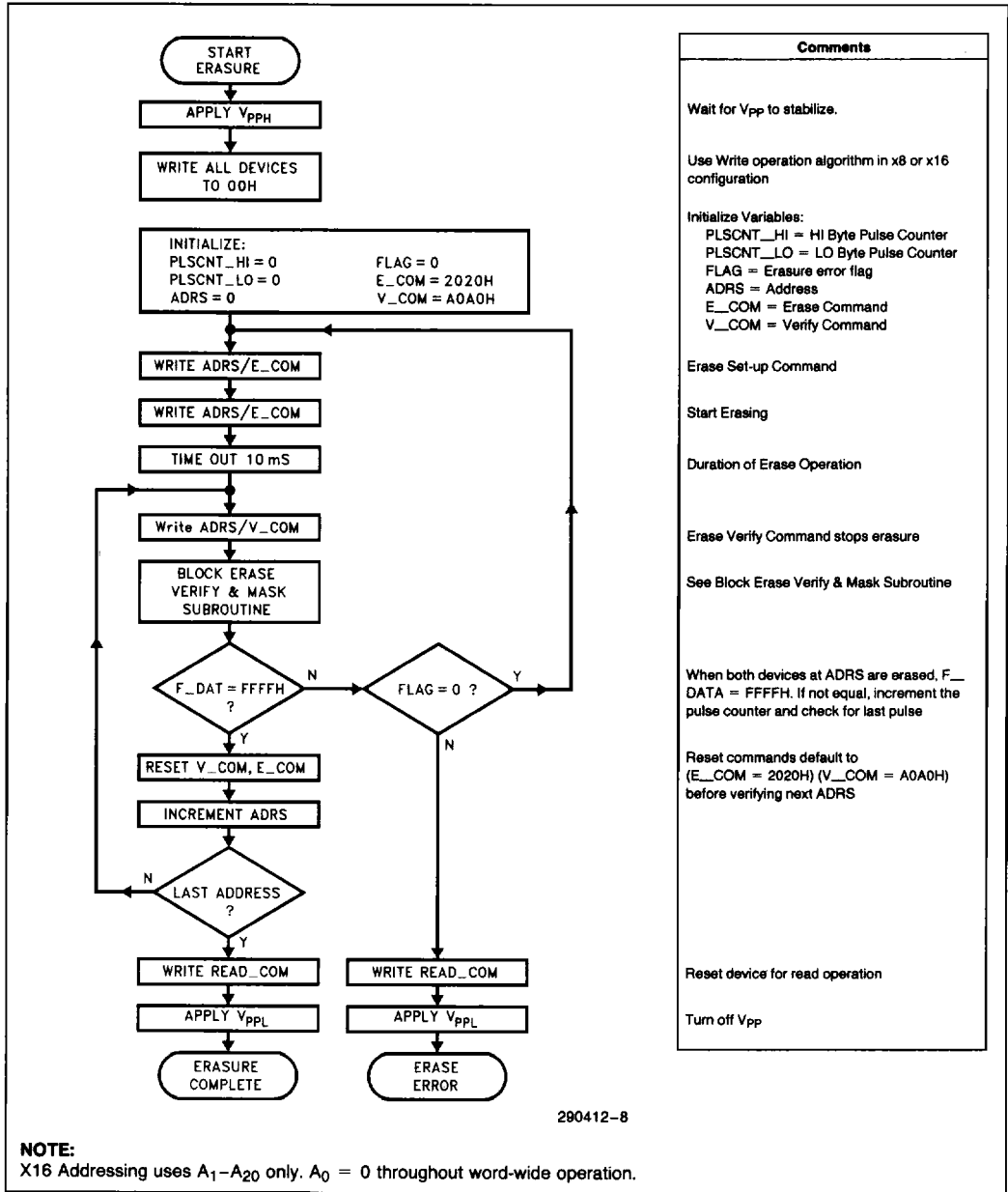
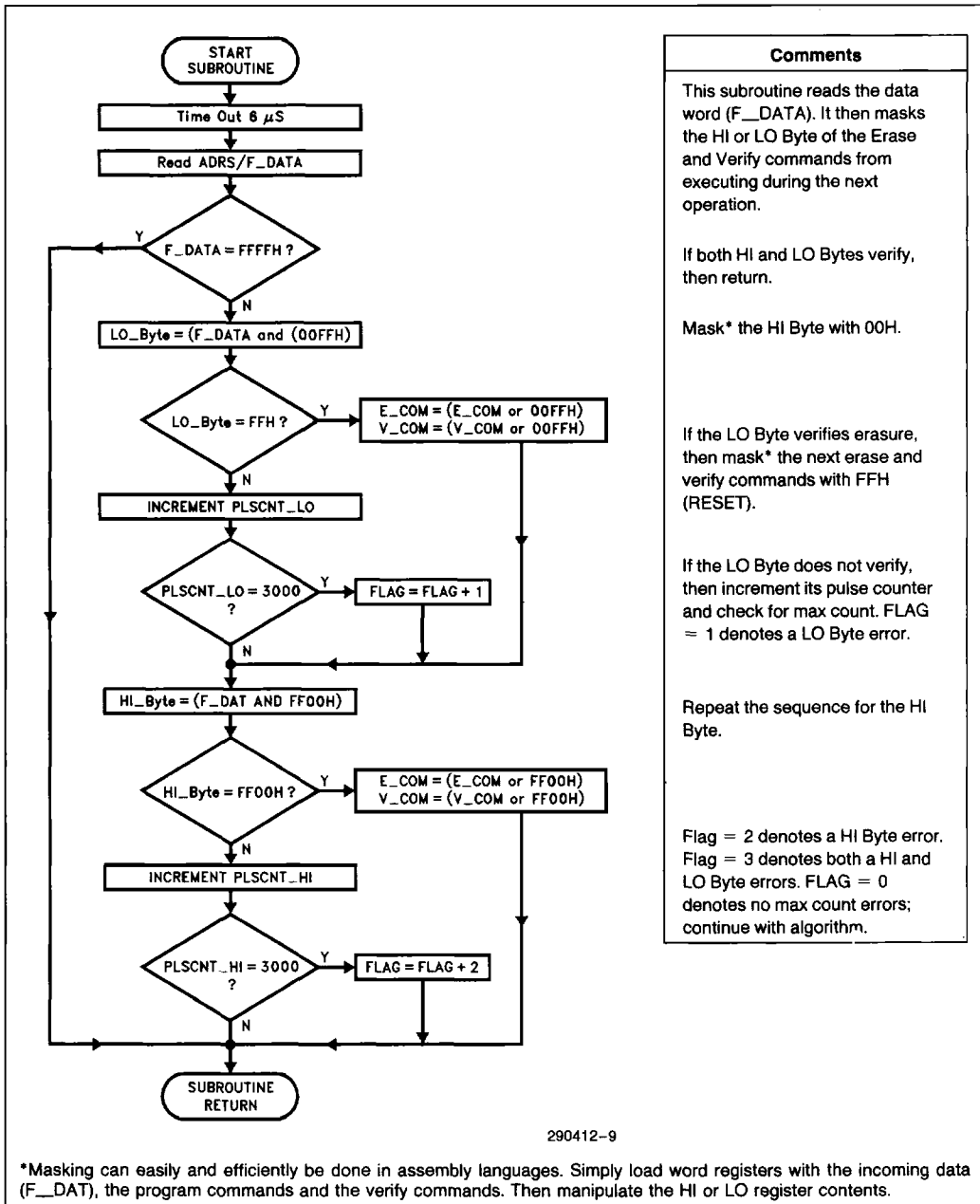


Figure 8. Erase Algorithm for Word-Wide Mode



Comments
This subroutine reads the data word (F_DATA). It then masks the HI or LO Byte of the Erase and Verify commands from executing during the next operation.
If both HI and LO Bytes verify, then return.
Mask* the HI Byte with 00H.
If the LO Byte verifies erasure, then mask* the next erase and verify commands with FFH (RESET).
If the LO Byte does not verify, then increment its pulse counter and check for max count. FLAG = 1 denotes a LO Byte error.
Repeat the sequence for the HI Byte.
Flag = 2 denotes a HI Byte error. Flag = 3 denotes both a HI and LO Byte errors. FLAG = 0 denotes no max count errors; continue with algorithm.

290412-9

*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F_DAT), the program commands and the verify commands. Then manipulate the HI or LO register contents.

Figure 9. Erase Verify and Mask Subroutine for Word-Wide Mode

SYSTEM DESIGN CONSIDERATIONS

Three-Line Control

Three-line control provides for:

- a. the lowest possible power dissipation and.
- b. complete assurance that output bus contention will not occur.

To efficiently use these three control inputs, an address-decoder output should drive $CE_{1,2\#}$, while the system's Read signal controls the card $OE\#$ signal, and other parallel zones. This, coupled with the internal zone decoder, assures that only enabled memory zones have active outputs, while deselected zones maintain the low power standby condition.

Power-Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues—standby, active and transient current peaks, produced by falling and rising edges of $CE_{1,2\#}$. The capacitive and inductive loads on the card and internal flash memory zones determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection will suppress transient voltage peaks. The iMC002FLKA features on-card ceramic decoupling capacitors connected between V_{CC} and V_{SS} , and between V_{PP1}/V_{PP2} and V_{SS} .

The card connector should also have a 4.7 μ F electrolytic capacitor between V_{CC} and V_{SS} , as well as between V_{PP1}/V_{PP2} and V_{SS} . The bulk capacitors will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

Power Up/Down Protection

The PCMCIA/JEIDA socket is specified, via unique Pin lengths, to properly sequence the power supplies to the flash memory card. This assures that hot insertion and removal will not result in card damage or data loss.

Each zone in the iMC002FLKA is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $WE\#$ and $CE_{1,2\#}$ must be low for a command write, driving either to V_{IH} will inhibit writes. With its control register architecture, alteration of zone contents only occurs after successful completion of the two-step command sequences.

While these precautions are sufficient for most applications, it is recommended that V_{CC} reach its steady state value before raising $V_{PP1,2}$ above $V_{CC} + 2.0V$. In addition, upon powering-down, $V_{PP1,2}$ should be below $V_{CC} + 2.0V$, before lowering V_{CC} .

Absolute Maximum Ratings*

Operating Temperature	
During Read0°C to + 60°C(1)
During Erase/Write0°C to + 60°C
Temperature Under Bias -10°C to +70°C
Storage Temperature -30°C to +70°C
Voltage on Any Pin with	
Respect to Ground -2.0V to +7.0V(2)
V _{PP1} /V _{PP2} Supply Voltage with	
Respect to Ground	
During Erase/Write -2.0V to +14.0V(2,3)
V _{CC} Supply Voltage with	
Respect to Ground -2.0V to +7.0V(2)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC input voltage on V_{PP1}/V_{PP2} may overshoot to +14.0V for periods less than 20 ns.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T _A	Operating Temperature	0	60	°C	For Read-Only and Read/Write Operations
V _{CC}	V _{CC} Supply Voltage	4.75	5.25	V	
V _{PPH}	Active V _{PP1} , V _{PP2} Supply Voltages	11.40	12.60	V	
V _{PPL}	V _{PP} During Read Only Operations	0.00	6.50	V	

6
DC CHARACTERISTICS—Byte Wide Mode

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I _{LI}	Input Leakage Current	1, 4		±1.0	±20	μA	V _{CC} = V _{CC} max V _{IN} = V _{CC} or V _{SS}
I _{LO}	Output Leakage Current	1		±1.0	±20	μA	V _{CC} = V _{CC} max V _{OUT} = V _{CC} or V _{SS}
I _{CCS}	V _{CC} Standby Current	1		0.4	0.8	mA	V _{CC} = V _{CC} max CE ₁ # = CE ₂ # = V _{CC} ±0.2V
				4	7		V _{CC} = V _{CC} max CE ₁ # = CE ₂ # = V _{IH}
I _{CC1}	V _{CC} Active Read Current	1, 2		25	50	mA	V _{CC} = V _{CC} max CE# = V _{IL} f = 6 MHz, I _{OUT} = 0 mA
I _{CC2}	V _{CC} Write Current	1, 2		5.0	15.0		Writing in Progress
I _{CC3}	V _{CC} Erase Current	1, 2		10.0	20.0	mA	Erasure in Progress
I _{CC4}	V _{CC} Write Verify Current	1, 2		10.0	20.0		V _{PP} = V _{PPH} Write Verify in Progress

DC CHARACTERISTICS—Byte Wide Mode (Continued)

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I _{CC5}	V _{CC} Erase Verify Current	1, 2		10.0	20.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
I _{PPS}	V _{PP} Leakage Current	1			± 80	μA	V _{PP} ≤ V _{CC}
I _{PP1}	V _{PP} Read Current or Standby Current	1, 3		0.4	0.8	mA	V _{PP} > V _{CC}
					± 0.08		V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Write Current	1, 3		8.0	30	mA	V _{PP} = V _{PPH} Write in Progress
I _{PP3}	V _{PP} Erase Current	1, 3		10	30	mA	V _{PP} = V _{PPH} Erasure in Progress
I _{PP4}	V _{PP} Write Verify Current	1, 3		2.0	5.0	mA	V _{PP} = V _{PPH} Write Verify in Progress
I _{PP5}	V _{PP} Erase Verify Current	1, 3		2.0	5.0	mA	V _{PP} = V _{PPH} Erase Verify in Progress
V _{IL}	Input Low Voltage		−0.5		0.8	V	
V _{IH}	Input High Voltage		2.4		V _{CC} ± 0.3	V	
V _{OL}	Output Low Voltage				0.40	V	I _{OL} = 3.2 mA V _{CC} = V _{CC} min
V _{OH1}	Output High Voltage		3.8			V	I _{OH} = −2.0 mA V _{CC} = V _{CC} min
V _{PP1}	V _{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Write are inhibited when V _{PP} = V _{PP1}
V _{PPH}	V _{PP} During Read/Write Operations		11.40		12.60	V	
V _{LKO}	V _{CC} Erase/Write Lock Voltage		2.5			V	

NOTES:

- All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C.
- 1 chip active and 7 in standby for byte-wide mode.
- Assumes 1 V_{pp} is active.
- Due to 100 kΩ pull up resistors OE#, CE₁#, CE₂# and WE# will exhibit ≤ 55 μA of additional I_{LI} when V_{IN} = V_{SS}.

DC CHARACTERISTICS—Word Wide Mode

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I _{LI}	Input Leakage Current	1, 4		± 1.0	± 20	μA	V _{CC} = V _{CC} max V _{IN} = V _{CC} or V _{SS}
I _{LO}	Output Leakage Current	1		± 1.0	± 20	μA	V _{CC} = V _{CC} max V _{OUT} = V _{CC} or V _{SS}
I _{CCS}	V _{CC} Standby Current	1		0.4	0.8	mA	V _{CC} = V _{CC} max CE ₁ # = CE ₂ # = V _{CC} ± 0.2V
				4	7	mA	V _{CC} = V _{CC} max CE ₁ # = CE ₂ # = V _{IH}

DC CHARACTERISTICS—Word Wide Mode (Continued)

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical	Max		
I _{CC1}	V _{CC} Active Read Current	1, 2		40	80	mA	V _{CC} = V _{CC} max CE# = V _{IL} f = 6 MHz, I _{OUT} = 0 mA
I _{CC2}	V _{CC} Write Current	1, 2		7.0	25	mA	Writing in Progress
I _{CC3}	V _{CC} Erase Current	1, 2		15	30	mA	Erasure in Progress
I _{CC4}	V _{CC} Write Verify Current	1, 2		15	30	mA	V _{PP} = V _{PPH} Write Verify in Progress
I _{CC5}	V _{CC} Erase Verify Current	1, 2		10	30	mA	V _{PP} = V _{PPH} Erase Verify in Progress
I _{PPS}	V _{PP} Leakage Current	1			± 80	μA	V _{PP} ≤ V _{CC}
I _{PP1}	V _{PP} Read Current or Standby Current	1, 3		0.7	1.6	mA	V _{PP} > V _{CC}
					± 0.16		V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Write Current	1, 3		16	60	mA	V _{PP} = V _{PPH} Write in Progress
I _{PP3}	V _{PP} Erase Current	1, 3		20	60	mA	V _{PP} = V _{PPH} Erasure in Progress
I _{PP4}	V _{PP} Write Verify Current	1, 3		5.0	12	mA	V _{PP} = V _{PPH} Write Verify in Progress
I _{PP5}	V _{PP} Erase Verify Current	1, 3		5.0	12	mA	V _{PP} = V _{PPH} Erase Verify in Progress
V _{IL}	Input Low Voltage		-0.5		0.8	V	
V _{IH}	Input High Voltage		2.4		V _{CC} ± 0.3	V	
V _{OL}	Output Low Voltage				0.40	V	I _{OL} = 3.2 mA V _{CC} = V _{CC} min
V _{OH1}	Output High Voltage		3.8			V	I _{OH} = -2.0 mA V _{CC} = V _{CC} min
V _{PPL}	V _{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Write are Inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} During Read/Write Operations		11.40		12.60	V	
V _{LKO}	V _{CC} Erase/Write Lock Voltage		2.5			V	

NOTES:

- All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C.
- 2 chips active and 6 in standby for word-wide mode.
- Assumes 2 V_{PPS} are active.
- Due to 100 kΩ pull up resistors OE#, CE₁#, CE₂# and WE# will exhibit ≤ 55 μA of additional I_L when V_{IN} = V_{SS}.

CAPACITANCE $T = 25^{\circ}\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN1}	Address Capacitance			40	pF	$V_{IN} = 0V$
C_{IN2}	Control Capacitance			40	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			40	pF	$V_{OUT} = 0V$
$C_{I/O}$	I/O Capacitance			40	pF	$V_{I/O} = 0V$

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) 10 ns

Input Pulse Levels V_{OL} and V_{OH1} Input Timing Reference Level V_{IL} and V_{IH} Output Timing Reference Level V_{IL} and V_{IH} **AC CHARACTERISTICS—Read-Only Operations**

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}/t_{RC}	Read Cycle Time	2	200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time	2		200	ns
t_{AVQV}/t_{ACC}	Address Access Time	2		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time	2		100	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	2	5		ns
t_{EHQZ}	Chip Disable to Output in High Z	2		60	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	2	5		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	2		60	ns
t_{OH}	Output Hold from Address, CE#, or OE# Change	1, 2	5		ns
t_{WHGL}	Write Recovery Time before Read	2	6		μs

NOTES:

1. Whichever occurs first.
2. Rise/Fall Time $\leq 10\text{ ns}$.

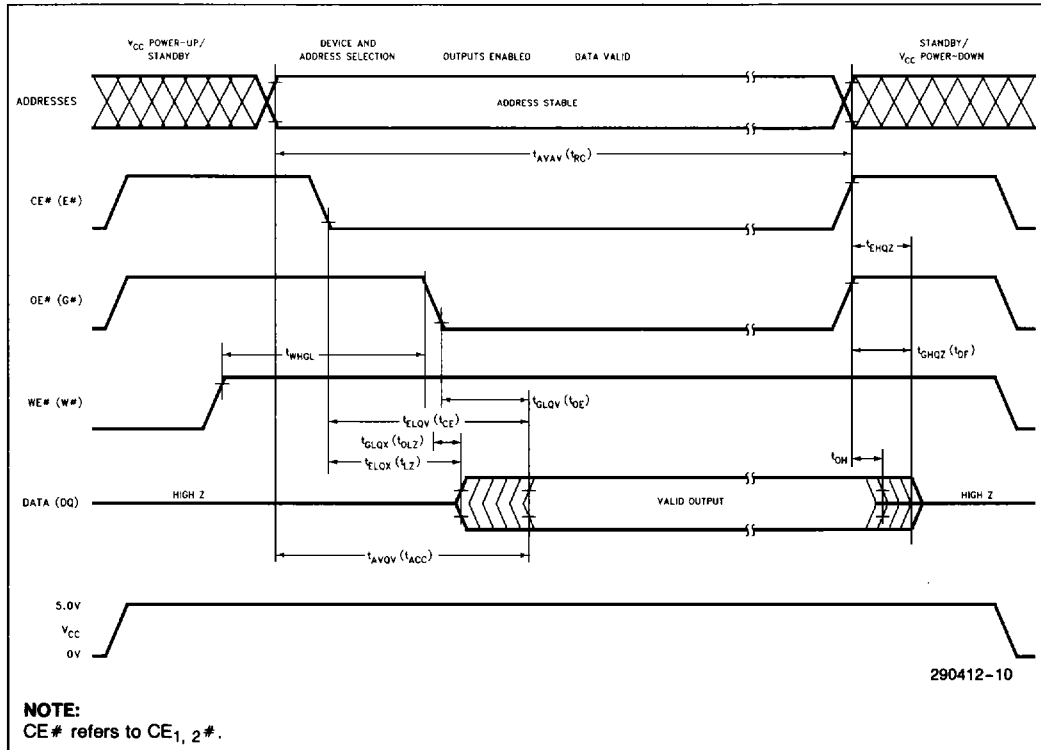


Figure 10. AC Waveforms for Read Operations

AC CHARACTERISTICS—For Write/Erase Operations

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}/t_{WC}	Write Cycle Time	1, 2	200		ns
t_{AVWL}/t_{AS}	Address Set-up Time	1, 2	0		ns
t_{WLAX}/t_{AH}	Address Hold Time	1, 2	100		ns
t_{DVWH}/t_{DS}	Data Set-up Time	1, 2	80		ns
t_{WHDX}/t_{DH}	Data Hold Time	1, 2	30		ns
t_{WHGL}	Write Recovery Time before Read	1, 2	6		μ s
t_{GHWL}	Read Recovery Time before Write	1, 2	0		μ s
t_{WLOZ}	Output High-Z from Write Enable	1, 2	5		ns
t_{WHOZ}	Output Low-Z from Write Enable	1, 2		60	ns
t_{ELWL}/t_{CS}	Chip Enable Set-up Time before Write	1, 2	40		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time	1, 2	0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	1, 2	100		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High	1, 2	20		ns
t_{WHWH1}	Duration of Write Operation	1, 2, 3	10		μ s
t_{WHWH2}	Duration of Erase Operation	1, 2, 3	9.5		ms
t_{VPEL}	V_{PP} Set-up Time to Chip Enable Low	1, 2	100		ns

NOTES:

1. Read timing parameters during read/write operations are the same as during read-only operations. Refer to A.C. Characteristics for Read-Only Operations.
2. Rise/Fall time \leq 10 ns.
3. The integrated stop timer terminates the write/erase operations, thereby eliminating the need for a maximum specification.

ERASE/WRITE PERFORMANCE

Parameter	Notes	Min	Typ	Max	Unit
Zone Erase Time	1, 3, 4		2.0	30	sec
Zone Write Time	1, 2, 4		4.0	25	sec
MTBF	5		10^6		Hrs

NOTES:

1. 25°C, 12.0V V_{PP} .
2. Minimum byte writing time excluding system overhead is 16 μ s (10 μ s program + 6 μ s write recovery), while maximum is 400 μ s/byte (16 μ s x 25 loops allowed by algorithm). Max chip write time is specified lower than the worst case allowed by the write algorithm since most bytes write significantly faster than the worst case byte.
3. Excludes 00H writing Prior to Erasure.
4. One zone equals 256 Kbytes.
5. MTBF – Mean Time between Failure, 50% failure point for disk drives.

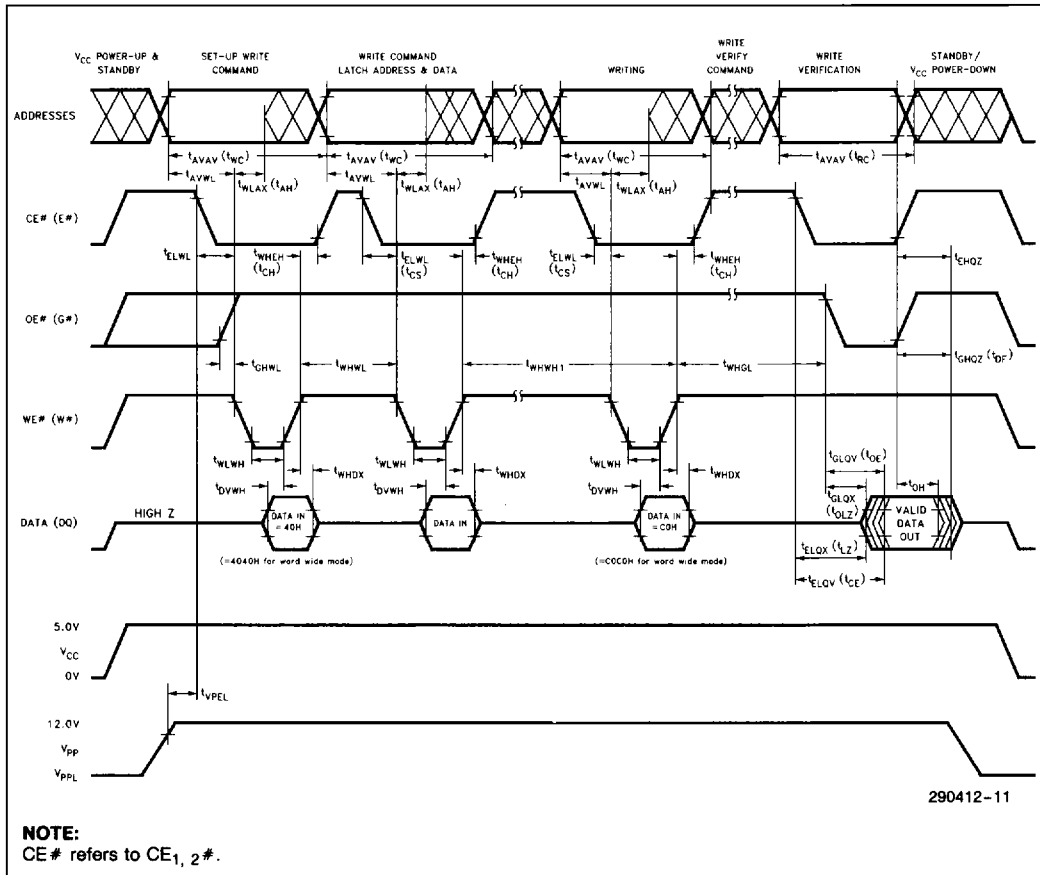


Figure 11. AC Waveforms for Write Operations

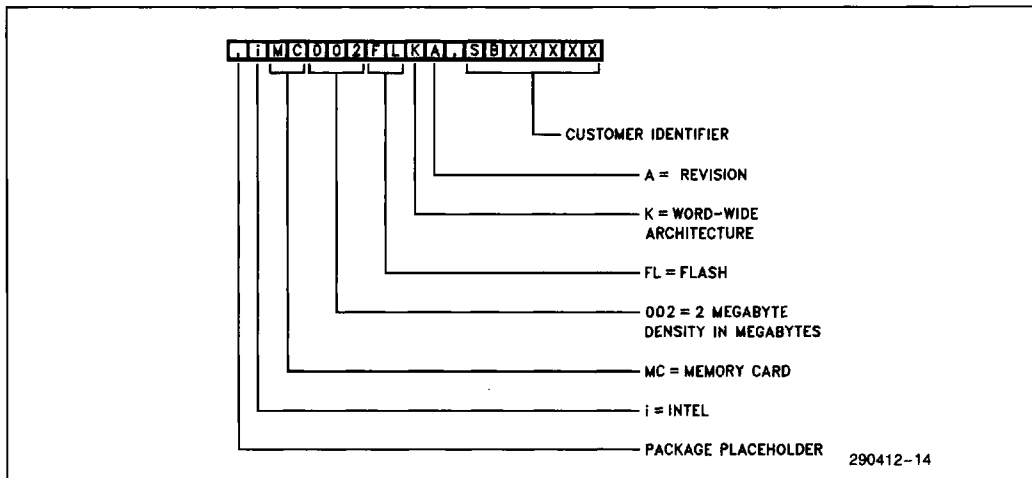
ALTERNATIVE CE #-CONTROLLED WRITES

Symbol	Characteristic	Notes	Min	Max	Unit
t _{AVAV}	Write Cycle Time		200		ns
t _{AVEL}	Address Set-up Time		0		ns
t _{ELAX}	Address Hold Time		100		ns
t _{DVEH}	Data Set-up Time		80		ns
t _{EHDX}	Data Hold Time		30		ns
t _{EHGL}	Write Recovery Time before Read		6		μs
t _{GHEL}	Read Recovery Time before Write		0		μs
t _{WLEL}	Write Enable Set-Up Time before Chip-Enable		0		ns
t _{EHWH}	Write Enable Hold Time		0		ns
t _{ELEH}	Write Pulse Width	1	100		ns
t _{EHEL}	Write Pulse Width High		20		ns
t _{PEL}	V _{PP} Set-up Time to Chip Enable Low		100		ns

NOTES:

1. Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse width (with a longer Write Enable timing waveform) all set-up, hold and inactive Write Enable times should be measured relative to the Chip Enable waveform.

ORDERING INFORMATION



ADDITIONAL INFORMATION

- ER-20, "ETOX™ II Flash Memory Technology"
- RR-60, "ETOX™ II Flash Memory Reliability Data Summary"
- AP-343, "Solutions for High Density Applications using Flash Memory"

ORDER NUMBER

- 294005
- 293002
- 292079

REVISION HISTORY

Number	Description
-002	<ul style="list-style-type: none"> — Removed Preliminary — Removed ExCA Compliance Section — Clarified need for Valid Address during commands — Corrected $V_{PP} = V_{PPH}$ in Erase Algorithm — Increased $I_{CC2} - I_{CC5}$ D.C. current specs for both Byte Wide and Word Wide modes — Revised and Updated Application Section discussion — Changed order number
-003	<ul style="list-style-type: none"> — Change Signal with Bar to # — Changed T/C Values

6