SMART®
Modular Technologies

SM5320130UUXUUU

November 19, 1996

4MByte (1M x 32) DRAM Module - 1Mx16 based
72-pin SIMM

Features

- Standard : JEDEC (5.0V FPM only)
- Configuration : Non-parity
- Access Time : 60/70/80ns
- Operation Mode : FPM/EDO
- Operating Voltage : 3.3/5.0V
- Refresh : 1K/4K
- Device Physicals : 400mil SOJ/TSOP
- Lead Finish : Gold/Solder
- Length x Height : 4.250" x 0.850"(SOJ)/1.000”(TSOP)
- No. of sides : Single-sided
- Mating Connector (Examples)
  - Horizontal : AMP-7-382486-2 (Tin) / 7-382487-2 (Gold)
  - Vertical : AMP-822019-4 (Tin) / 822031-4 (Gold)
  - Angled : AMP-822110-3 (Tin) / 822097-3 (Gold)

Part Numbers

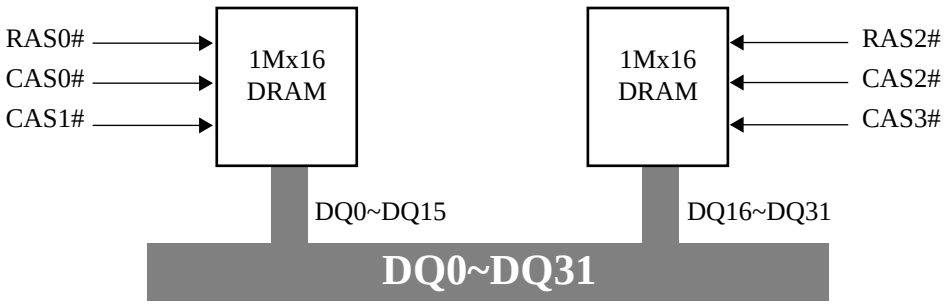
SM53201300UXUUU	:	FPM, 5.0V
SM53201301UXUUU	:	FPM, 3.3V
SM53201308UXUUU	:	EDO, 5.0V
SM53201309UXUUU	:	EDO, 3.3V

Note: Refer last page for all "U” options.

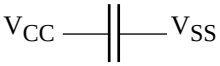
Related Products

SM5320140U1XUUU	:	1Mx32, 1Mx4 based.

Functional Diagram



Notes : 1. A0~A11 to all DRAMs (A10 & A11 are NC for 1K refresh module).
2. WE# to all DRAMs.
3. OE# of all DRAMs is grounded.



Decoupling capacitors to all devices.

(All specifications of this device are subject to change without notice.)

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Pin Name

A0~A9	Row and Column Addresses for 1K Refresh Module
A0~A11	Row Addresses for 4K Refresh Module
A0~A7	Column Addresses for 4K Refresh Module
DQ0~DQ31	Data Inputs/Outputs
RAS0#, RAS2#	Row Address Strobes
CAS0#~CAS3#	Column Address Strobes
WE#	Write Enable
PD1~PD4	Presence Detects
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Presence Detect Pins

	Access Time		
Pin	60ns	70ns	80ns
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	37	NC
2	DQ0	38	NC
3	DQ16	39	V_{SS}
4	DQ1	40	CAS0#
5	DQ17	41	CAS2#
6	DQ2	42	CAS3#
7	DQ18	43	CAS1#
8	DQ3	44	RAS0#
9	DQ19	45	NC
10	V_{CC}	46	NC
11	NC	47	WE#
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10 (Note)	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	V_{CC}
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	A11 (Note)	65	DQ15
30	V_{CC}	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	RAS2#	70	PD4
35	NC	71	NC
36	NC	72	V_{SS}

Note : A10 & A11 are NC for 1 K refresh module.

DC Characteristics

FPM & EDO-based Modules

Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		Vcc=3.3V	Vcc=5.0V	
Voltage on any pin relative to V_{SS}	V_T	- 0.5 to +4.6	- 1.0 to +7.0	V
Power Dissipation	P_T	2	2	W
Operating Temperature	T_{opr}	0 to +70	0 to +70	°C
Storage Temperature	T_{stg}	- 55 to +150	- 55 to +150	°C
Short Circuit Output Current	I_{OS}	50	50	mA

Recommended DC Operating Conditions

(T_A = 0 to +70°C)

Parameter	Symbol	Vcc=3.3V			Vcc=5.0V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC} +0.3	2.4	-	V_{CC}+1.0	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	-1.0	-	0.8	V

Capacitance

(V_{CC} = 3.3V±10%/5.0V±10%, T_A = +25°C)

Parameter	Symbol	Max	Unit
Input Capacitance (Address)	CI1	20	pF
Input Capacitance (RAS#, CAS#)	C_{I2}	17	pF
Input Capacitance (WE#)	C_{I3}	24	pF
Input/Output Capacitance (DQ0~DQ31)	$C_{I/O}$	17	pF

Notes : Capacitance is sampled per Mil-Std-883.

DC Characteristics (cont'd)

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	60ns		70ns		80ns		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{CC}+0.3V$	-20	20	-20	20	-20	20	µA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le V_{CC}$ D_{out} = Disable	-10	10	-10	10	-10	10	µA
Output High Voltage	V_{OH}	High I_{out} = -2mA	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	Low I_{out} = 2mA	-	0.4	-	0.4	-	0.4	V

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	60ns		70ns		80ns		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{CC}+0.5V$	-20	20	-20	20	-20	20	µA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le V_{CC}$ D_{out} = Disable	-10	10	-10	10	-10	10	µA
Output High Voltage	V_{OH}	High I_{out} = -5mA	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	Low I_{out} = 4.2mA	-	0.4	-	0.4	-	0.4	V

DC Characteristics (cont'd)

FPM-based Modules

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 60ns	Max. 70ns	Max. 80ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	1K	300	280	260	mA	1, 2
		t_{RC} = min.	4K	180	160	140	mA	1, 2
Standby Current	I_{CC2}	LVTTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		4	4	4	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		2	2	2	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=VIH; RAS#, Address	1K	300	280	260	mA	2
		cycling @ t_{RC}=min.	4K	180	160	140	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @	1K	300	280	260	mA	
		t_{RC}=min.	4K	180	160	140	mA	
Fast Page Mode Current	I_{CC5}	RAS#=VIL, CAS#, Address	1K	200	180	160	mA	1, 3
		cycling @ t_{PC}=min.	4K	180	160	140	mA	1, 3

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 60ns	Max. 70ns	Max. 80ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	1K	320	300	280	mA	1, 2
		t_{RC} = min.	4K	200	180	160	mA	1, 2
Standby Current	I_{CC2}	TTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		4	4	4	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		2	2	2	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=V_{IH}; RAS#, Address	1K	320	300	280	mA	2
		cycling @ t_{RC}=min.	4K	200	180	160	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @	1K	320	300	280	mA	
		t_{RC}=min.	4K	200	180	160	mA	
Fast Page Mode Current	I_{CC5}	RAS#=V_{IL}, CAS#, Address	1K	220	200	180	mA	1, 3
		cycling @ t_{PC}=min.	4K	200	180	160	mA	1, 3

Notes: 1. Values depend on output load condition when the device is selected. Maximum values are specified at the output open condition.
2. Address can be changed once or less while RAS# = V_{IL} .
3. Address can be changed once or less while CAS# = V_{IH} .

DC Characteristics (cont'd)

EDO-based Modules

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 60ns	Max. 70ns	Max. 80ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	1K	300	280	260	mA	1, 2
		t_{RC} = min.	4K	180	160	140	mA	1, 2
Standby Current	I_{CC2}	LVTTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		4	4	4	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		2	2	2	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=V_{IH}; RAS#, Address cycling @ t_{RC}=min.	1K	300	280	260	mA	2
			4K	180	160	140	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	1K	300	280	260	mA	
			4K	180	160	140	mA	
Hyper Page Mode Current	I_{CC5}	RAS#=V_{IL}, CAS#, Address cycling @ t_{HPC}=min.	1K	240	220	200	mA	1, 3
			4K	220	200	180	mA	1, 3

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 60ns	Max. 70ns	Max. 80ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	1K	320	300	280	mA	1, 2
		t_{RC} = min.	4K	200	180	160	mA	1, 2
Standby Current	I_{CC2}	TTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		4	4	4	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		2	2	2	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=V_{IH}; RAS#, Address cycling @ t_{RC}=min.	1K	320	300	280	mA	2
			4K	200	180	160	mA	
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	1K	320	300	280	mA	
			4K	200	180	160	mA	
Hyper Page Mode Current	I_{CC5}	RAS#=V_{IL}, CAS#, Address cycling @ t_{HPC}=min.	1K	260	240	220	mA	1, 3
			4K	240	220	200	mA	1, 3

Notes: 1. Values depend on output load condition when the device is selected. Maximum values are specified at the output open condition.
2. Address can be changed once or less while RAS# = V_{IL} .
3. Address can be changed once or less while CAS# = V_{IH} .

AC Characteristics

FPM-based Modules

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	60ns		70ns		80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Common to Read and Write Cycles									
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	10	-	15	-	15	-	ns	
CAS# pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	
CAS# to output in Low-Z	t_{CLZ}	0	-	0	-	0	-	ns	3
CAS# to RAS# precharge time	t_{CRP}	5	-	5	-	5	-	ns	
CAS# hold time	t_{CSH}	60	-	70	-	80	-	ns	
RAS# to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	10
Row address hold time	t_{RAH}	10	-	10	-	10	-	ns	
RAS# pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
Random read/write cycle time	t_{RC}	110	-	130	-	150	-	ns	
RAS# to CAS# delay time	t_{RCD}	20	45	20	50	20	60	ns	4
RAS# precharge time	t_{RP}	40	-	50	-	60	-	ns	
RAS# hold time	t_{RSH}	15	-	20	-	20	-	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
Read Cycle									
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	3, 10
Access time from CAS#	t_{CAC}	-	13	-	20	-	20	ns	3, 4, 5
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	15	ns	6
Access time from RAS#	t_{RAC}	-	60	-	70	-	80	ns	3, 4
Column address to RAS# lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command hold time referenced to CAS#	t_{RCH}	0	-	0	-	0	-	ns	8
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time referenced to RAS#	t_{RRH}	0	-	0	-	0	-	ns	8
Write Cycle									
Write command to CAS# lead time	t_{CWL}	15	-	15	-	20	-	ns	
Data-in hold time	t_{DH}	10	-	15	-	15	-	ns	9
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	9
Write command to RAS# lead time	t_{RWL}	15	-	15	-	20	-	ns	
Write command hold time	t_{WCH}	10	-	15	-	15	-	ns	
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	7
Write command pulse width	t_{WP}	10	-	15	-	15	-	ns	

AC Characteristics (cont'd)

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	60ns		70ns		80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page Mode Cycle									
Access time from CAS# precharge	t_{ACP}	-	35	-	40	-	45	ns	3, 11
CAS# precharge time	t_{CP}	10	-	10	-	10	-	ns	
Fast page mode cycle time	t_{PC}	40	-	45	-	50	-	ns	
RAS# pulse width	t_{RASP}	60	200000	70	200000	80	200000	ns	12
RAS# hold time from CAS# precharge	t_{RHCP}	35	-	40	-	45	-	ns	
Refresh Cycle									
CAS# hold time (CBR refresh)	t_{CHR}	10	-	10	-	10	-	ns	1
CAS# set-up time (CBR refresh)	t_{CSR}	10	-	10	-	10	-	ns	1
Refresh period	t_{REF}								
1K refresh		-	16	-	16	-	16	ms	
4K refresh		-	64	-	64	-	64	ms	
RAS# precharge to CAS# hold time	t_{RPC}	5	-	5	-	5	-	ns	

EDO-based Modules

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	60ns		70ns		80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Common to Read and Write Cycles									
Column address hold time referenced to RAS#	t_{AR}	45	-	55	-	60	-	ns	13
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Column address hold time	t_{CAH}	10	-	15	-	15	-	ns	
CAS# pulse width	t_{CAS}	10	10000	15	10000	20	10000	ns	
CAS# to output in Low-Z	t_{CLZ}	3	-	3	-	3	-	ns	3
CAS# to RAS# precharge time	t_{CRP}	5	-	5	-	5	-	ns	
CAS# hold time	t_{CSH}	50	-	60	-	70	-	ns	
RAS# to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	10
Row address hold time	t_{RAH}	10	-	10	-	10	-	ns	
RAS# pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
Random read/write cycle time	t_{RC}	110	-	130	-	150	-	ns	
RAS# to CAS# delay time	t_{RCD}	20	45	20	50	20	60	ns	4
RAS# precharge time	t_{RP}	40	-	50	-	60	-	ns	
RAS# hold time	t_{RSH}	17	-	20	-	20	-	ns	
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2

AC Characteristics (cont'd)

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	60ns		70ns		80ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle									
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	3, 10
Access time from CAS#	t_{CAC}	-	17	-	20	-	20	ns	3, 4, 5
Output buffer turn-off time to CAS#	t_{CEZ}	3	15	3	20	3	20	ns	6
Access time from RAS#	t_{RAC}	-	60	-	70	-	80	ns	3, 4
Column address to RAS# lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command hold time referenced to CAS#	t_{RCH}	0	-	0	-	0	-	ns	8
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Output buffer turn-off delay to RAS#	t_{REZ}	3	15	3	20	3	20	ns	
Read command hold time referenced to RAS#	t_{RRH}	0	-	0	-	0	-	ns	8
Write Cycle									
Write command to CAS# lead time	t_{CWL}	10	-	15	-	20	-	ns	
Data-in hold time	t_{DH}	10	-	15	-	15	-	ns	9
Data-in hold time to RAS#	t_{DHR}	45	-	55	-	60	-	ns	13
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	9
Write command to RAS# lead time	t_{RWL}	15	-	15	-	20	-	ns	
Write command hold time	t_{WCH}	10	-	15	-	15	-	ns	
Write command hold time referenced to RAS#	t_{WCR}	45	-	50	-	55	-	ns	13
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	7
Write command pulse width	t_{WP}	10	-	15	-	15	-	ns	
Hyper Page Mode Cycle									
Access time from CAS# precharge	t_{ACP}	-	35	-	40	-	45	ns	3, 11
CAS# precharge time	t_{CP}	10	-	10	-	10	-	ns	
Output data hold time	t_{DOH}	5	-	5	-	5	-	ns	
Hyper page mode cycle time	t_{HPC}	24	-	29	-	34	-	ns	
RAS# pulse width	t_{RASP}	60	200000	70	200000	80	200000	ns	12
RAS# hold time from CAS# precharge	t_{RHCP}	35	-	40	-	45	-	ns	
Refresh Cycle									
CAS# hold time (CBR refresh)	t_{CHR}	10	-	10	-	10	-	ns	1
CAS# set-up time (CBR refresh)	t_{CSR}	10	-	10	-	10	-	ns	1
Refresh period	t_{REF}								
1K refresh		-	16	-	16	-	16	ms	
4K refresh		-	64	-	64	-	64	ms	
RAS# precharge to CAS# hold time	t_{RPC}	5	-	5	-	5	-	ns	

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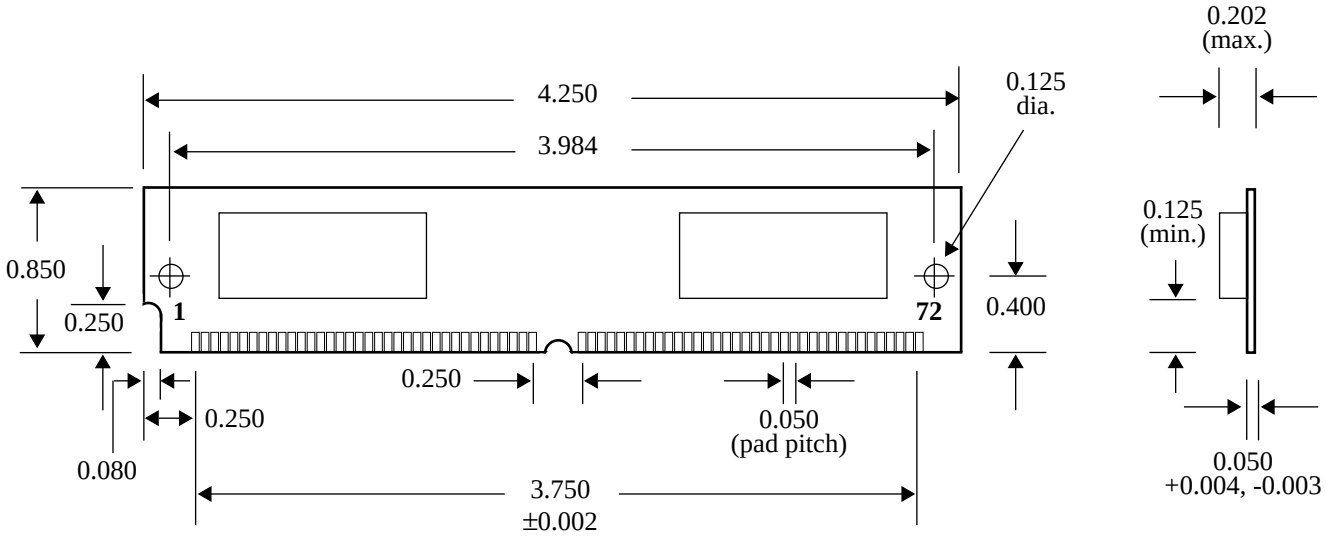
Notes:

1. An initial pause of atleast 200µs is required after power-up followed by any eight RAS# cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) limit can be met; t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS# leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. Access time is determined by the longer of t_{AA} , t_{CAC} or $t_{ACP.}$
12. t_{RASP} defines RAS# pulse width in fast page mode cycles.
13. $t_{AR,}$ $t_{WC,}$ t_{DHR} are referenced to t_{RAD}(max).

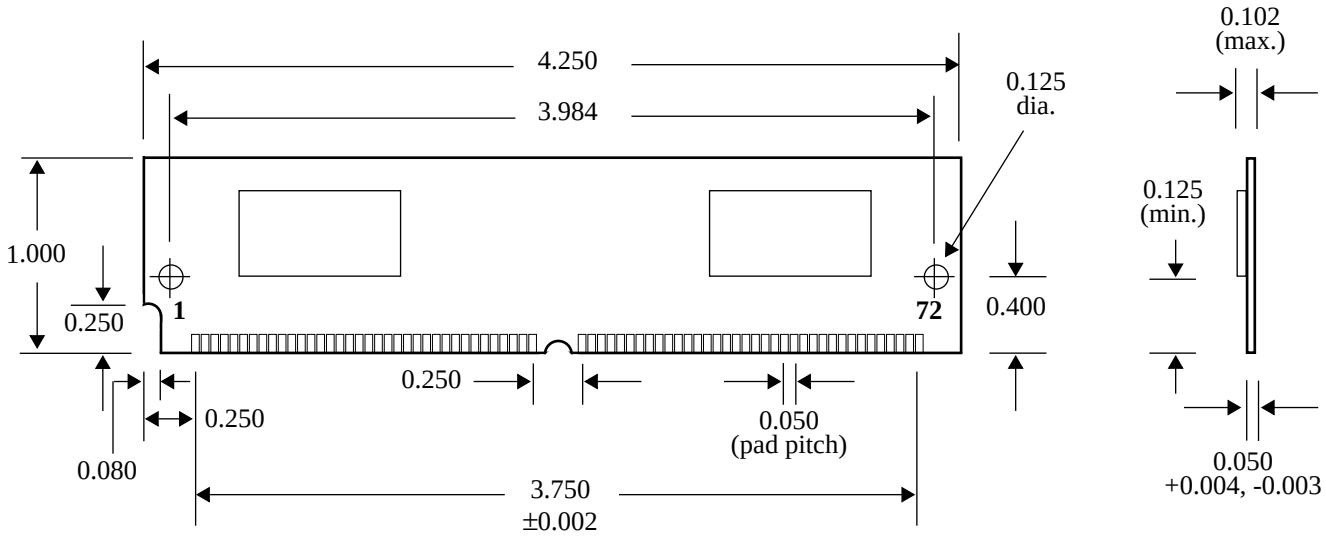
Physical Dimensions

72-pin SIMM Module

SOJ Based



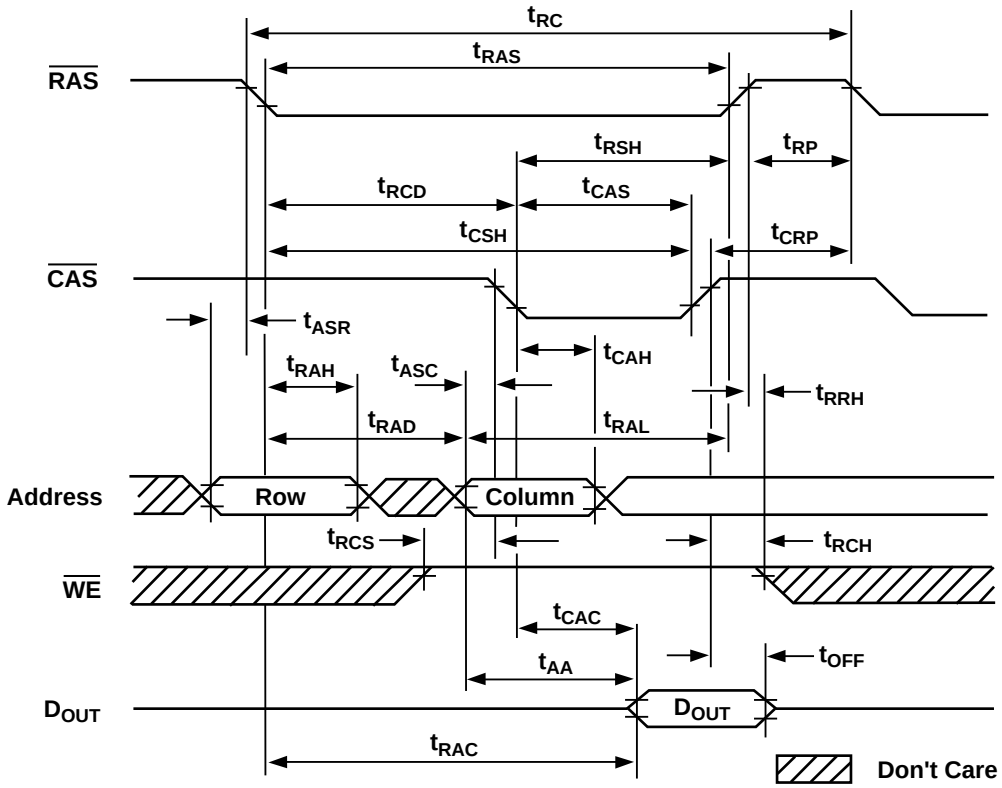
TSOP Based



(All dimensions are in inches with ±0.005” tolerance unless specified otherwise.)

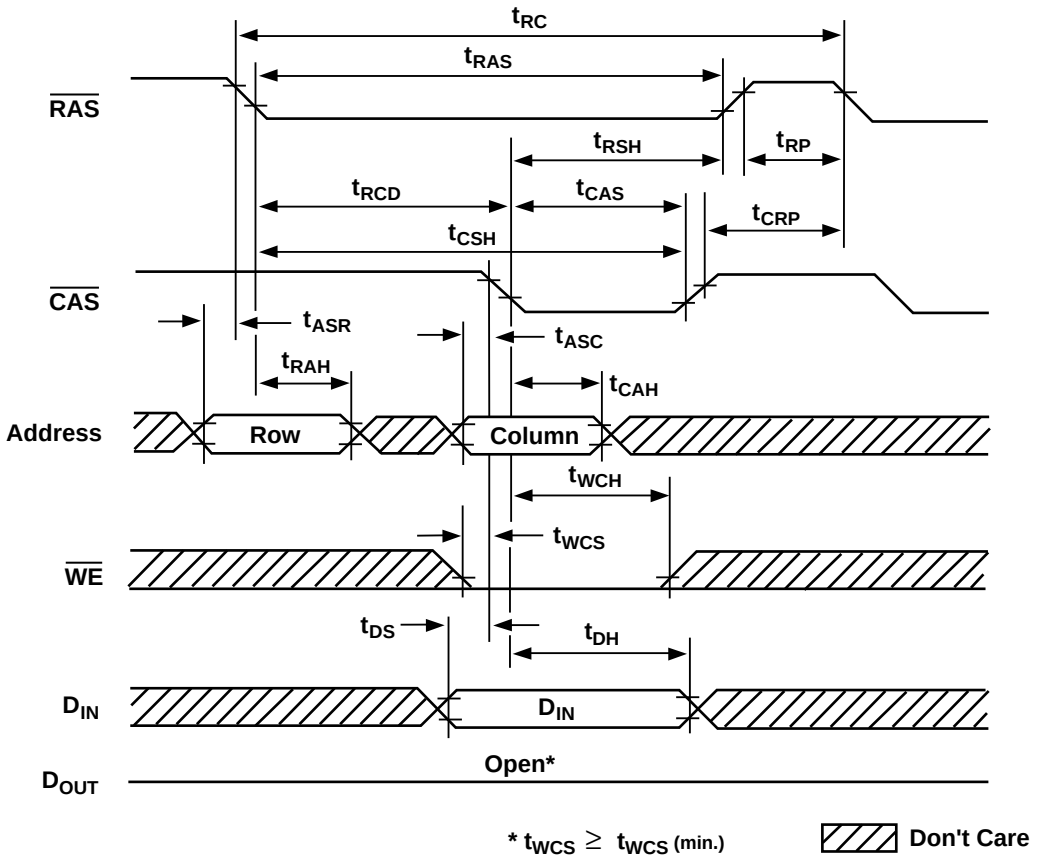
FPM-based Module Timing Waveforms

Read Cycle



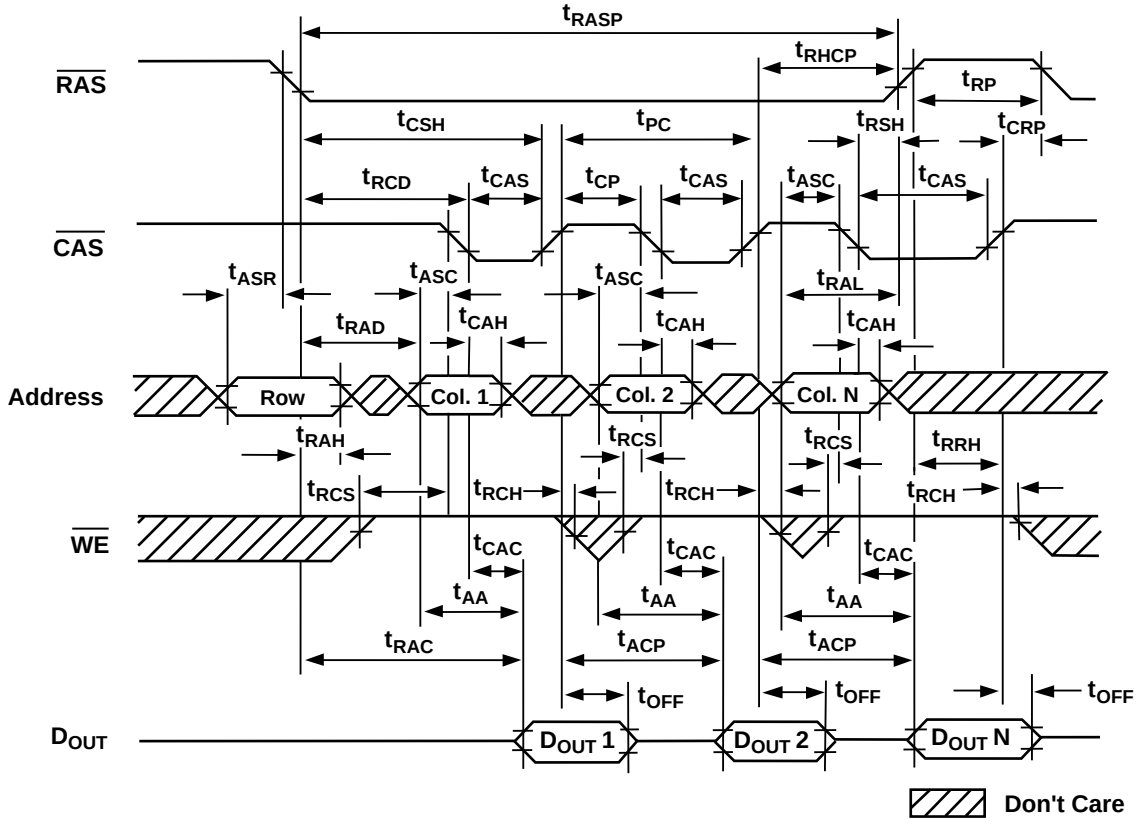
FPM-based Module Timing Waveforms (cont'd)

Write Cycle (Early Write)



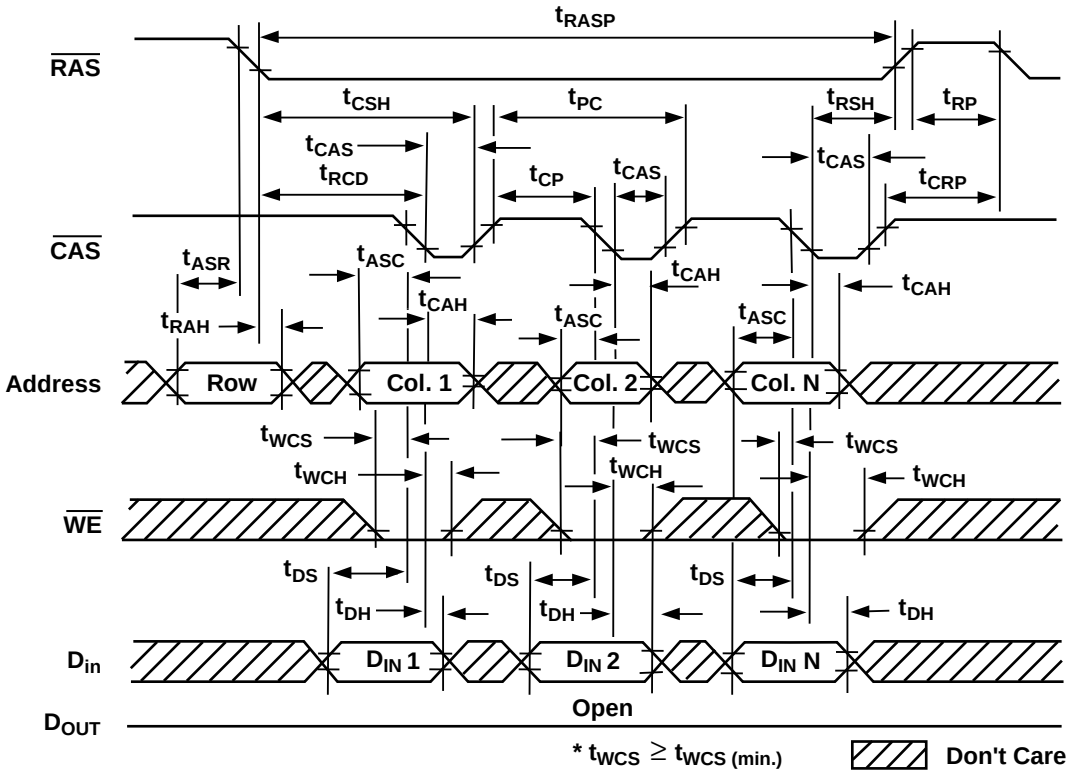
FPM-based Module Timing Waveforms (cont'd)

Fast Page Mode Read Cycle



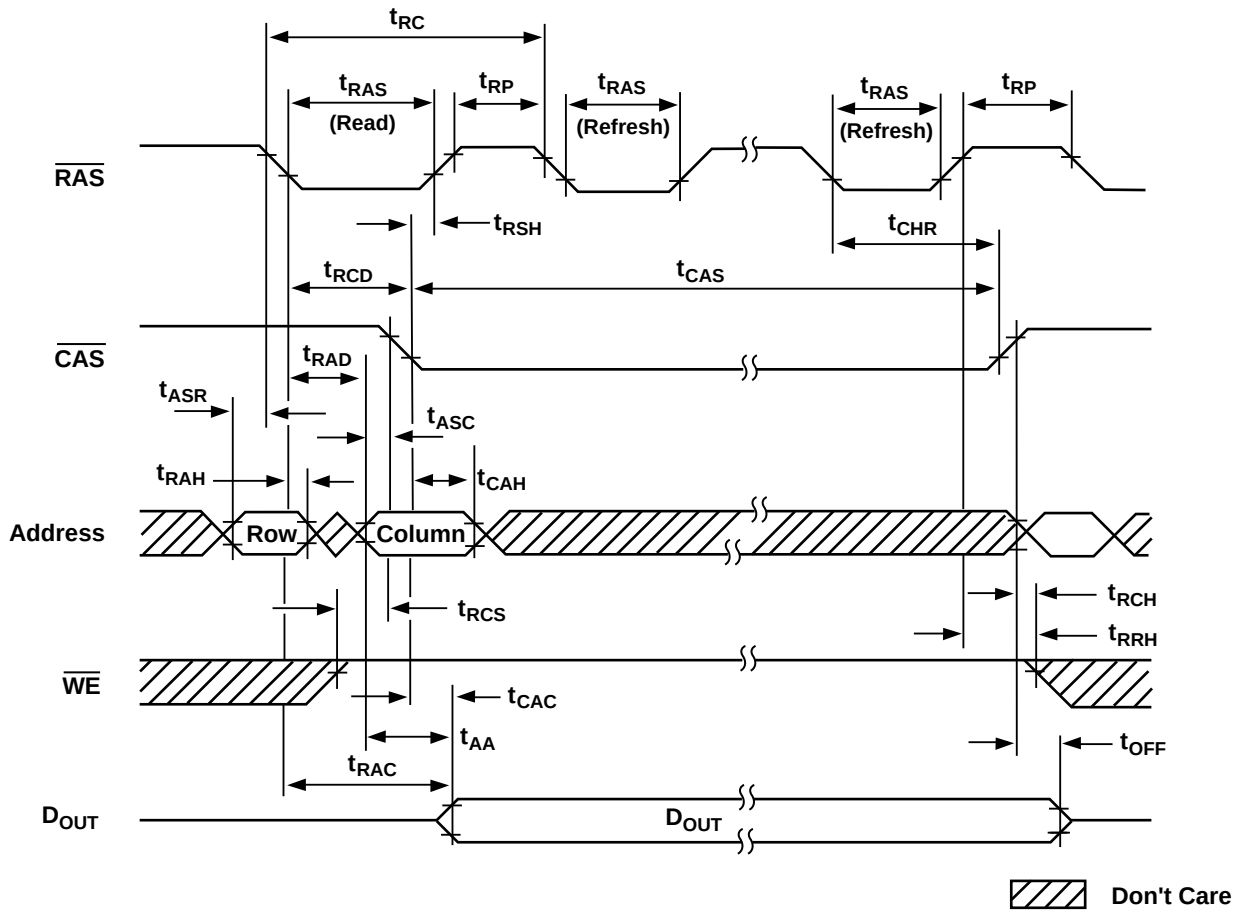
FPM-based Module Timing Waveforms (cont'd)

Fast Page Mode Write Cycle (Early Write)



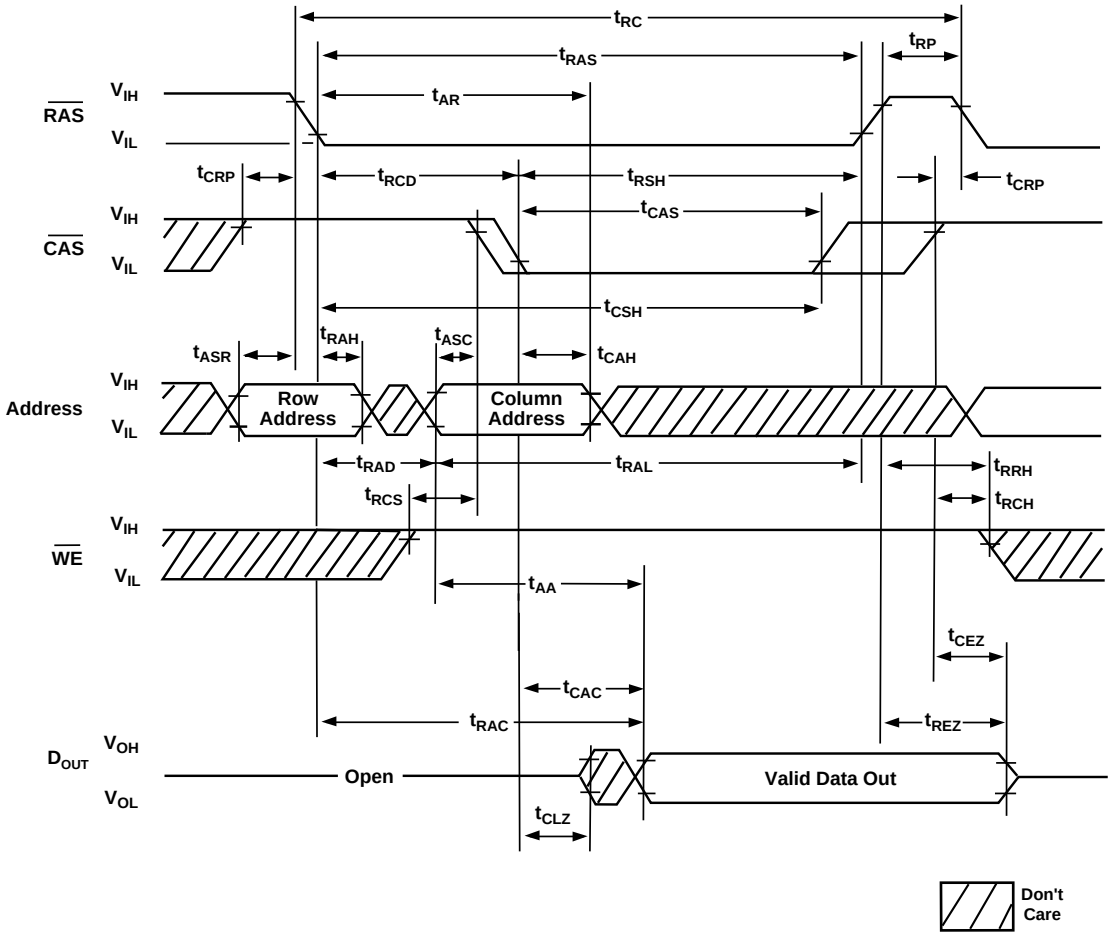
FPM-based Module Timing Waveforms (cont'd)

Hidden Refresh Cycle



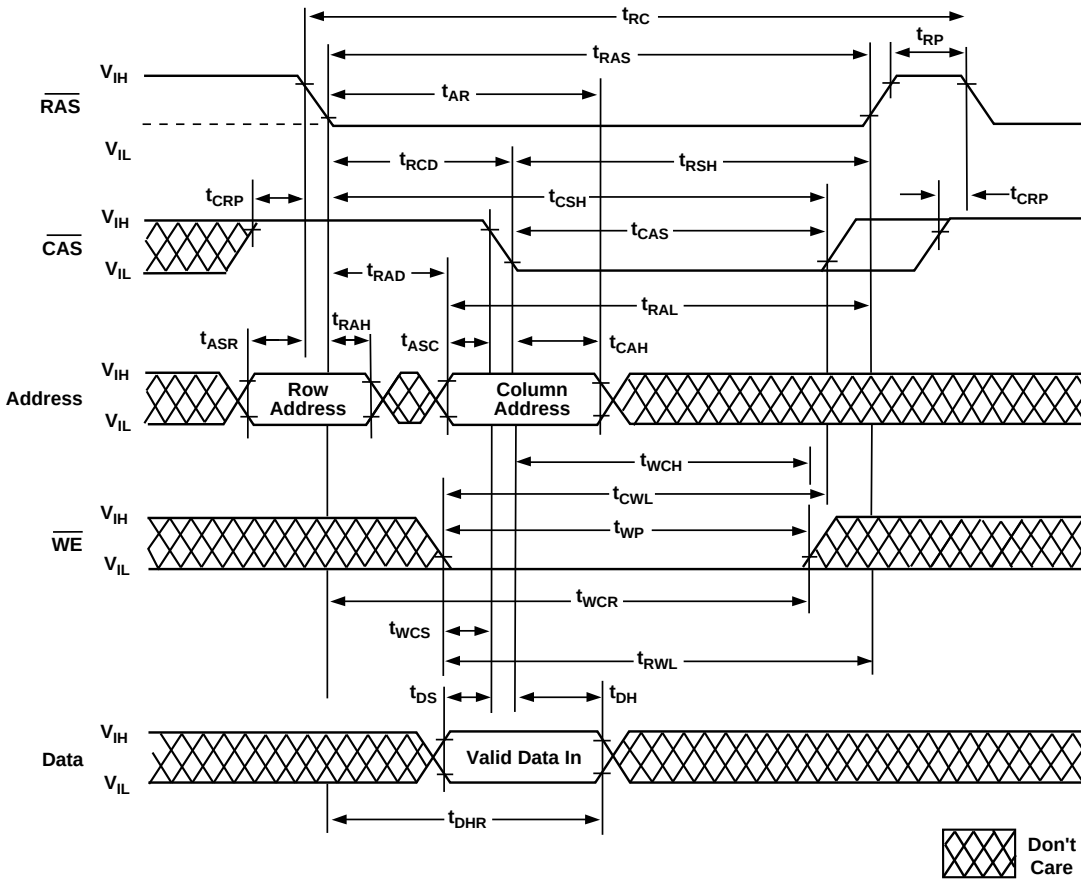
EDO-based Module Timing Waveforms

Read Cycle



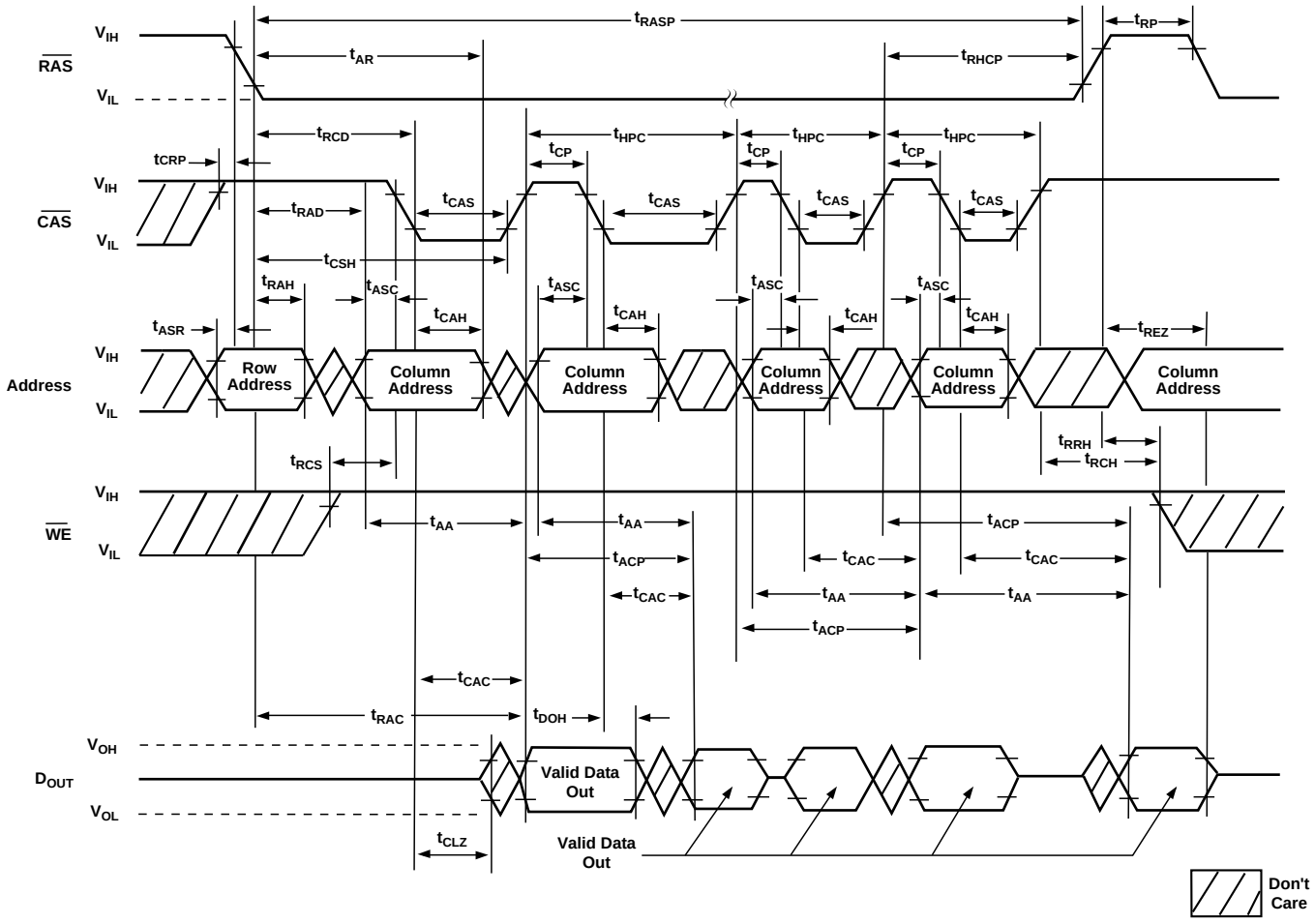
EDO-based Module Timing Waveforms (cont'd)

Write Cycle (Early Write)



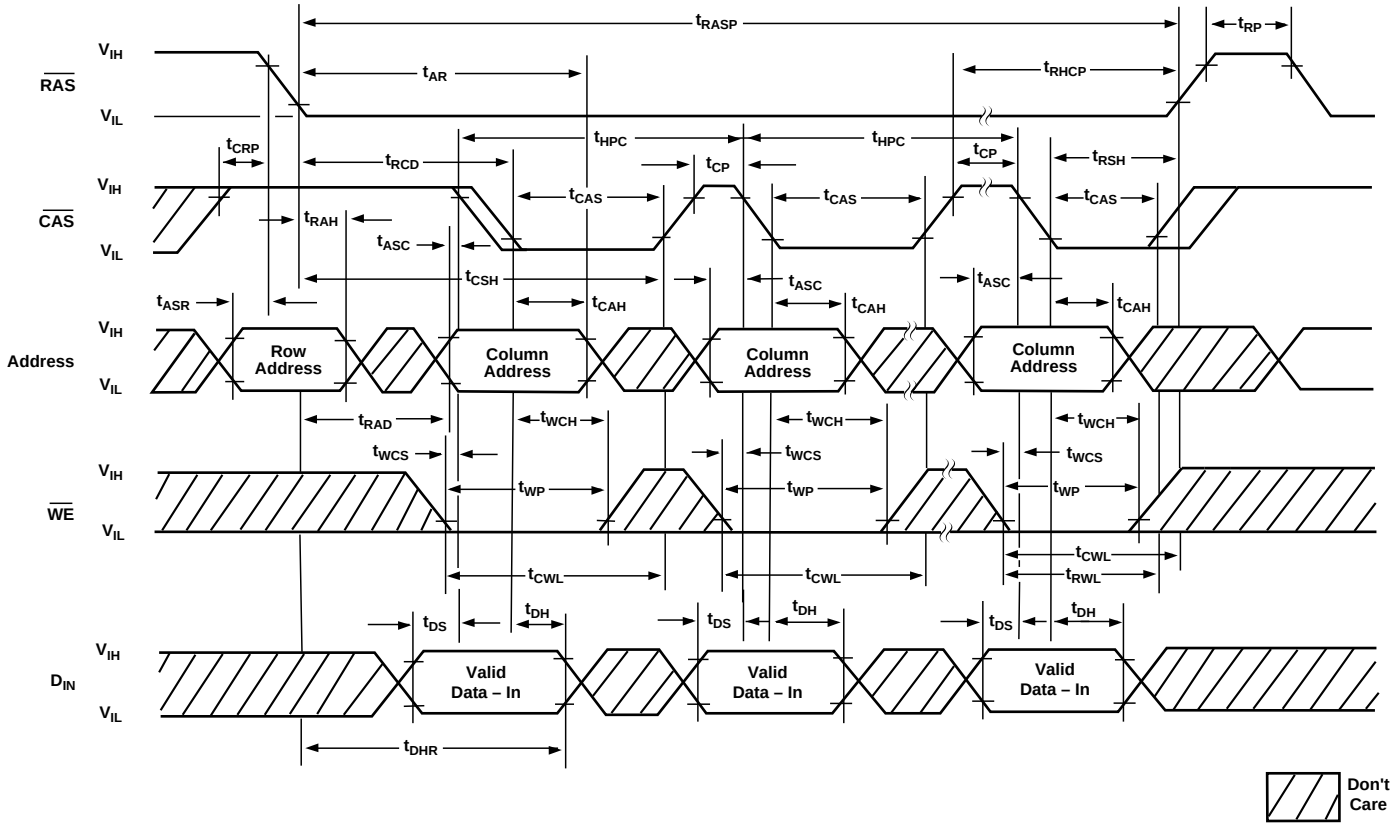
EDO-based Module Timing Waveforms (cont'd)

Hyper Page Read Cycle



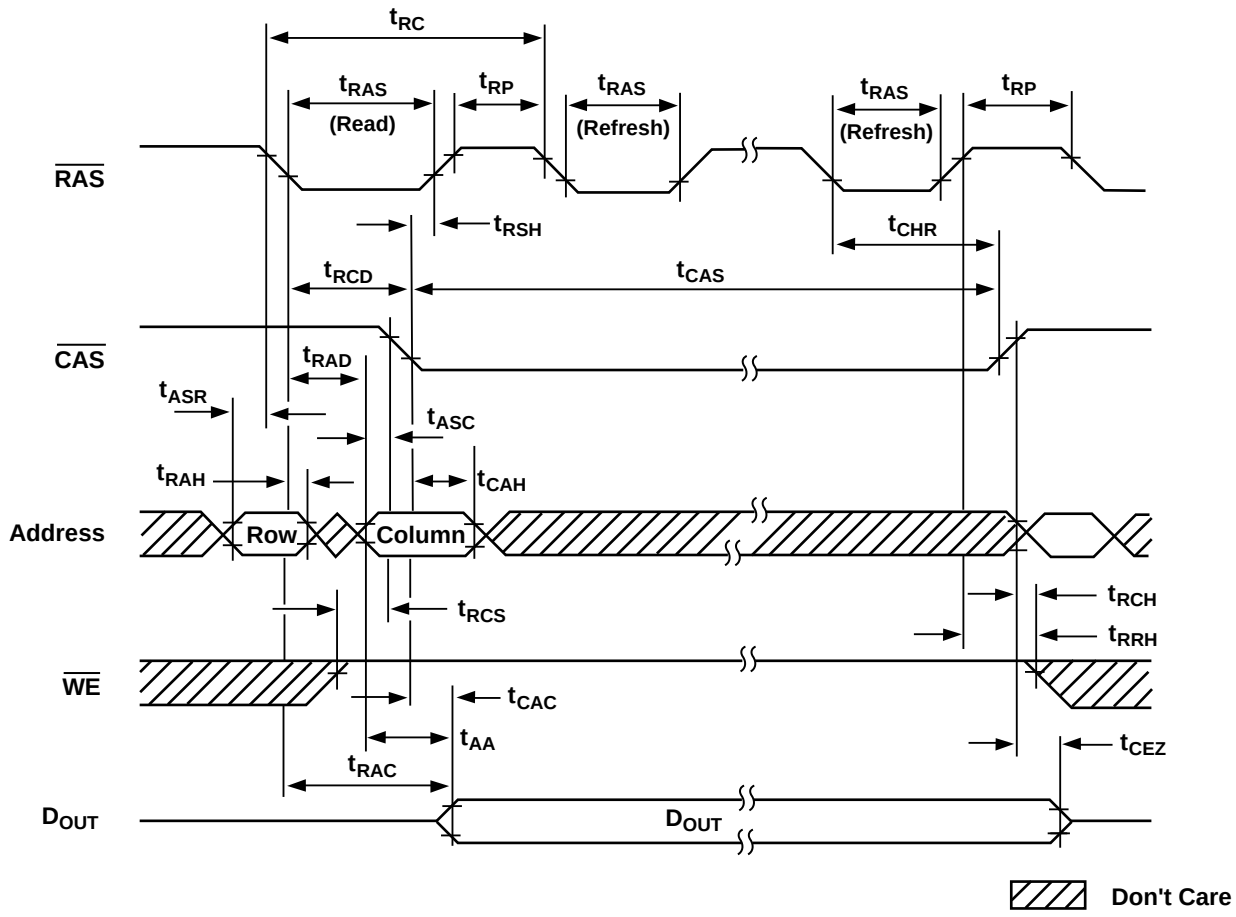
EDO-based Module Timing Waveforms (cont'd)

Hyper Page Write Cycle (Early Write)



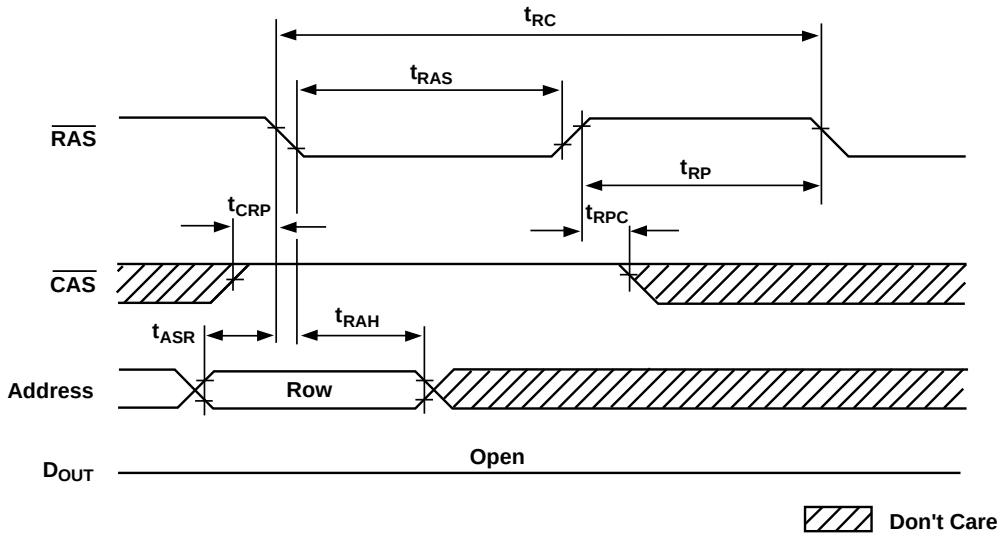
EDO-based Module Timing Waveforms (cont'd)

Hidden Refresh Cycle

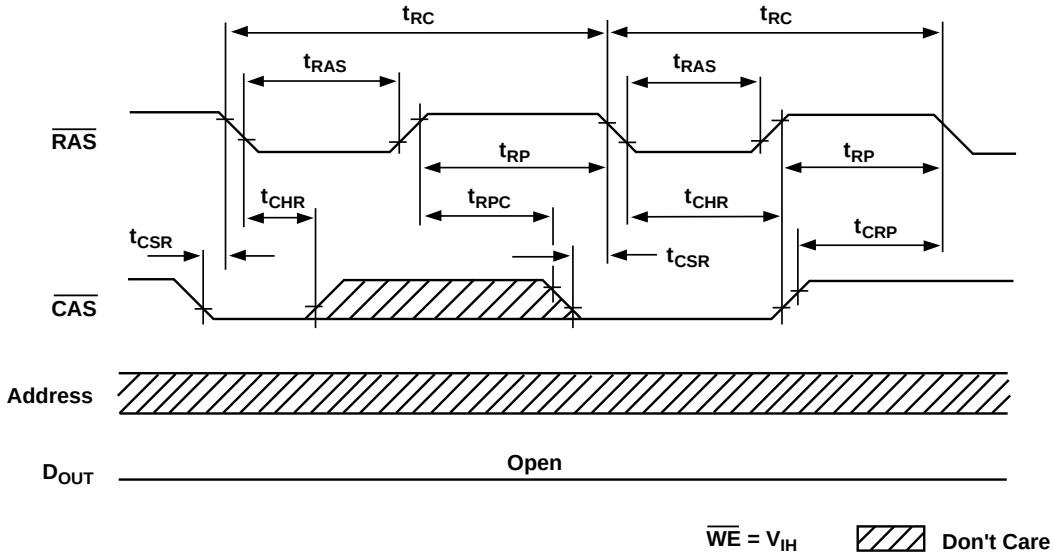


FPM & EDO-based Module Timing Waveforms (cont'd)

RAS# Only Refresh Cycle



CAS#-Before-RAS# Refresh Cycle



Ordering Information

SM	5	32	01	3	0	U	U	X	U	U	U
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)

(1) **SMART**
Modular Technologies

(2) **Product Category**
5 : DRAM SIMM / DIMM

(3) **Module Data Bus Width**
32 : x32

(4) **Module Address Depth**
01 : 1M

(5) **Device Data Width**
3 : x16

(6) **Special Device Feature**
0 : Standard

(7) **Voltage / Mode**
0 : 5.0V / Fast Page Mode
1 : 3.3V / Fast Page Mode
8 : 5.0V / Hyper Page Mode (EDO)
9 : 3.3V / Hyper Page Mode (EDO)

(8) **Refresh / Power**
1 : 1K Ref. / Standard Power
4 : 4K Ref. / Standard Power

(9) **Module Configuration**
X : Non-Parity

(10) **Device Physicals**
4 : SOJ DRAMs (400mil)
6 : TSOP DRAMs (400mil)

(11) **Module Lead Finish**
S : Solder
G : Gold

(12) **Module Access Speed**
6 : 60ns
7 : 70ns
8 : 80ns

Note : “U” in the part number should be replaced by user specified option.

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