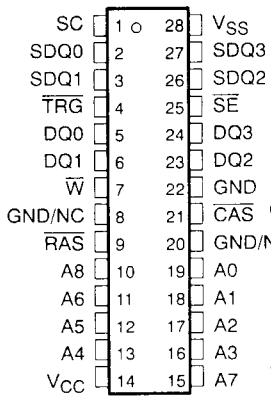
REV A — SMVS250 — JUNE 1990 — REVISED JANUARY 1991

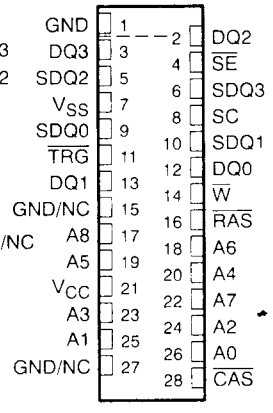
- DRAM: 262 144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Dual Port Accessibility — Simultaneous and Asynchronous Access from the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- Write Per Bit Feature for Selective Write to Each RAM I/O.
- Enhanced Page Mode Operation for Faster Access
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes
- RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Long Refresh Period . . . Every 8 ms (Max)
- DRAM Port Is Compatible with the TMS44C256
- Up to 33 MHz Uninterrupted Serial Data Streams
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- 512 Selectable Serial Register Starting Locations
- All Inputs and Outputs TTL Compatible
- Performance Ranges: V_{CC} ± 10%

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS44C250-10	100 ns	25 ns	30 ns	20 ns
TMS44C250-12	120 ns	30 ns	35 ns	25 ns

DZ Package
(Top View)



SD Package
(Top View)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0-DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0-SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
GND/NC	No Connect or Ground Only
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: not connected to internal V_{SS})

- Performance Ranges: V_{CC} ± 5%

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$
TMS44C250-1	100 ns	25 ns	30 ns	20 ns

- Texas Instruments EPIC™ CMOS Process

description

The TMS44C250 Multiport Video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each, interfaced to a serial data register, or Serial Access Memory (SAM), organized as 512 words of 4 bits each. The TMS44C250 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer

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operations, the TMS44C250 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle. The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz.

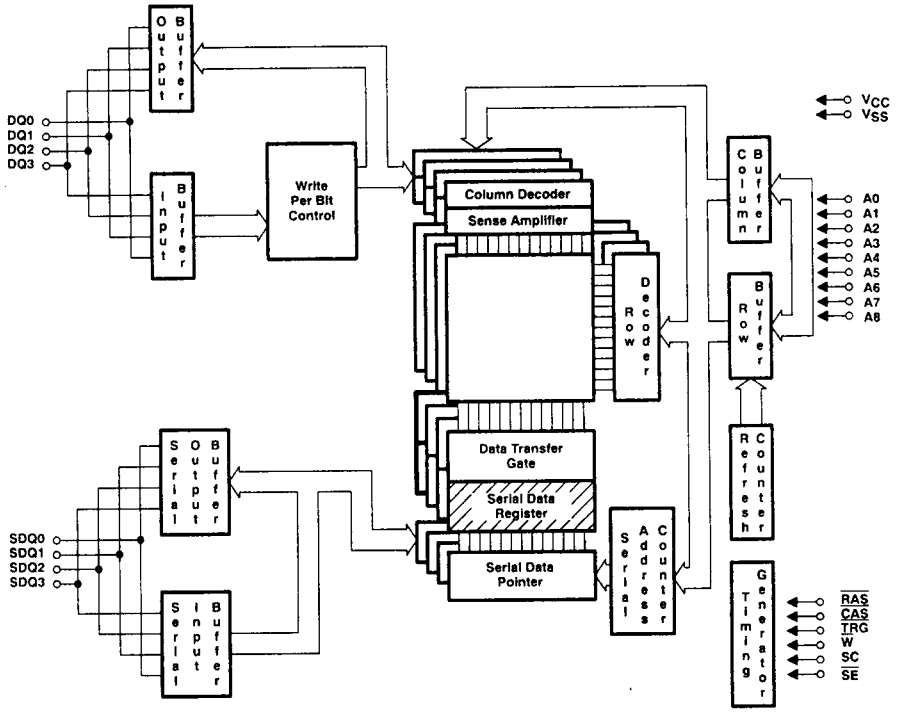
All inputs, outputs, and clock signals on the TMS44C250 are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The TMS44C250 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

The TMS44C250 is offered in a 28-pin small-outline J-leaded package (DZ suffix) for direct surface mounting in rows on 400-mil (5,08-mm) centers. It is also offered in a 400-mil, 28-pin zig-zag in-line package (SD suffix). Both packages are characterized for operation from 0°C to 70°C (L suffix).

The TMS44C250 and other Multiport Video RAMs are supported by a broad line of graphics processor and control devices from Texas Instruments.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0-A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
$\overline{RAS}$	Row Enable	Row Enable	
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write per Bit Select	Transfer Write Enable	
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND/NC	No Connect or Ground Only		
GND	System Ground		

operation

random access operation

Refer to Table 1, Functional Table, for Random Access and Transfer Operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a " T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See "Transfer Operation" for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then, the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, and $\overline{CAS}$, onto the chip to invoke the various DRAM and Transfer functions of the TMS44C250. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write per bit mode of operation. A logic high level on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write per bit operation.

A four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a 0 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a 1 was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

See the corresponding timing diagrams for details. IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write per bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0-DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed-in by $\overline{W}$ with data setup and hold times referenced to this signal.

The three-state output buffers provide direct TTL compatability (no pullup resistors required) with a fanout of two Series 74 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ and $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory to register or register to memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows theTMS44C250 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The TMS44C250 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

GND

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground or left floating (no connection) to ensure proper device operation.

IMPORTANT: GND is not connected internally to V_{SS}.

Table 1. Functional Table

TYPE†	RAS FALL				ADDRESS		DQ0-DQ3		FUNCTION
	CAS	TRG	W	SE	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	CAS-Before-RAS Refresh
T	H	L	L	L	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	Refresh Addr	Tap Point	X	X	Serial Write-mode Enable (Pseudo-Transfer Write)
T	H	L	H	X	Row Addr	Tap Point	X	X	Memory to Register Transfer (Transfer Read)
R	H	H	L	X	Row Addr	Col Addr	Write Mask	Valid Data	Load and use Write Mask, Write Data to Dram
R	H	H	H	X	Row Addr	Col Addr	X	Valid Data	Normal Dram Read/Write (Non Masked)

† R = Random access operation; T = Transfer operation.
‡ DQ0-3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
WRITE MASK = 1 write to I/O enabled.

random port to serial port interface

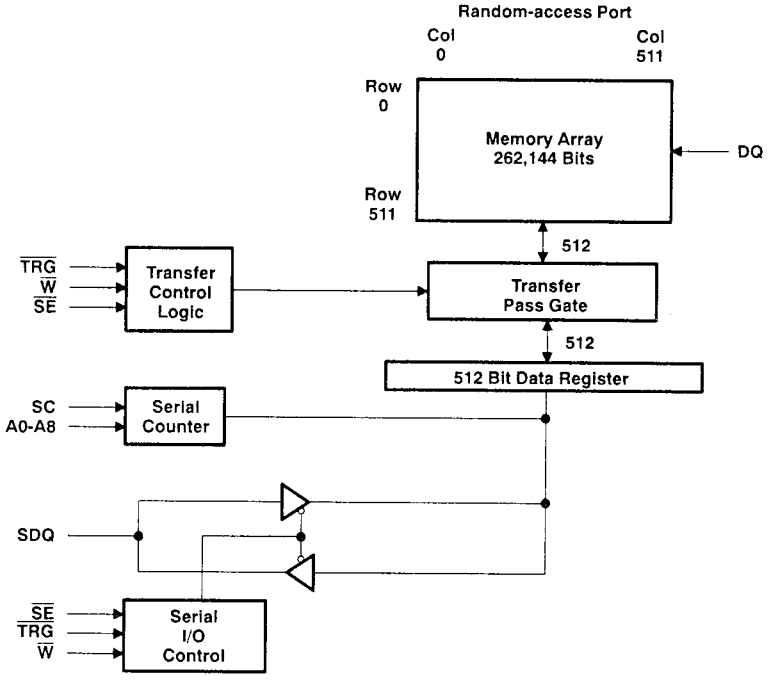


Figure 1. Block Diagram Showing One Random and One Serial I/O Interface

random address space to serial address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

transfer operations

As illustrated in Table 1, the TMS44C250 supports three basic transfer modes of operation:

1. Write Transfer (SAM to DRAM)
2. Pseudo Write Transfer (Switches serial port from serial out mode to serial in mode. No actual data transfer takes place between the DRAM and the SAM.)
3. Read Transfer (Transfer entire contents of DRAM to SAM)

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$ and $\overline{SE}$, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or "tap," position.

transfer write enable ($\overline{W}$)

In register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. This allows serial data to be input into the SAM. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0-A8 are latched on the fallling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be accessed, the appropriate 9-bit column address (A0-A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The TMS44C250 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0-SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The Serial Enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 3.) If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	MODE
L	L	L	Register to memory (write) transfer
L	L	H	Serial write mode enable
L	H	X	Memory to register (read) transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

Table 3. Serial Operation Logic

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Serial write mode enable†	L	Input enable
Serial write mode enable†	H	Input disable
Memory to register	L	Output enabled
Memory to register	H	Hi-Z

†Pseudo transfer write

power up

To achieve proper device operation, an initial pause of 200 μs is required after power up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle and two SC cycles.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage on any pin except DQ and SDQ (see Note 1) ..... – 1 V to 7 V
Voltage on DQ and SDQ (see Note 1) ..... – 1 V to V_{CC}
Voltage range on V_{CC} (see Note 1) ..... 0 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	TMS44C250-1	4.75	5	5.25	V
		TMS44C250-10, TMS44C250-12	4.5	5	5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.4		V_{CC}	V
V_{IL}	Low-level input voltage (see Note 2)		– 1.0		0.8	V
V_{OH}	High-level output voltage		2.4		V_{CC}	V
V_{OL}	Low-level output volage		– 1		0.4	V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
				MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage		I_{OH} = −5.0 mA	2.4		2.4		V
V_{OL}	Low level output voltage		I_{OL} = 4.2 mA		0.4		0.4	V
I_L	Input leakage current	TMS44C250-10, TMS44C250-12	V_I = 0 V to 5.8 V, V_{CC} = 5.5 V All other pins = 0 V to V_{CC}		±10		±10	μA
		TMS44C250-1	V_I = 0 V to 5.55 V, V_{CC} = 5.25 V All other pins = 0 V to V_{CC}		±10		±10	μA
I_O	Output leakage current (see Note 3)	TMS44C250-10, TMS44C250-12	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V		±10		±10	μA
I_O	Output leakage current (see Note 3)	TMS44C250-1	V_O = 0 V to V_{CC}, V_{CC} = 5.25 V		±10		±10	μA

PARAMETER		SAM PORT	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Operation current $t_{c(RW)}$ = Minimum	Standby		90		80	mA
I_{CC1A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC2}	Standby current, All clocks = V_{CC}	Standby		10		10	
I_{CC2A}	$t_{c(SC)}$ = Minimum	Active		35		35	
I_{CC3}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC3A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC4}	Page mode current, $t_{c(P)}$ = Minimum	Standby		50		45	
I_{CC4A}	$t_{c(SC)}$ = Minimum	Active		60		55	
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC5A}	$t_{c(SC)}$ = Minimum	Active		110		95	
I_{CC6}	Data transfer current, $t_{c(RW)}$ = Minimum	Standby		90		80	
I_{CC6A}	$t_{c(SC)}$ = Minimum	Active		110		95	

NOTE 3: $\overline{SE}$ is disabled for SDQ output leakage tests.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 4)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		7	pF

NOTE 4: V_{CC} equal to 5 V ± 0.5 V for TMS44C250-10, and TMS44C250-12; 5 V ± 0.25 V for TMS44C250-1, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}	0	25		30	ns
$t_{A(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60	ns
$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MAX	t_{CAP}		55		65	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		100		120	ns
$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 50 pF	t_{SCA}		30		35	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 50 pF	t_{SEA}		20		25	ns
$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high	C_L = 100 pF	t_{OFF}	0	20	0	20	ns
$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high	C_L = 100 pF	t_{OEZ}	0	20	0	20	ns
$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high	C_L = 50 pF	t_{SEZ}	0	20	0	20	ns

NOTE 5: Switching times assume C_L = 100 pF unless otherwise noted (see Figure 2).

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 6)	t_{RC}	190		220		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	250		290		ns
$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{RWC}	105		125		ns
$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		ns
$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		ns
$t_{c(SC)}$	Serial clock cycle time (see Note 7)	t_{SCC}	30		35		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 8)	t_{CAS}	25	75 000	30	75 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 9)	t_{RAS}	100	75 000	120	75 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		35		ns
$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low	t_{MS}	0		0		ns
$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		ns
$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low	t_{ESR}	0		0		ns
$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	− 5		− 5		ns
$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high with $\overline{TRG}$ = $\overline{W}$ = low	t_{RWL}	25		30		ns
$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 6. All cycle times assume t_t = 5 ns.

7. When the odd tap is used (tap address can be 0-511, and odd taps are 1,3,5, etc.), the cycle time for SC in serial data out cycle needs to be 50 ns minimum.

8. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].

9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$]

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

		ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		ns
$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low	t_{REH}	15		15		ns
$t_{h(RWM)}$	Write mask, transfer enable hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 9)	t_{AR}	45		45		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 10)	t_{DHR}	45		50		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 11)	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 11)	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 10)	t_{WCR}	50		55		ns
$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 12)	t_{OEH}	25		30		ns
$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	10		10		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	30		35		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 13 and 14)	t_{CWD}	55		65		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Notes 15 and 16)	t_{RCD}	25	75	25	90	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 13)	t_{RWD}	130		155		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 13)	t_{AWD}	85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 11)	t_{CHR}	25		25		ns
$t_{d(CLRL)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 17)	t_{CSR}	10		10		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 17)	t_{RCP}	5		5		ns
$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		35		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		25		30		ns
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	t_{RTH}	90		95		ns

Continued next page.

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
10. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
11. Either $t_{h(RHrd)}$ or $t_{(CHrd)}$ must be satisfied for a read cycle.
12. Output enable controlled write. Output remains in the high-impedance state for the entire cycle.
13. Read-modify-write operation only.
14. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
15. Read cycles only.
16. Maximum value specified only to guarantee $\overline{RAS}$ access time.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

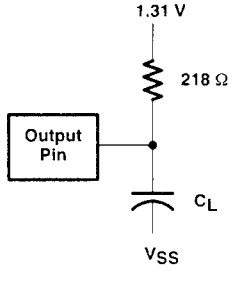
		ALT. SYMBOL	TMS44C250-1 TMS44C250-10		TMS44C250-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)	t_{RSD}	130		135		ns
$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 18)	t_{CSD}	40		45		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 18 and 19)	t_{TSL}	10		15		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 18)	t_{TRD}	−10		−10		ns
$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ low with $\overline{TRG}$ = $\overline{W}$ = low (see Notes 20 and 21)	t_{SRS}	10		10		ns
$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		20		20		ns
$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 21)	t_{SRD}	25		30		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 22)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 22)	t_{TSD}	35		40		ns
$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 23)	t_{SWS}	10		15		ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms
t_t	Transition time	t_T	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 18. Memory to register (read) transfer cycles only.

19. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
20. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to guarantee proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
21. Register to memory (write) transfer cycles reserved only.
22. Memory to register (read) and register to memory (write) transfer cycles only.
23. Serial data-in cycles only.

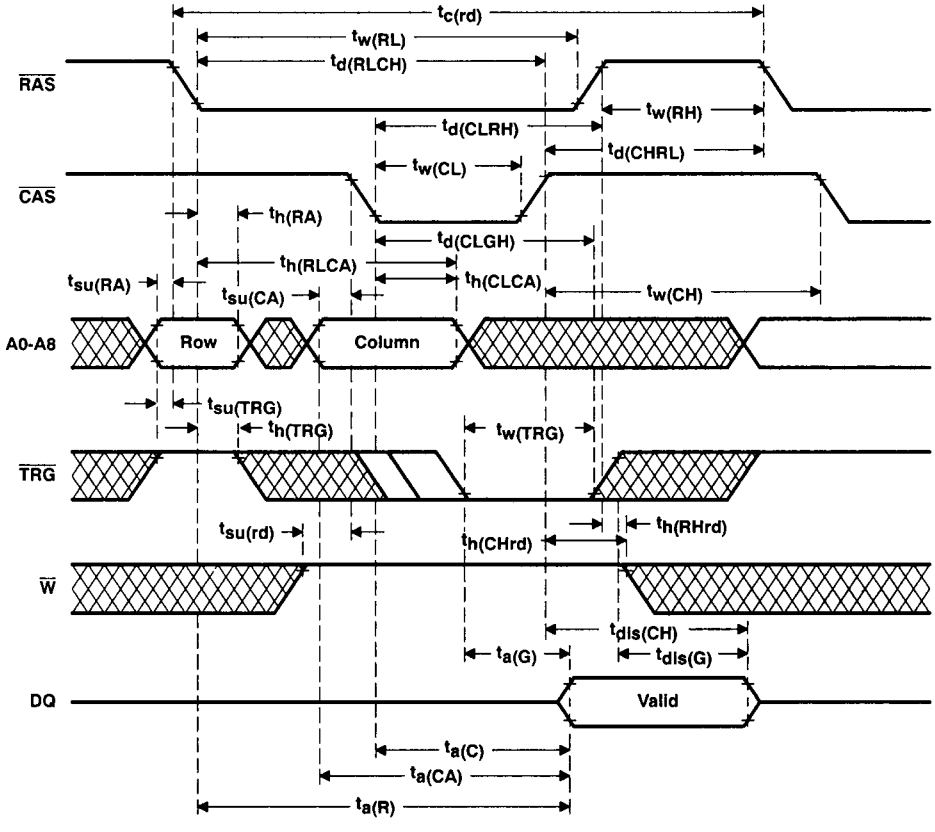
PARAMETER MEASUREMENT INFORMATION



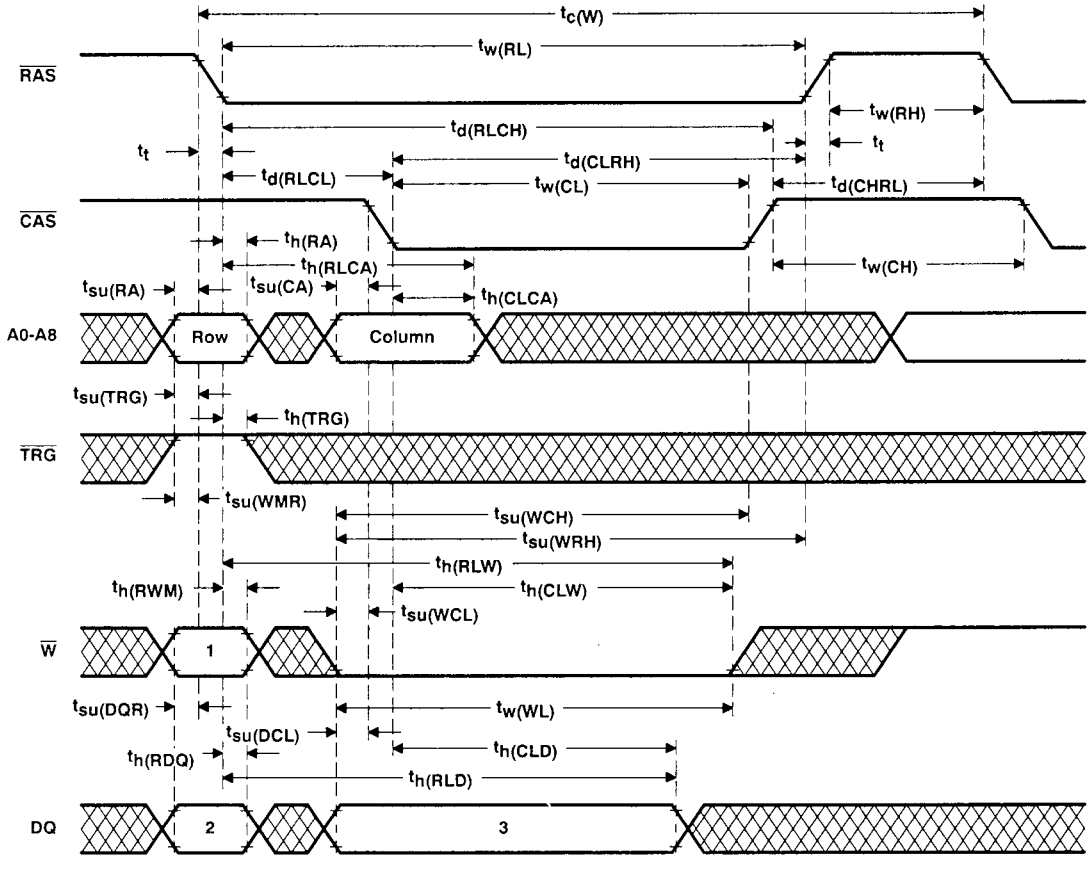
Load Circuit

Figure 2. Load Circuit

read cycle timing

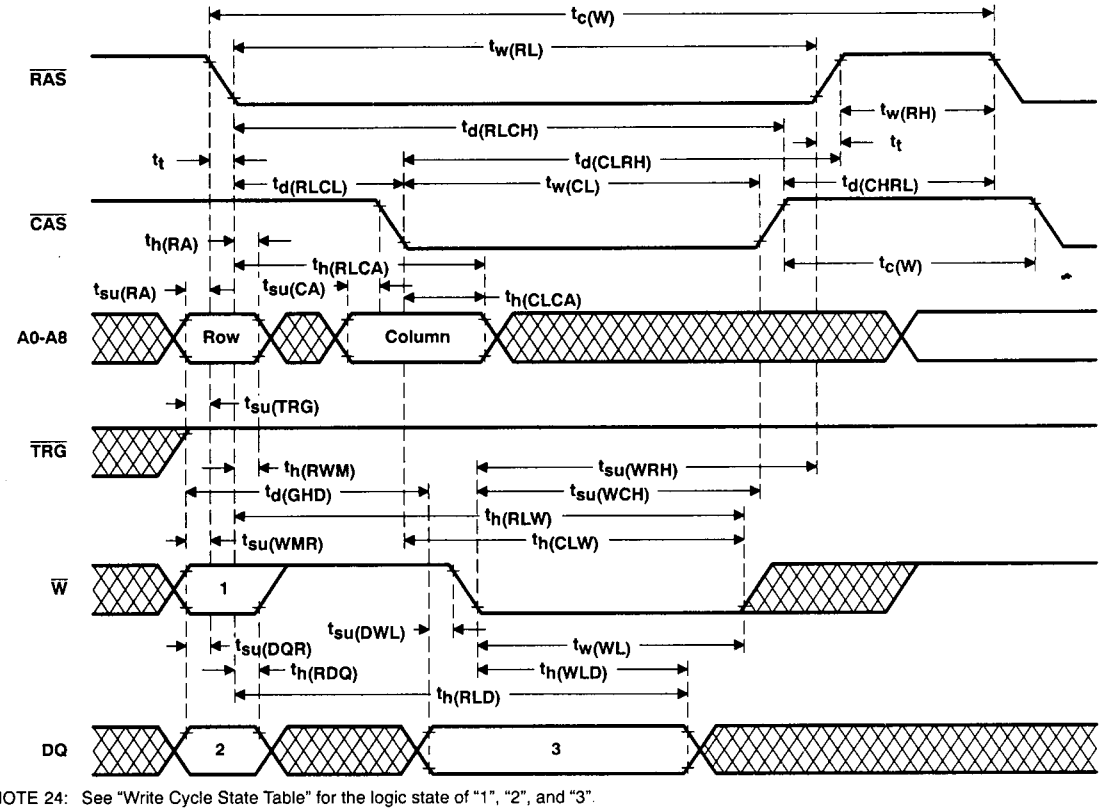


early write cycle timing



NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", and "3".

delayed write cycle timing

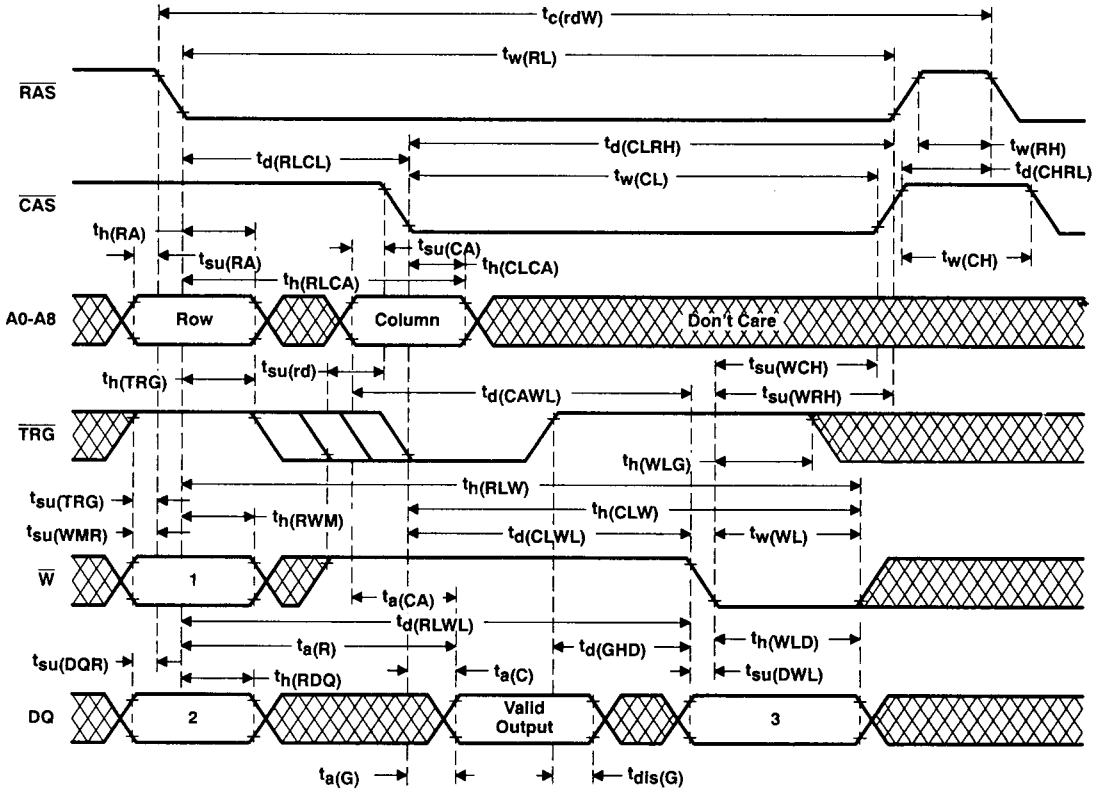


NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", and "3".

write cycle state table

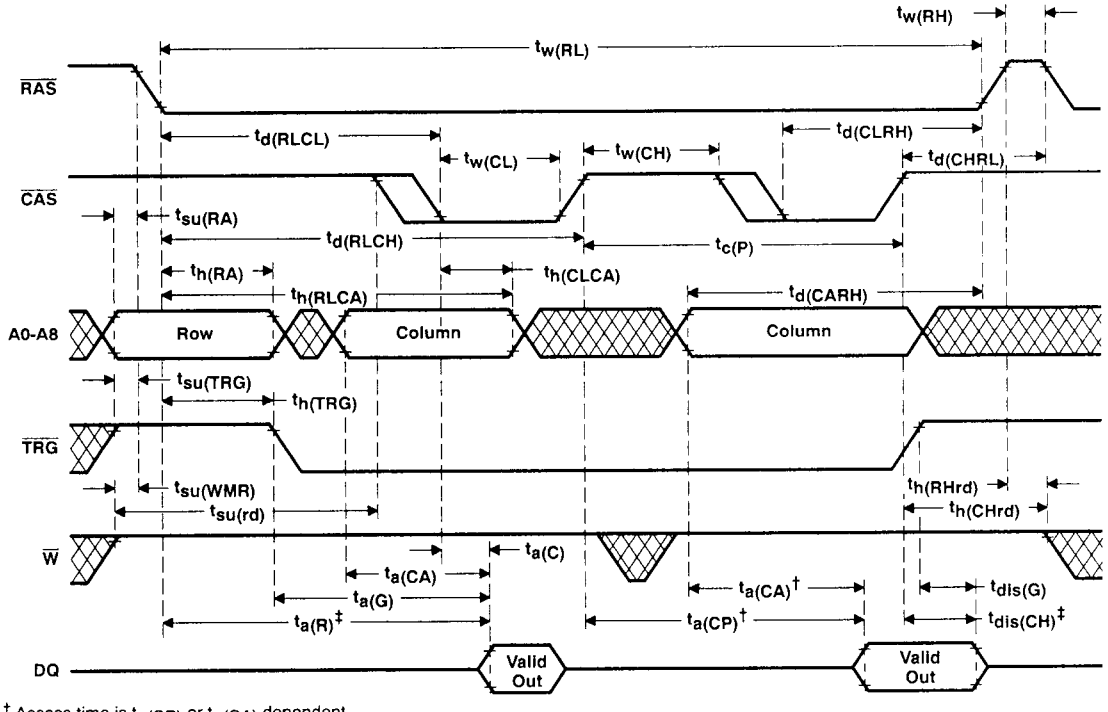
CYCLE	STATE		
	1	2	3
Write mask load/use Write DQs to I/Os	L	Write Mask	Valid Data
Normal early or late Write operation	H	Don't Care	Valid Data

read-write/read-modify-write cycle timing



NOTE 24: See "Write Cycle State Table" for the logic state of "1", "2", and "3". Same logic as delayed write cycle.

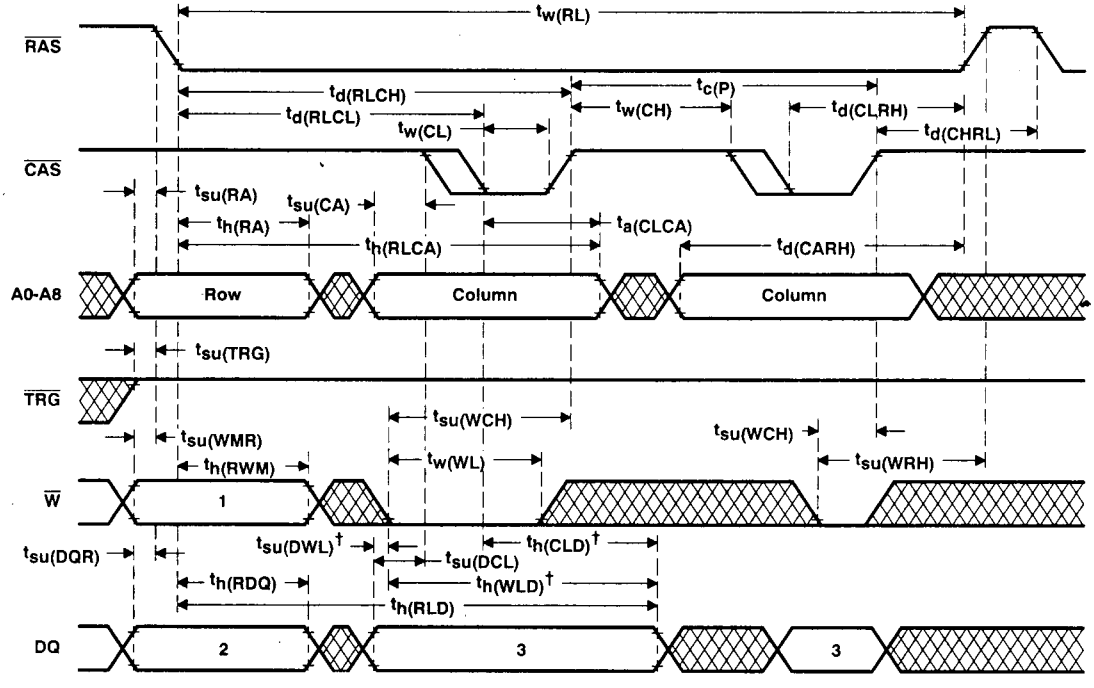
enhanced page-mode read cycle timing



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.

NOTE 25: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

enhanced page mode write cycle timing

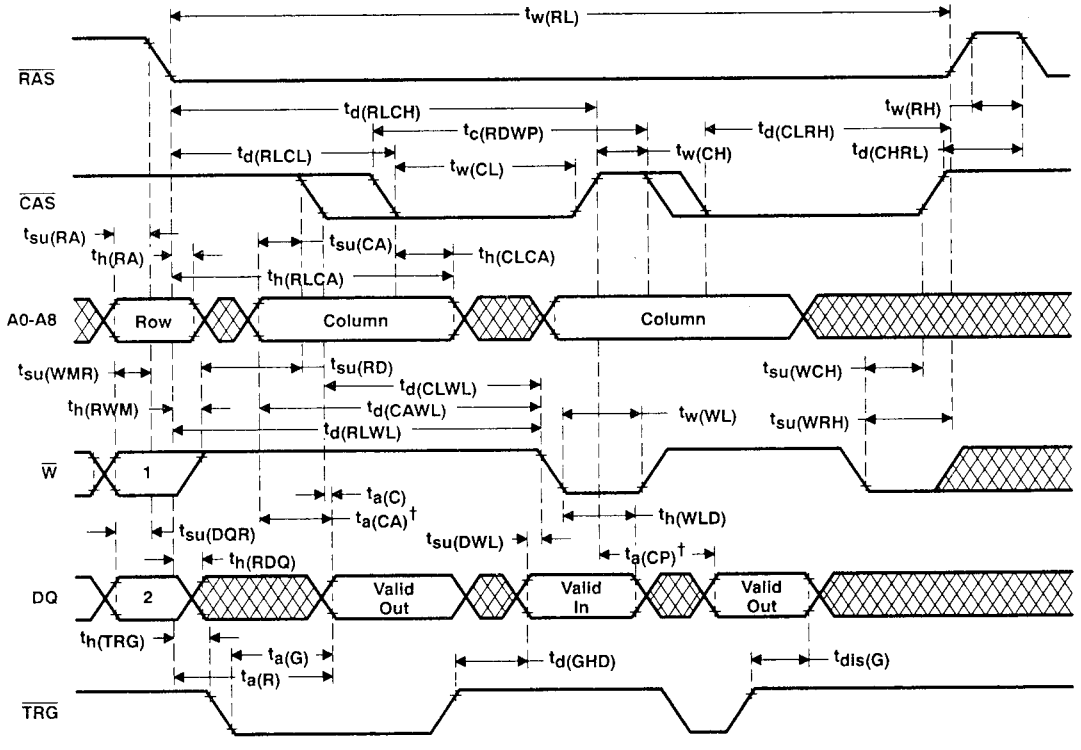


† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", and "3".

26. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to guarantee page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

enhanced page-mode read-modify-write cycle timing

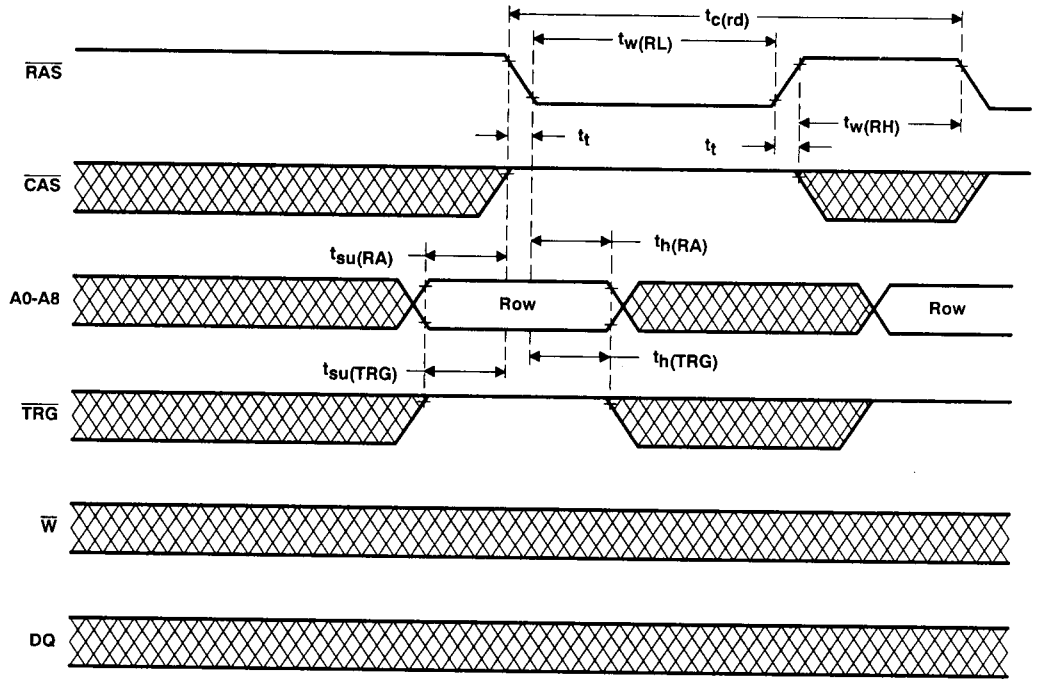


† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

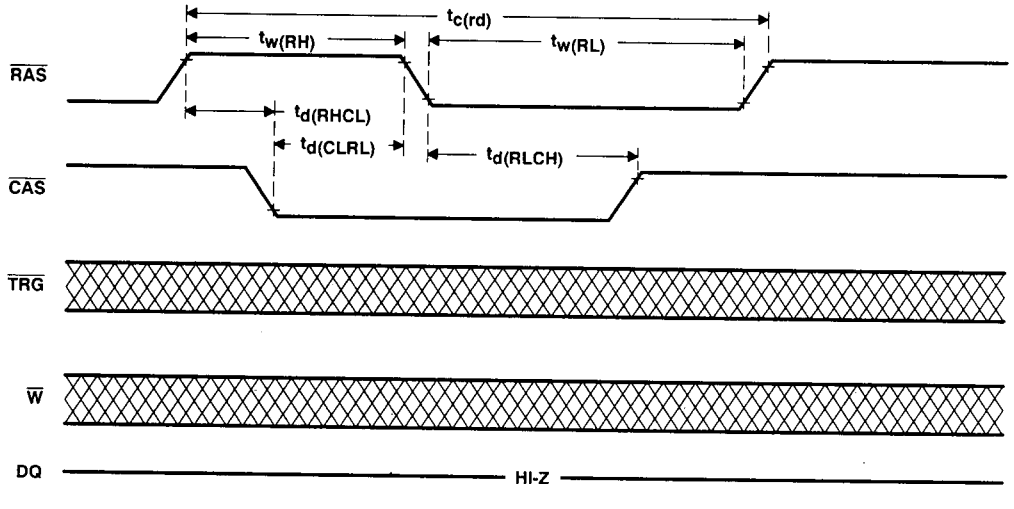
NOTES: 24. See "Write Cycle State Table" for the logic state of "1", "2", and "3".

27. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

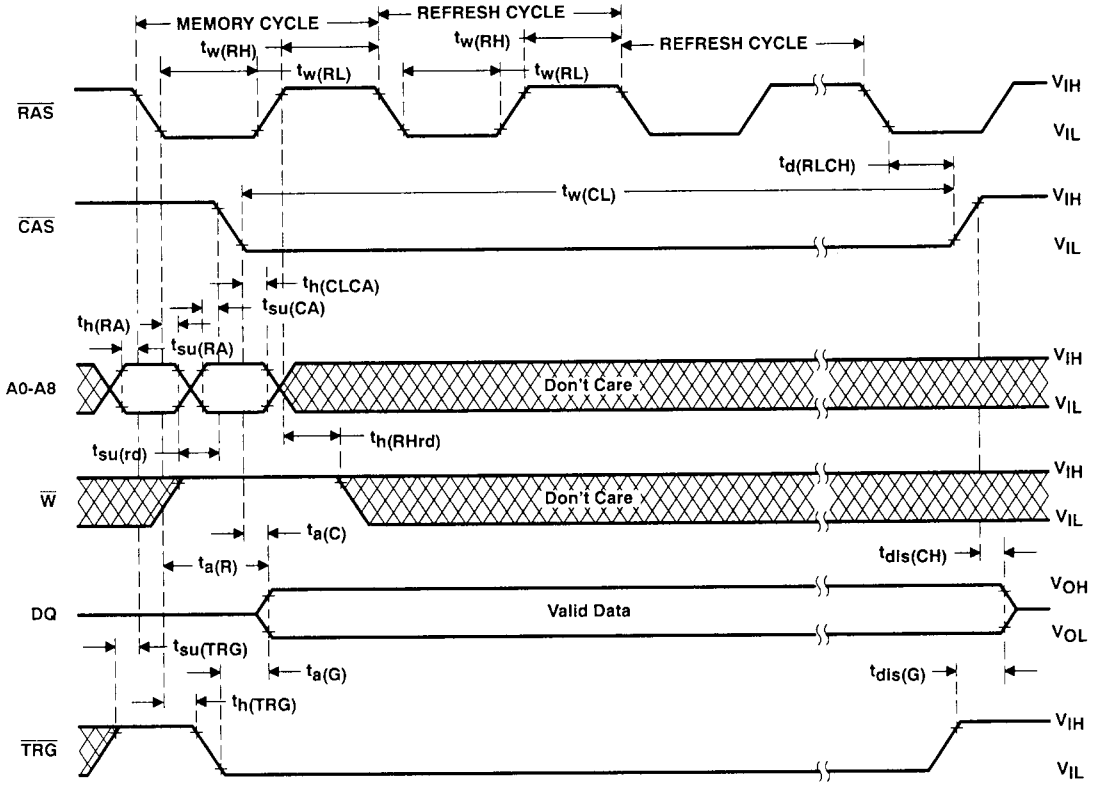
RAS-only refresh timing



CAS-before-RAS refresh

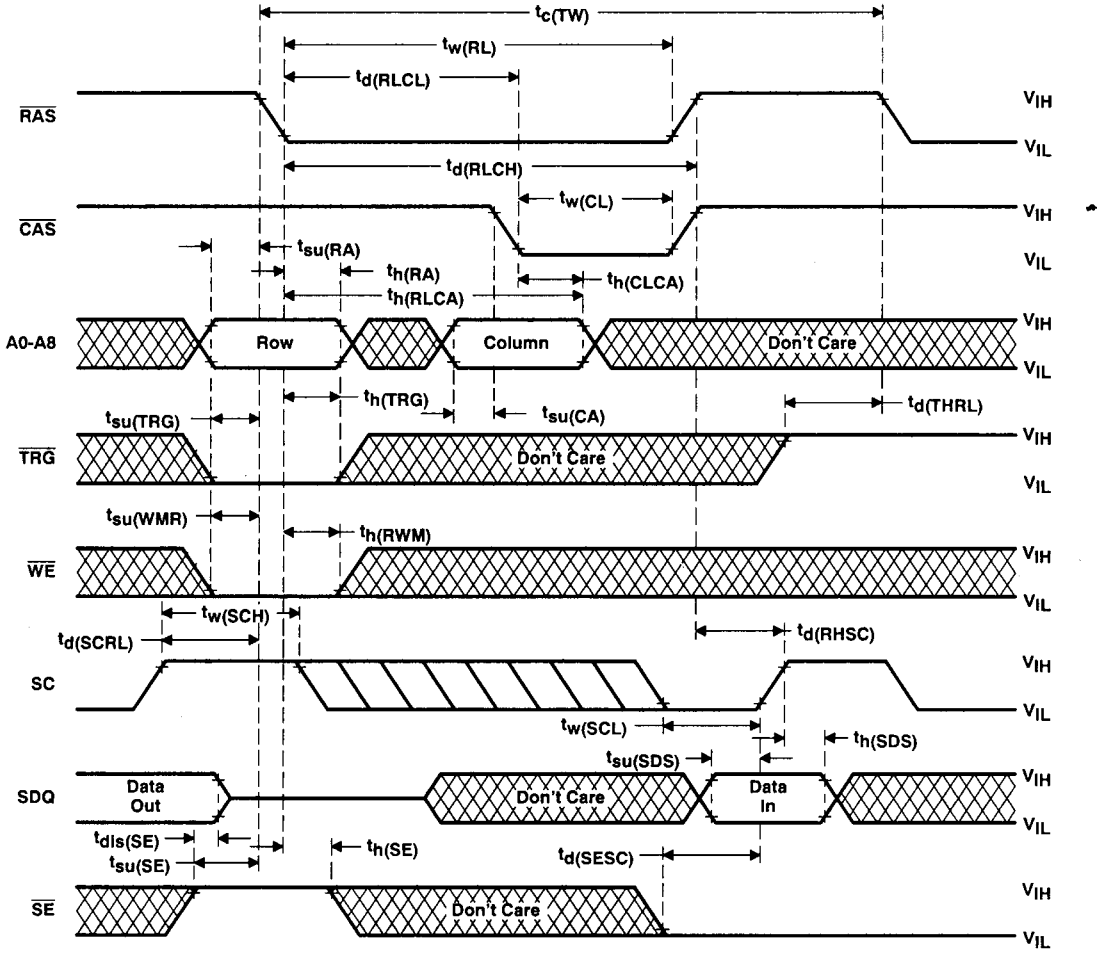


hidden refresh cycle timing



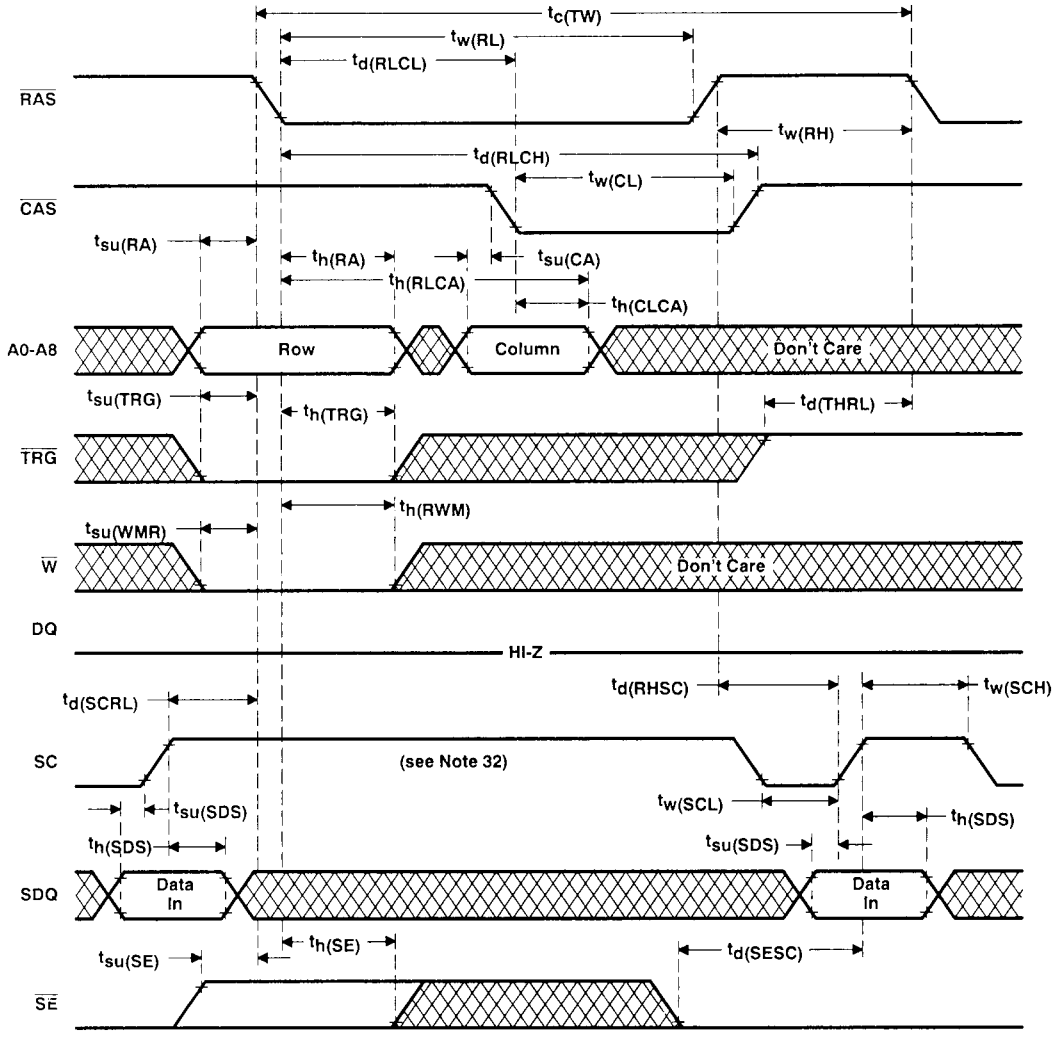
write-mode control pseudo write transfer timing

The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: 28. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
29. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

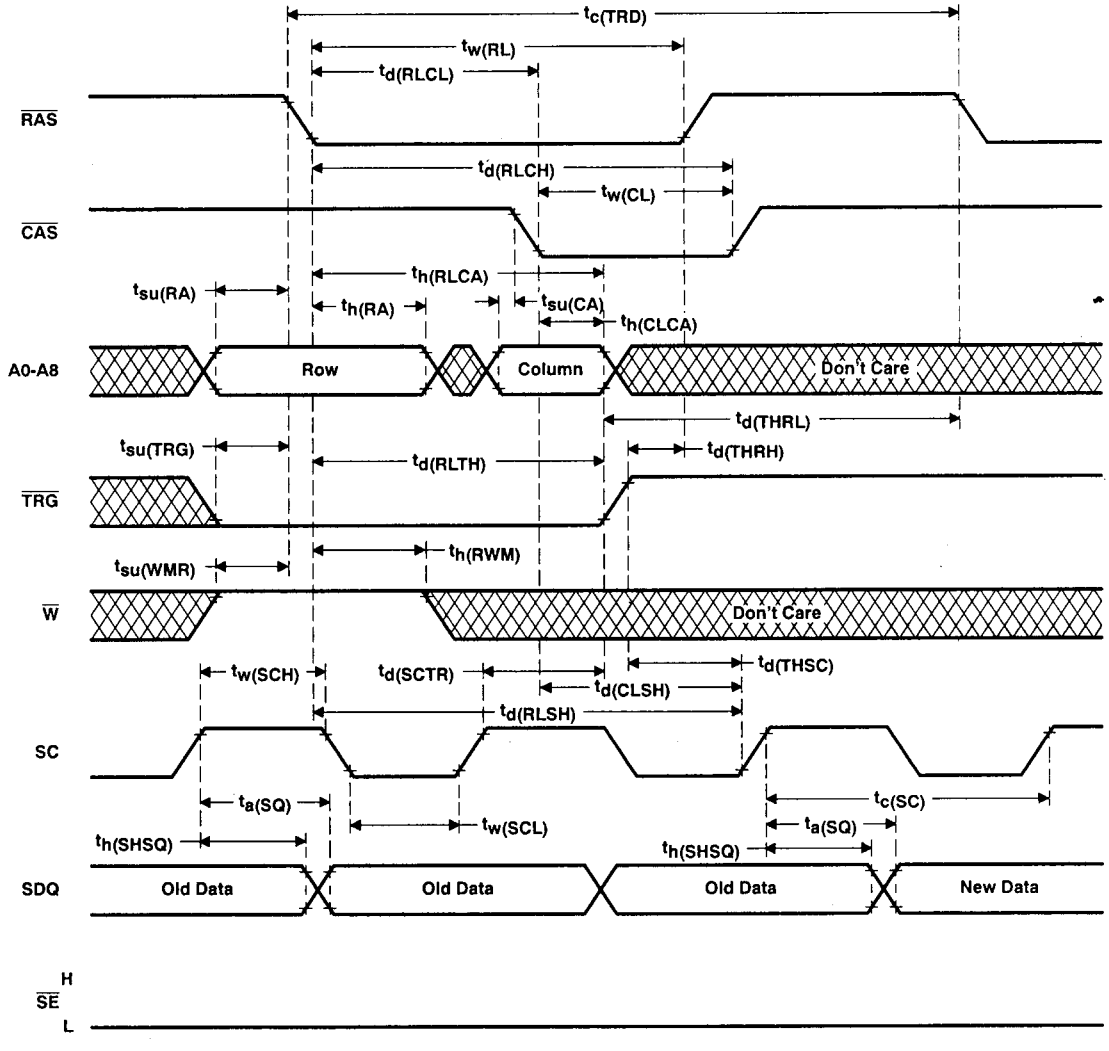
data register to memory timing, serial input enabled



NOTES: 30. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

31. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.
32. SC transitions are not allowed between $\overline{RAS}$ low and $\overline{TRG}$ high.
33. For multiple transfer write operation; a transfer read cycle needs to be done from the same row after the first transfer write is carried out, then do multiple transfer write for subsequent rows.

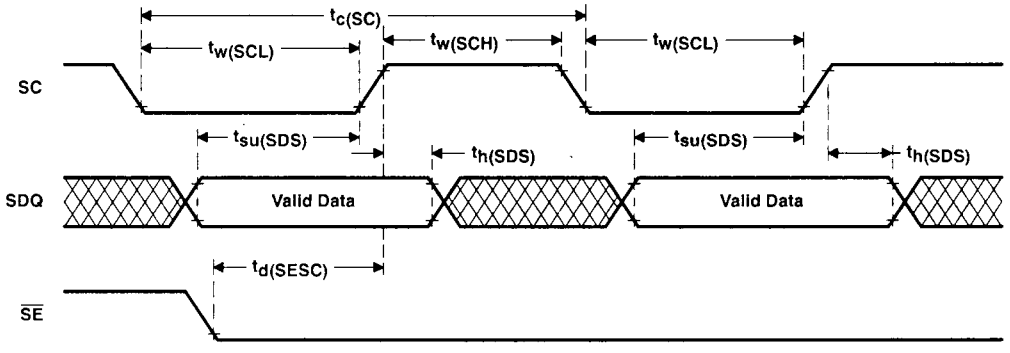
memory to data register transfer timing



NOTES: 34. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

35. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

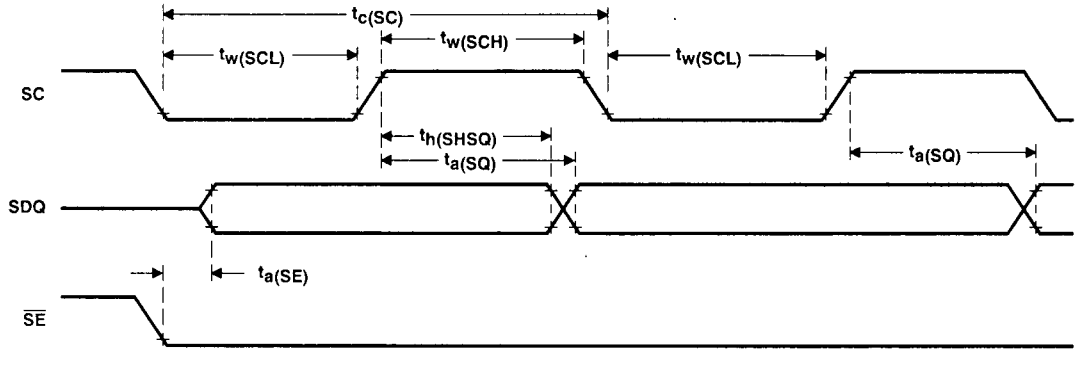
serial data-in timing



The serial data-in cycle (SD) is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control, or pseudo-transfer, cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing of data will take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.

serial data-out timing



NOTES: 7. When the odd tap is used (tap addresses can be 0-511, and odd taps are 1,3,5 ... etc.), the cycle time for SC in serial data out cycle needs to be 50 ns minimum.

36. While reading data through the serial data register, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register to memory or memory to register data transfer operation.

The serial data-out cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.