1 INTRODUCTION

1.1 SUMMARY

The Rockwell R96MFX, R96EFX, R96DFX, and R96VFX MONOFAX® modems are synchronous 9600 bits per second (bps) half-duplex modems. Each modem is housed in a single VLSI device package. In this document, the word "modem" refers to each of these modems unless otherwise noted.

The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem is designed for use in Group 3 facsimile machines and satisfies the requirements specified in CCITT recommendations V.29, V.27 ter, V.21 channel 2 (FSK), and T.4, and meets the binary signaling requirements of T.30.

The modem can operate at 9600, 7200, 4800, 2400, or 300 bps depending upon the selected configuration.

The modem features three programmable tone detectors.

The voice mode allows the host computer to efficiently transmit and receive audio signals and messages.

The R96MFX and R96EFX also support CCITT T.3 Group 2 with concurrent programmable tone detection.

The R96EFX, R96DFX, and R96VFX support V.27 ter short train. The R96VFX also supports V.29 short train.

The R96EFX, R96DFX, and R96VFX can perform HDLC framing according to T.30 at 9600, 7200, 4800, 2400, or 300 bps.

The R96VFX incorporates an enhanced Adaptive Differential Pulse Code Modulation (ADPCM) voice coder and decoder (codec). The full-duplex codec compresses and decompresses voice signals to allow efficient digital storage of voice messages. The codec operates at 32k, 24k, or 16k bits per second with the default 8 kHz programmable sample rate. Optional coder silence detection/deletion and decoder silence interpolation is included to achieve greater compression rates.

The R96DFX and R96VFX modems include a programmable DTMF receiver and three programmable tone detectors which operate concurrently with the FSK receiver or ADPCM receiver (R96VFX).

The R96VFX modem includes a programmable digital equalizer and a FSK flag pattern (7E) detector to facilitate FSK detection during high speed reception.

The modem is available in either a 68-pin plastic leaded chip carrier (PLCC) package (Figure 1-1) or a 64-pin quad in-line package (QUIP). The general modem interface is shown in Figure 1-2.

1.2 FEATURES

Features supported by all modems

- Group 3 facsimile transmission/reception
  - CCITT V.29, V.27 ter, T.30, V.21 Channel 2 (FSK), T.4
- Voice mode transmission/reception
- Half-duplex (2-wire)
- Maximum transmit level: 0 dBm programmable to –15 dBm
- Receive dynamic range: 0 dBm to –43 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable interface memory interrupt
- Diagnostic capability
  - Allows telephone line quality monitoring
- Equalization
  - Automatic adaptive
  - Selectable compromise cable
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - CCITT V.24 (EIA-232-D compatible) interface
- TTL and CMOS compatible
- Low power consumption:
  - 370 mW (typical) (except R96VFX)
  - 400 mW (typical) (R96VFX)
- Single package: 68-pin PLCC or 64-pin QUIP

Features supported only by R96MFX and R96EFX

- CCITT T.3 Group 2 facsimile transmission/reception

Features supported only by R96EFX, R96DFX, and R96VFX

- CCITT V.27 ter short train option
- HDLC framing at all speeds

Features supported only by R96DFX and R96VFX

- Concurrent DTMF reception, FSK, and tone detection

Features supported only by R96VFX

- Enhanced ADPCM voice codec
  - Full duplex
  - 2, 3, or 4 bits per sample
  - Programmable sample rate
  - Coder silence detection/deletion
  - Decoder silence interpolation
  - Concurrent DTMF reception, FSK flag pattern (7E) detection, and tone reception
- FSK flag pattern (7E) detection during high speed reception
- Programmable digital equalizer
- V.29 short train using a Rockwell algorithm

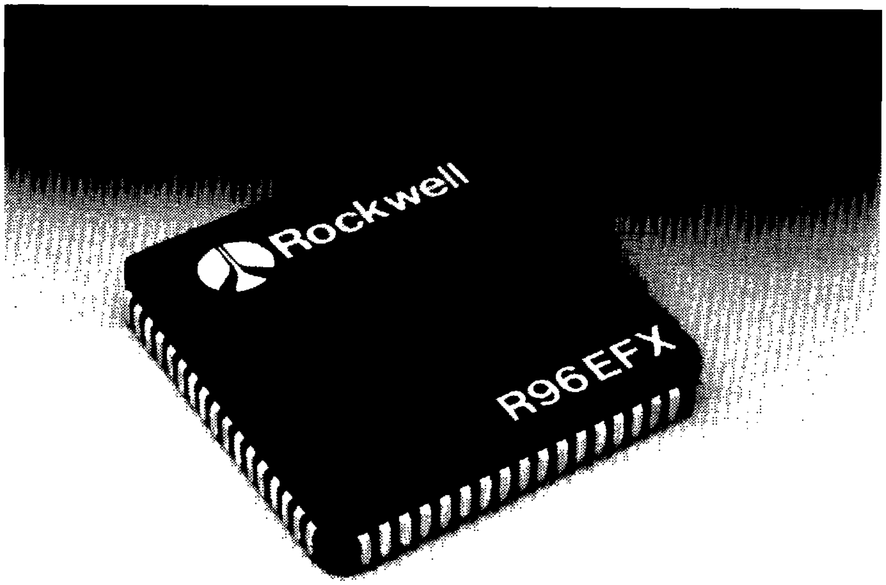


Figure 1-1. 9600 bps MONOFAX Modem

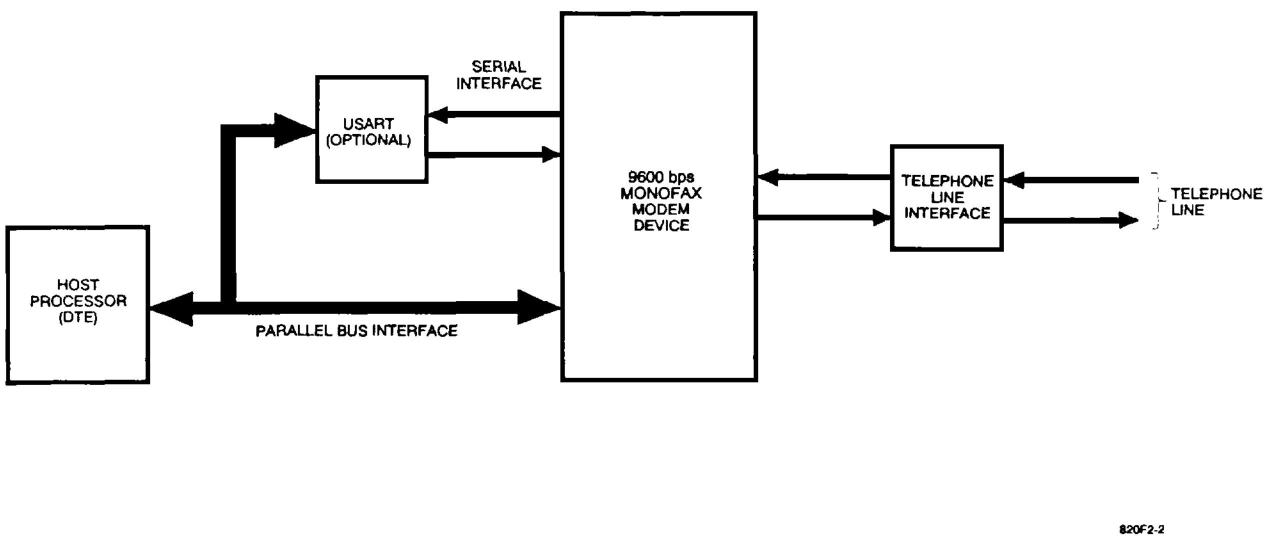


Figure 1-2. 9600 bps MONOFAX Modem General Interface

1.3 TECHNICAL SPECIFICATIONS

Configurations, Signaling Rates and Data Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1-1.

Tone Generation

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer (see Section 7).

Data Encoding

The data encoding conforms to CCITT recommendations V.29, V.27 ter, V.21 Channel 2, and T.3.

Adaptive Equalizer

An adaptive equalizer in V.29 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

Compromise Cable Equalizers

Compromise equalization can improve performance when operating over low quality lines. Equalizer characteristics for cable lengths of 0, 1.8, 3.6, or 7.2 km are selectable by two hardware input pins (see CABLE1 and CABLE2 signal description in Table 2-5). The selected filter operates in both transmit and receive paths.

Programmable Digital Equalizer (R96VFX)

A programmable digital equalizer is provided in the high speed receiver path. It defaults to a Japanese two link delay response.

Transmitted Data Spectrum

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The transmit spectrum characteristics assume that the cable equalizers are disabled.

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range are below –55.0 dBm.

Turn-on Sequence

Transmitter turn-on sequence times are shown in Table 1-2.

Turn-off Sequence

For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy.

Table 1-2. Turn-On Sequences

Configuration	RTS On to CTS On: Echo Protector Tone Disabled	RTS On to CTS On: Echo Protector Tone Enabled
V.29 (All Speeds)	253 ms	441 ms
V.29 Short Train (All Speeds)[3]	75 ms	283 ms
V.27 ter 4800 bps Long Train	708 ms	915 ms
V.27 ter 4800 bps Short Train[1]	50 ms	257 ms
V.27 ter 2400 bps Long Train	943 ms	1150 ms
V.27 ter 2400 bps Short Train[1]	67 ms	274 ms
V.21 channel 2 300 bps	≤ 14 ms	≤ 14 ms
Group 2[2]	≤ 400 μs	≤ 400 μs

Notes:
1. R96EFX, R96DFX, and R96VFX only.
2. R96MFX and R96EFX only.
3. R96VFX only.

Table 1-1. Configurations and Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol	Constellation Points
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 channel 2 300	FSK	1650,1850	300	300	1	–
T.3 (Group 2)[2]	VSAMPM	2100	–	–	–	–

Notes:
1. Modulation legend:
   - QAM Quadrature Amplitude Modulation
   - DPSK Differential Phase Shift Keying
   - FSK Frequency Shift Keying
   - VSAMPM Vestigial Sideband Amplitude Modulation - Phase Modulation
2. R96MFX and R96EFX only.

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy.

In V.21 channel 2, the transmitter turns off within 7 ms after RTS goes off.

In Group 2 (R96MFX and R96EFX only), the transmitter turns off within 200 μs after RTS goes false.

When operating in parallel data mode, the turn-off sequence may be extended by 8 bit times.

When HDLC is selected (except R96MFX), the turn-off sequence may be extended by more than 8 bit times.

Transmit Level

The transmitter output level is programmable in the DSP RAM from 0 dBm to −15.0 dBm and is accurate to ± 1.0 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.29 or V.27 ter depending on the configuration.

Receive Dynamic Range

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to −43 dBm measured at the Receiver Analog (RXA) input. An external input buffer and filter must be supplied between RXA and RXIN.

The default values of the programmable Received Line Signal Detector (RLSD) turn-on and turn-off threshold levels are −43 dBm and −48 dBm, respectively.

The RLSD threshold levels can be programmed over the following range:

Turn on: −10 dBm to −47 dBm
Turn off: −10 dBm to −52 dBm

Receiver Timing

The timing recovery circuit can track a ± 0.01% frequency error in the associated transmit timing source.

Carrier Recovery

The carrier recovery circuit can track a ± 7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever RLSD is off.

Tone Detectors

Tone detectors 1 and 2 operate in all non-high speed receive modes. Tone detector 3 operates in all receive modes. The tone detectors can also operate as one 12th order filter (see 12TH bit in Table 3-1).

The filter coefficients of each filter are host programmable in RAM (See Section 6).

General Specifications

The modem power and environmental requirements are shown in Tables 1-3 and 1-4, respectively.

Table 1-3. Power Requirements

Voltage	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+5 VDC ±5%		
Except R96VFX	60 mA	≤ 64 mA
R96VFX	66 mA	≤ 70 mA
− 5 VDC ±5%	14 mA	≤ 16 mA

Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 μV peak.

Table 1-4. Environmental Requirements

Parameter	Specification
Temperature	
Operating	0°C +70°C (32°F to 158°F)
Storage	−55°C to +125°C (−67°F to 257°F) (Stored in a suitable anti-static container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

2 HARDWARE INTERFACE

2.1 PIN ASSIGNMENTS

The modem pin assignments are shown in Figure 2-1. The pin assignments are listed by pin number in Table 2-1.

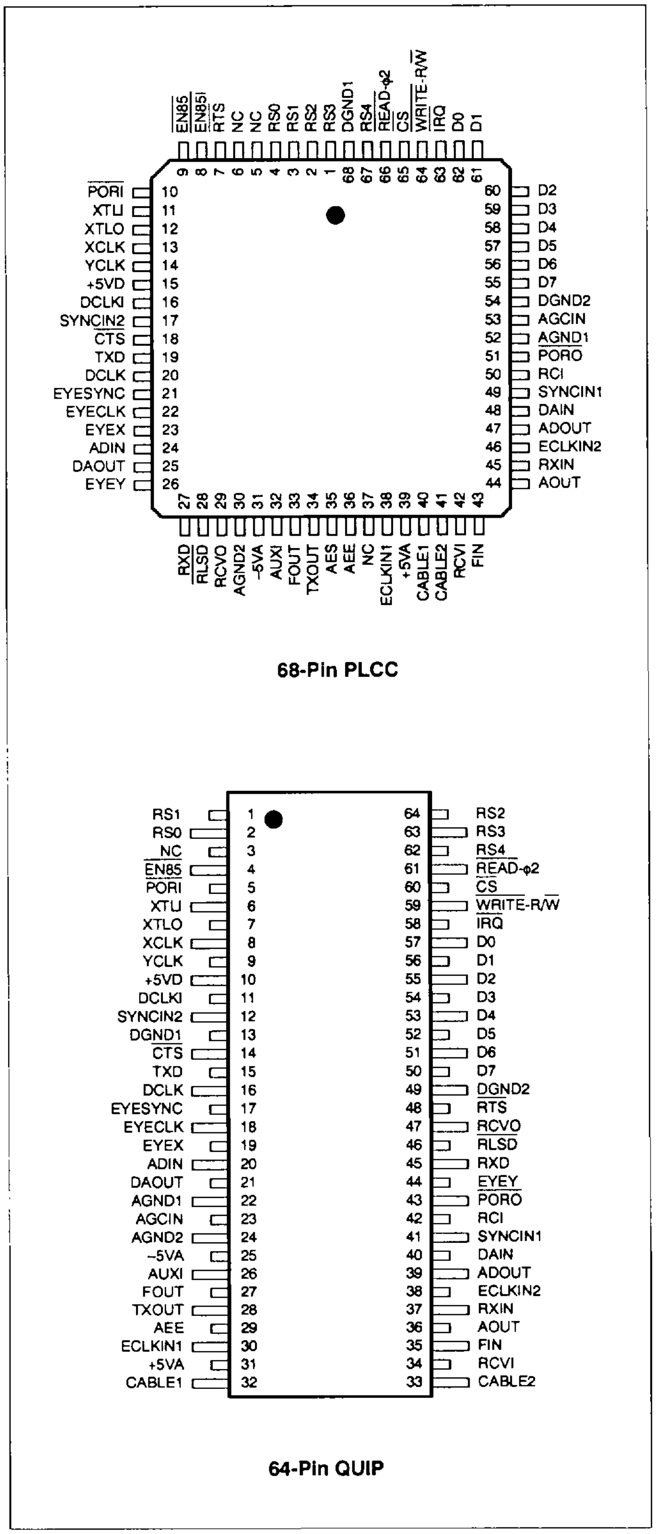


Figure 2-1. Modem Device Pin Assignments

Table 2-1. Modem Device Pin Assignments

PLCC Pin	QUIP Pin	Signal Name	I/O Type
1	63	RS3	IA
2	64	RS2	IA
3	1	RS1	IA
4	2	RS0	IA
5	–	NC	NC
6	3	NC	NC
7	48	RTS	IA
8	–	EN85I	R
9	4	EN85	R
10	5	PORI	ID
11	6	XTLI	R
12	7	XTLO	R
13	8	XCLK	OD
14	9	YCLK	OD
15	10	+5VD	PWR
16	11	DCLKI	R
17	12	SYNCIN2	R
18	14	CTS	OA
19	15	TXD	IA
20	16	DCLK	OA
21	17	EYESYNC	OA
22	18	EYECLK	OA
23	19	EYEX	OA
24	20	ADIN	R
25	21	DAOUT	R
26	44	EYEY	OA
27	45	RXD	OA
28	46	RLSD	OA
29	47	RCVO	R
30	24	AGND2	GND
31	25	–5VA	PWR
32	26	AUXI	AC
33	27	FOUT	R
34	28	TXOUT	AA
35	-	AES	R
36	29	AEE	R
37	-	NC	NC
38	30	ECLKIN1	R
39	31	+5VA	PWR
40	32	CABLE1	IB
41	33	CABLE2	IB
42	34	RCVI	R
43	35	FIN	R
44	36	AOUT	R
45	37	RXIN	AB
46	38	ECLKIN2	R
47	39	ADOUT	R
48	40	DAIN	R
49	41	SYNCIN1	R
50	42	RCI	R
51	43	PORO	OE
52	22	AGND1	GND
53	23	AGCIN	R
54	49	DGND2	GND
55	50	D7	IA/OB
56	51	D6	IA/OB
57	52	D5	IA/OB
58	53	D4	IA/OB
59	54	D3	IA/OB
60	55	D2	IA/OB
61	56	D1	IA/OB
62	57	D0	IA/OB
63	58	IRQ	OC
64	59	WRITE-R/W	IA
65	60	CS	IA
66	61	READ-φ2	IA
67	62	RS4	IA
68	13	DGND1	GND

Notes: 1. NC = No connection, leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 2-3;
Analog signals: see Table 2-4.
3. R = Required overhead connection; no connection to host equipment.

2.2 HARDWARE INTERFACE SIGNALS

The functional interconnect diagram (Figure 2-2) shows the typical modem connection in a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or −12 VDC for EIA-232-D) is called active low and is represented by a small circle at the signal point. Active low signals are overscored (e.g., POR).

Edge-triggered clocks are indicated by a small triangle (e.g., DCLK).

Open-collector (open-source or open-drain) outputs are denoted by small half circle (e.g., signal IRQ).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The hardware interconnect signals shown in Figure 2-2 are listed by functional group in Table 2-2. The digital and analog signal interface characteristics are defined in Tables 2-3 and 2-4, respectively. The hardware interface signals are defined in Table 2-5.

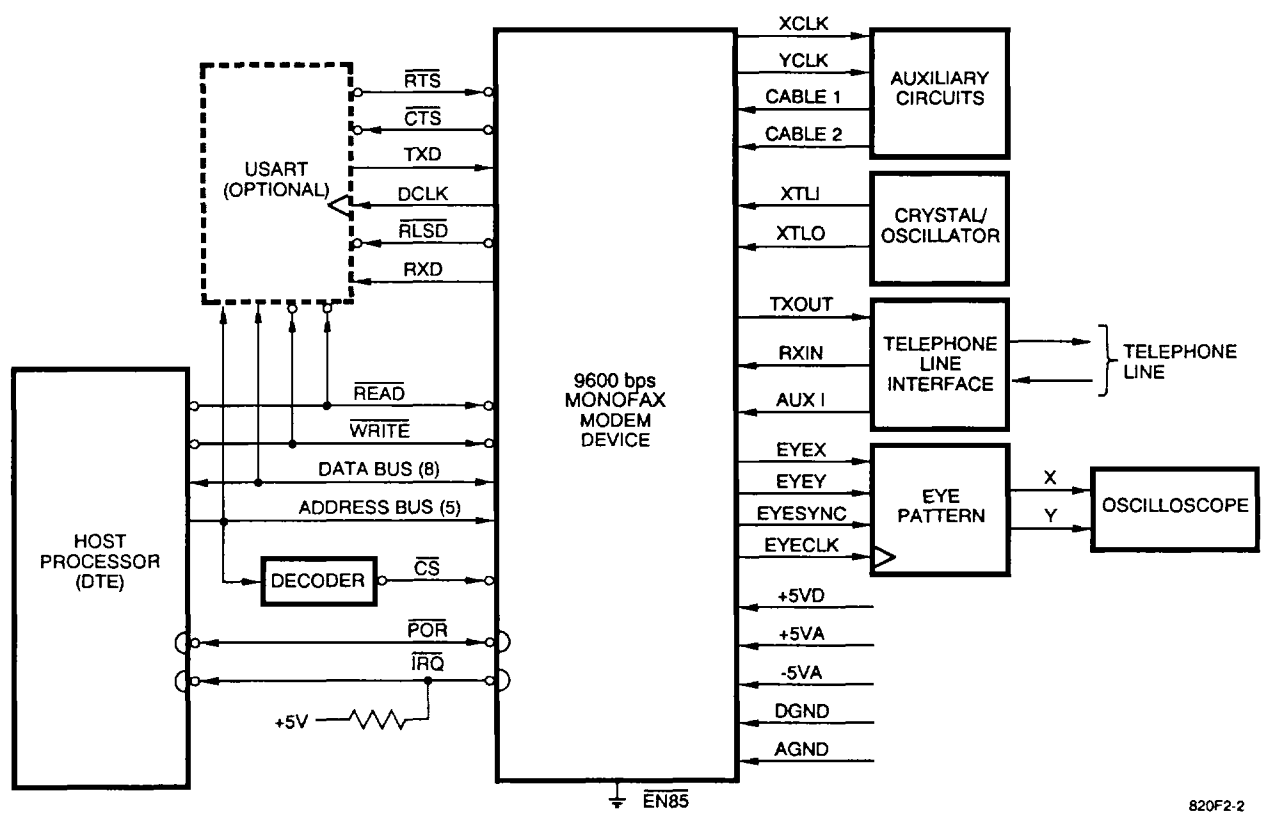


Figure 2-2. Modem Functional Interconnect Diagram

Table 2-2. Modem Hardware Interface Signals

Name	Type[1]	Description
Overhead Signals		
XTLI	R	Connect to Crystal/Oscillator
XTLO	R	Connect to Crystal/Oscillator
PORO	OE	Power-On-Reset Output
PORI	ID	Power-On-Reset Input
+5VD	PWR	Connect to Digital +5V Power
+5VA	PWR	Connect to Analog +5V Power
–5VA	PWR	Connect to Analog –5V Power
DGND1	GND	Connect to Digital Ground
DGND2	GND	Connect to Digital Ground
AGND1	GND	Connect to Analog Ground
AGND2	GND	Connect to Analog Ground
Microprocessor Bus Interface		
D7	IA/OB	Data Bus Line 7
D6	IA/OB	Data Bus Line 6
D5	IA/OB	Data Bus Line 5
D4	IA/OB	Data Bus Line 4
D3	IA/OB	Data Bus Line 3
D2	IA/OB	Data Bus Line 2
D1	IA/OB	Data Bus Line 1
D0	IA/OB	Data Bus Line 0
RS4	IA	Register Select 4
RS3	IA	Register Select 3
RS2	IA	Register Select 2
RS1	IA	Register Select 1
RS0	IA	Register Select 0
CS	IA	Chip Select
READ-ϕ2	IA	Read Enable (808X), ϕ2 Clock (65XX)
WRITE-R/W	IA	Write Enable (808X), R/W (65XX)
IRQ	OC	Interrupt Request
V.24 Serial Interface		
TXD	IA	Transmit Data
RXD	OA	Received Data
RTS	IA	Request to Send
CTS	OA	Clear to Send
RLSD	OA	Received Line Signal Detected
DCLK	OA	Transmit and Receive Data Clock
Auxiliary Signals		
EN85	R	Enable 8085 Bus
CABLE1	IB	Cable Select 1
CABLE2	IB	Cable Select 2
XCLK	OD	12 MHz (except R96VFX) or 13.2 MHz (R96VFX) output
YCLK	OD	6 MHz (except R96VFX) or 6.6 MHz (R96VFX) output

Table 2-2. Modem Hardware Interface Signals (Cont'd)

Name	Type[1]	Description
Analog Signals		
TXOUT	AA	Connect to Smoothing Filter Input
RXIN	AB	Connect to Anti-aliasing Filter Output
AUXI	AC	Auxiliary Analog Input
Eye Diagnostic Interface		
EYEX	OA	Serial Eye Pattern X Output
EYEY	OA	Serial Eye Pattern Y Output
EYECLK	OA	Serial Eye Pattern Clock
EYESYNC	OA	Serial Eye Pattern Strobe
Modem Interconnect		
DCLKI	R	Connect to DCLK
ECLKIN1	R	Connect to EYECLK
ECLKIN2	R	Connect to EYECLK
SYNCIN1	R	Connect to EYESYNC
SYNCIN2	R	Connect to EYESYNC
RCVI	R	Connect to RCVO
RCVO	R	Mode Select Output
ADIN	R	Connect to ADOUT
ADOUT	R	ADC Output
DAIN	R	Connect to DAOUT
DAOUT	R	DAC/AGC Output
EN85I	R	Connect to EN85
AEE	R	Connect to Analog Ground
AES	R	Connect to Analog Ground4
AGCIN	R	AGC Input
AOUT	R	Smoothing Filter Output
FIN	R	Connect to FOUT
FOUT	R	Smoothing Filter Output
RCI	R	RC Junction for POR Time Constant

Notes:

1. Digital signals are described in Table 2-3. Analog signals are described in Table 2-4.
2. R = Required overhead connection; no connection to host equipment.
3. Unused inputs tied to +5V or ground require individual 10K Ω series resistors.
4. PLCC only.

Table 2-3. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.0	–	V_{CC}		
Type ID		0.8(V_{CC})	–	V_{CC}		
Input High Current	I_{IH}	–	–	40	µA	V_{CC} = 5.25 V, V_{IN} = 5.25 V
Type IB						
Input Low Voltage	V_{IL}	–0.3	–	0.8	Vdc	
Input Low Current	I_{IL}	–	–	–400	µA	V_{CC} = 5.25 V
Type IB						
Input Leakage Current	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5 V, V_{CC} = 5.25 V
Types IA and ID						
Output High Voltage	V_{OH}				Vdc	
Types OA and OB		3.5	–	–		I_{LOAD} = – 100 µA
Type OE		2.4	–	–		I_{LOAD} = –40 µA
Output High Current	I_{OH}	–	–	–0.1	mA	
Type OD						
Output Low Voltage	V_{OL}				Vdc	
Types OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OE		–		0.4		I_{LOAD} = 0.4 mA
Output Low Current	I_{OL}	–	–	100	µA	
Type OD						
Output Leakage Current	I_{LO}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID		–	5	–		
Type IB		–	20	–		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC		–	100	–		
Type OD		–	50	–		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC and OE						Open drain
Type OD						Clock
Power Dissipation	P_D				mW	V_{CC} = 5.0 V @ 25°C for P_D typ.
Except R96VFX		–	370	400		V_{CC} = 5.25 V @ 0°C for P_D max.
R96VFX		–	400	430		

Note: Loads on XCLK and YCLK outputs must be balanced within 20%.

Table 2-4. Analog Interface Characteristics

Name	Type	Characteristic
TXOUT	AA	Maximum output: ±3.03 volts Minimum load: 10K Ω Smoothing filter transfer function: 28735.63/(s + 11547.34)
RXIN	AB	Input impedance: > 1M Ω Anti-aliasing filter transfer function: 21551.72/(s + 11547.34)
AUXI	AC	Maximum input frequency: 4800 Hz Input Impedance: > 1M Ω Gain to TXOUT: 0 dBm ±1 dB

Table 2-5. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	I O	**Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a 24.00014 MHz (except R96VFX) or 26.39998 MHz (R96VFX) crystal and two capacitors, or a square wave generator/sine wave oscillator (R96MFX and R96EFX only). (See Figures 10-1 and 10-2.)
$\overline{\text{PORI}}$ PORO	ID OE	**Power-On-Reset Input.** **Power-On-Reset Output.** The $\overline{\text{PORI}}$ and $\overline{\text{PORO}}$ pins should be connected together to form a bidirectional $\overline{\text{POR}}$ signal. When power is applied to the modem, the modem pulses ($\overline{\text{POR}}$) within 350 ms. The modem is ready to use 15 ms after the low-to-high transition of $\overline{\text{POR}}$. The POR sequence is reinitiated any time the + 5V supply drops below + 3.5V for more than 15 ms, or an external device drives $\overline{\text{POR}}$ low for at least 3 µs. POR is not pulsed low by the modem when the POR sequence is initiated externally. The POR sequence initializes the modem interface memory (Table 3-1) to default values.
+5VD	PWR	**+ 5V Digital Supply.** +5VD must be connected to +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5VA must be connected to +5V ± 5%.
–5VA	PWR	**–5V Analog Supply.** –5VA must be connected to –5V ± 5%.
DGND1, DGND2	GND	**Digital Ground.** DGND1 and DGND2 must be connected to digital ground.
AGND1, AGND2	GND	**Analog Ground.** AGND1 and AGND2 must be connected to analog ground.
		MICROPROCESSOR BUS INTERFACE Address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. The read/write cycle timing waveforms are illustrated in Figure 2-3 and the timing requirements are shown in Table 2-6.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable (READ-ϕ2) and Write Enable ($\overline{\text{WRITE-R/W}}$) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when $\overline{\text{CS}}$ is low. These lines are typically connected to address lines A0-A4. When selected by $\overline{\text{CS}}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).

Table 2-5. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{CS}$	IA	**Chip Select.** The active low $\overline{CS}$ input selects and enables the modem DSP for parallel data transfer between the modem and the host over the microprocessor bus. The RS0-RS4 input lines are typically connected to the host bus five least significant address lines (A0-A4), and the CS input line is typically connected to the next significant address line (A5) through a decoder.
$\overline{READ}$–φ2	IA	**Read Enable–φ2.**
$\overline{WRITE}$–R/$\overline{W}$	IA	**Write Enable–R/$\overline{W}$.** When $\overline{EN85}$ is low (8085 bus selected), reading or writing is controlled by the host pulsing either $\overline{READ}$ or $\overline{WRITE}$ input low, respectively, during the microprocessor bus access cycle (Figure 2-3a).
$\overline{IRQ}$	OC	**Interrupt Request.** $\overline{IRQ}$ interrupt request output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem. The use of $\overline{IRQ}$ is optional depending upon modem application. Refer to Section 3.2 and Table 3-1 for additional information. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high). Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms ±20%, 0.25 W, is sufficient (see Table 2-3).
		V.24 SERIAL INTERFACE Seven pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA-232-D voltage levels. The transmitter and receiver serial interface timing is illustrated in Figures 2-4 and 2-5, respectively.
TXD	IA	**Transmit Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmit Data (TXD) input in serial data mode (PDM bit = 0), or from the interface memory Transmit Data Register (DBUFF) in parallel data mode (PDM bit = 1).
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output and to the interface memory Receive Data Register (DBUFF) in parallel data mode.
$\overline{RTS}$	IA	**Request to Send.** The active low $\overline{RTS}$ input allows the modem to transmit data present at TXD in the serial data mode (PDM bit = 0) or in DBUFF in the parallel data mode (PDM bit = 1) when $\overline{CTS}$ becomes active. The $\overline{RTS}$ hardware control input is logically ORed with the RTSP bit (Table 3-1) by the modem to form the resultant control signal.

Table 2-5. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
CTS	OA	**Clear To Send.** CTS active indicates to the local DTE that the training sequence has been completed and any data present at the TXD input in the serial data mode (PDM bit = 0) or in DBUFF in the parallel data mode (PDM bit = 1) will be transmitted. CTS response times from RTS are shown in Table 1-2. The CTS hardware status output parallels the operation of the CTSP bit (Table 3-1).
RLSD	OA	**Received Line Signal Detector.** For V.29 and V.27 ter; RLSD goes active at the end of the training sequence. If energy is above the turn-on threshold and training is not detected, the RLSD off-to-on response time is 804 baud times. The RLSD on-to-off time is 35±5ms for V.29 or 11.6 ± 5 ms for V.27 ter. The RLSD on-to-off time ensures that all valid data bits have appeared on RXD. The RLSD programmable threshold levels default to –43 dBm for off-to-on and to –48 dBm for on-to-off (see Section 4.2). A minimum hysteresis of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm.
DCLK	OA	**Data Clock.** The modem outputs a single mode-dependent synchronous data clock (DCLK) for USRT timing. The DCLK frequency is 9600, 7200, 4800, 2400, or 300 Hz (± 0.01%) with a duty cycle of 50 ± 1% except in Group 2. In Group 2, the DCLK frequency is 10368 Hz (±5 ppm) when using a precision oscillator. (See Figure 10-1 and 10-2.) Transmit Data (TXD) must be stable during the one microsecond period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.
		AUXILIARY SIGNALS
EN85	I	**Enable 85.** The EN85 input selects the modem microprocessor bus compatibility. When EN85 is low, the modem can interface directly to an 8085 compatible microprocessor bus using READ and WRITE. When EN85 is high, the modem can interface directly to a 6500 compatible microprocessor bus using $\phi 2$ and R/W. In the 6500 configuration, the READ input becomes $\phi 2$ and the WRITE input becomes R/W. This selection is performed only during initialization, i.e., when power is turned on or when POR is activated.
CABLE1, CABLE2	IB IB	**Cable Equalizer Select 1 and 2.** These encoded inputs select equalization for the following cable lengths:

CABLE2	CABLE1	Cable Length	Gain (dB) * 700 Hz	1500 Hz	2000 Hz	3000 Hz
Low	Low	0.0 km	0.00	0.00	0.00	0.00
Low	High	1.8 km	–0.99	–0.20	+0.15	+1.43
High	Low	3.6 km	–2.39	–0.65	+0.87	+3.06
High	High	7.2 km	–3.93	–1.22	+1.90	+4.58

* Relative to 1700 Hz for length of 0.4 mm diameter cable.

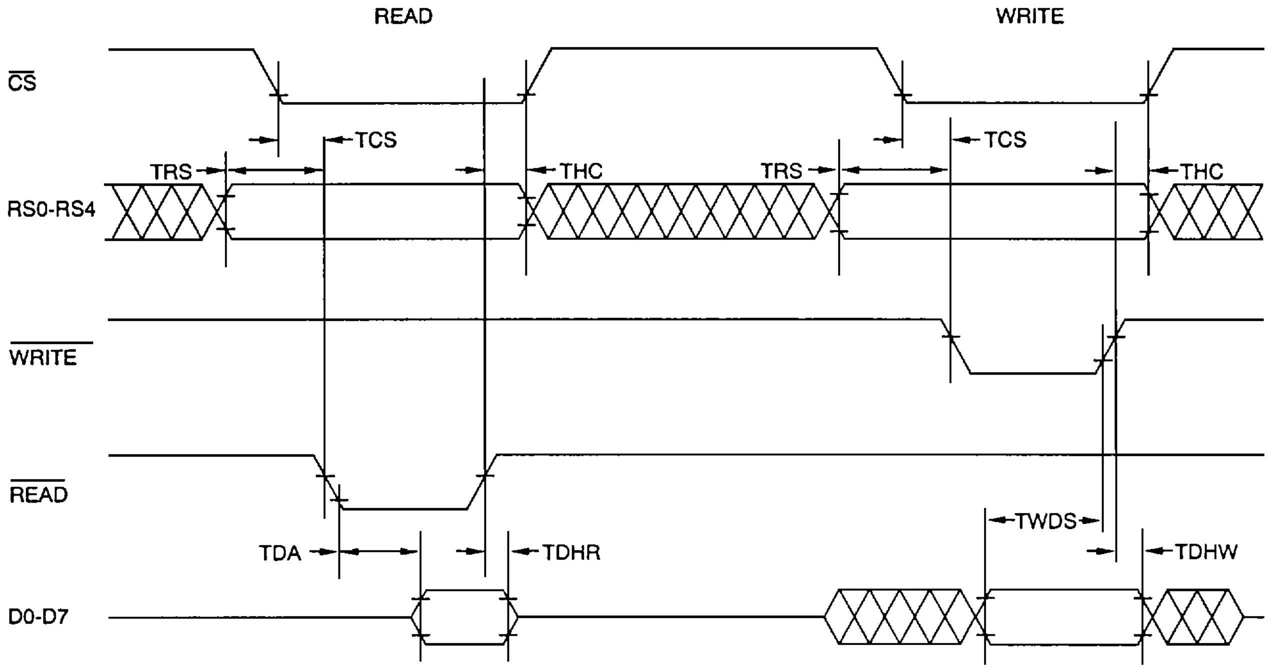
Modems may be connected by direct wiring, such as leased telephone cable or through the PSTN, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some of its route.

To minimize the impact of this copper wire passband shaping, a compromise equalizer with more attenuation at the lower frequencies than at the higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. When selected, the equalizers are inserted in the transmit path when transmitting, and in the receive path when receiving.

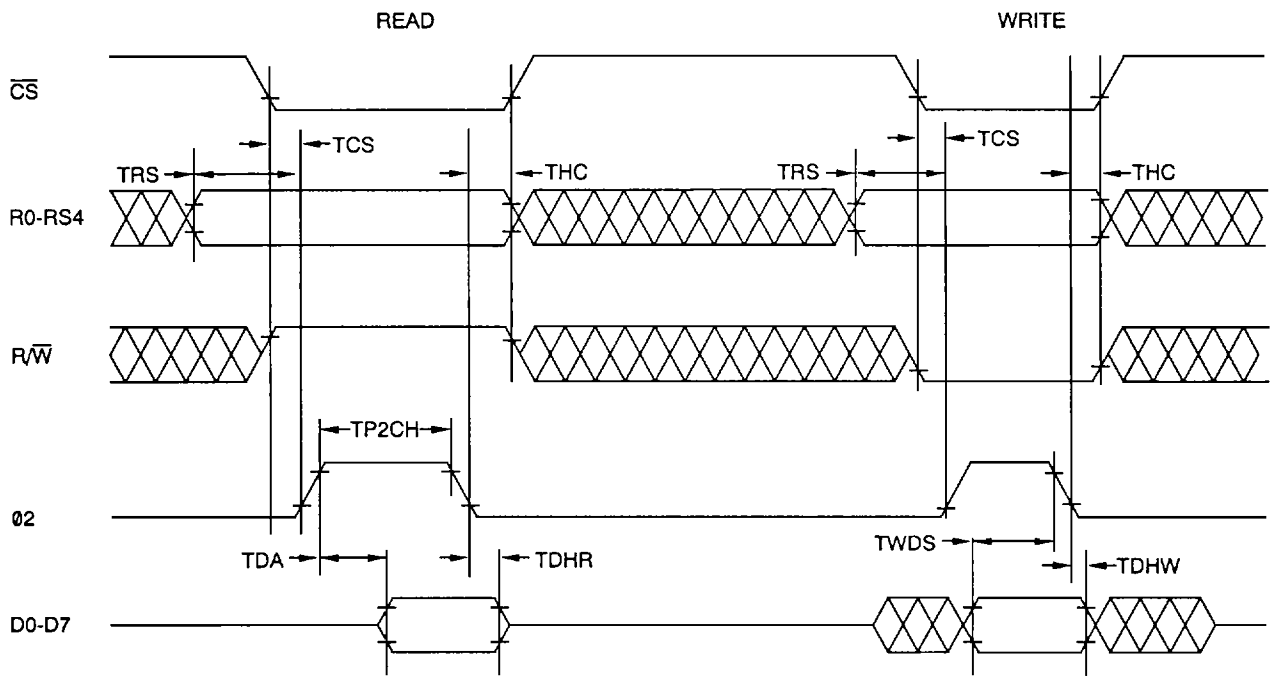
Label	I/O Type	Signal/Definition
XCLK	OD	**XCLK Output.** A 12 MHz (except R96VFX) or 13.2 MHz (R96VFX) square wave output derived from XTLI (XTLI divided by 2).
YCLK	OD	**YCLK Output.** A 6 MHz (except R96VFX) or 6.6 MHz (R96VFX) square wave output derived from XTLI (XTLI divided by 4).

Table 2-5. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		ANALOG SIGNALS
		The Transmitter Analog Output (TXOUT) and Receiver Analog Input (RXIN) allow modem connection to either a leased line or the PSTN through the appropriate buffering and an audio transformer or a data access arrangement. The Auxiliary Input (AUXI) provides access to the transmitter for summing audio signals with the modem's transmitter output. The analog signal characteristics are described in Table 2-4.
TXOUT	AA	**Transmitter Analog Output.** TXOUT can supply a maximum of ± 3.03 volts (peak) into a load resistance of 10K ohms minimum. A 600 ohm line impedance can be matched using an external smoothing filter with a 604 ohm series resistor in its output. The smoothing filter should have a transfer function of 28735.63/(s + 11547.34).
RXIN	AB	**Receiver Analog Input.** The RXIN input impedance is >1M ohms. RXIN requires an external anti-aliasing filter between the modem and the line interface, with a transfer function of 21551.72/(s + 11547.34). The maximum input level into the anti-aliasing filter should not be greater than 0 dBm.
		The filters required for anti-aliasing on the receiver input and the smoothing filter on the transmitter output have a single pole within the modem's passband. Internal filters compensate for its presence, therefore, the pole location must not be changed. Some variation from the recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10K ohms (see Section 10).
AUXI	AC	**Auxiliary Analog Input.** AUXI allows access to the transmitter for the purpose of interfacing with user-provided equipment. Because this is a sampled input, any signal above one half the sample rate will cause aliasing errors. The input impedance is > 1M ohm, and the gain to TXOUT is 0 dBm ± 1 dB.
		EYE DIAGNOSTIC INTERFACE
		Four signals provide the timing necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified. Timing of these signals is illustrated in Figure 2-6 and an example eye pattern generation schematic is shown in Figure 2-7.
EYEX, EYEY	OA OA	**Serial Eye Pattern X Output.** **Serial Eye Pattern Y Output.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters.
		EYEX and EYEY outputs are 9-bit words with their sign bits repeated. The 9-bit data words are shifted out sign bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 230.4 kHz clock. EYECLK* is a clock derived from EYECLK and EYESYNC for shifting EYEX and EYEY data into the serial-to-parallel converters (see Figure 2-7).
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a 9600 Hz strobe used for loading the eye pattern D/A converters.



a. 8085 Bus Compatible ($\overline{EN85}$ = L)



b. 6500 Bus Compatible ($\overline{EN85}$ = H)

820F2-3/910986

Figure 2-3. Microprocessor Interface Waveforms

Table 2-6. Microprocessor Interface Timing

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$ Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns
Phase 2 (φ2) Clock High	TP2CH	100	–	ns

Notes:
1. $\overline{CS}$ and $\overline{READ}$ must not both be active continuously.
2. A read or write operation following a write operation must be delayed by at least 2 YCLK cycles (304 ns for R96VFX; 334 ns for other modems).
3. A read or write operation following a read operation must be delayed by at least 1 YCLK cycle (152 ns for R96VFX; 167 ns for other modems).

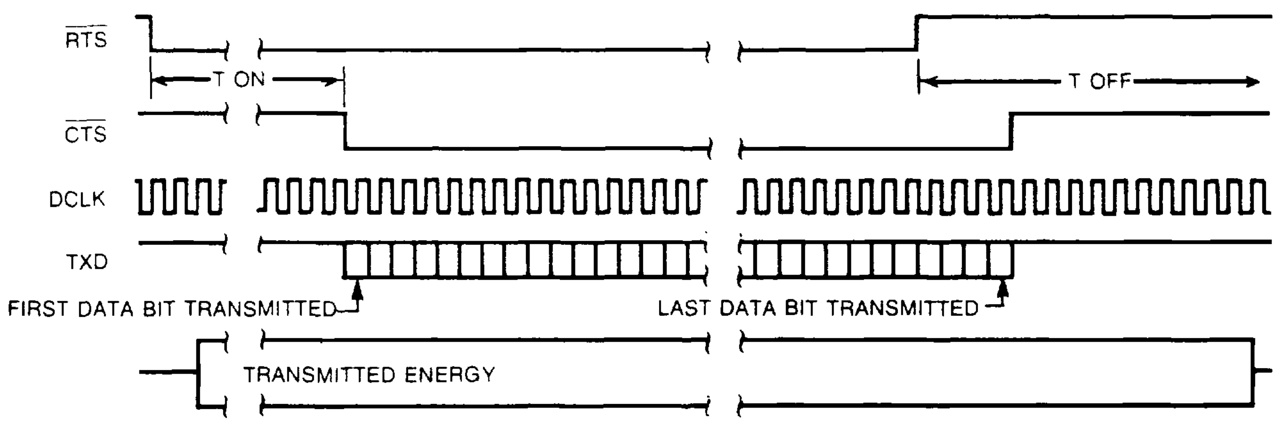


Figure 2-4. Transmitter Signal Timing

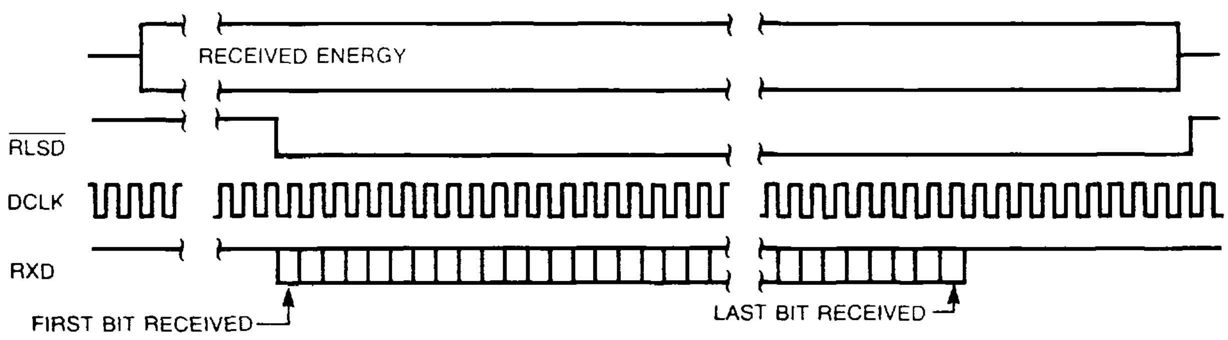


Figure 2-5. Receiver Signal Timing

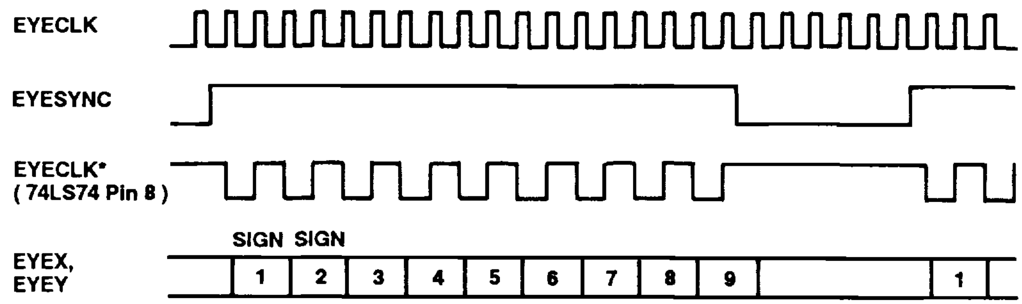


Figure 2-6. Eye Pattern Timing

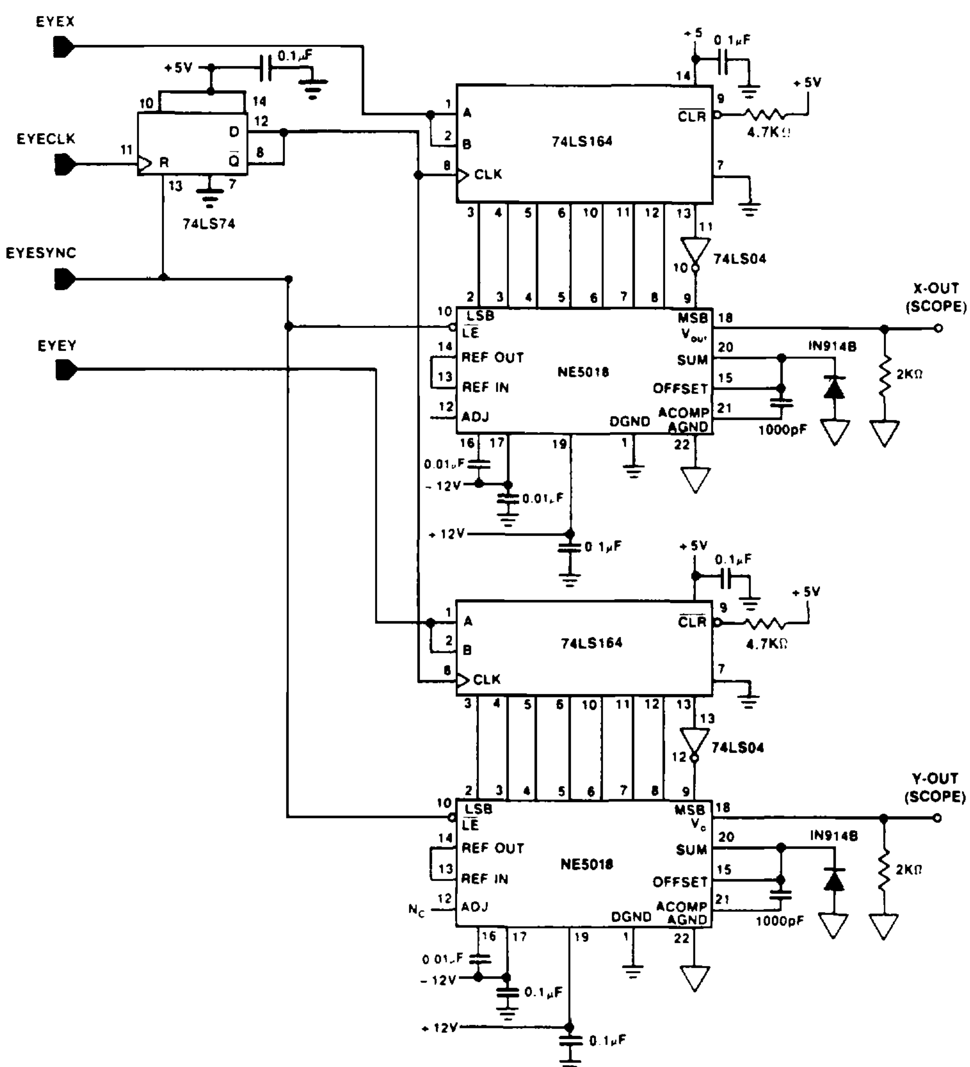


Figure 2-7. Eye Pattern Circuit

3 SOFTWARE INTERFACE

3.1 INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1Fh. Each register can be read from, or written into, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory. Writing parameter values to DSP RAM and reading parameter values from DSP RAM is described in Section 4.

3.1.1 Interface Memory Map

A memory map of the 32 addressable registers in the modem is shown in Figure 3-1. These 8-bit registers may be read or written during any host read or write cycle. In order to operate on a single bit or a group of bits in a register, the host must read a register and then mask out unwanted data. When writing a single bit or group of bits in a register, the host must perform a read-modify-write operation. That is, the entire register (8-bits) must first be read, the necessary bits must be set or reset without altering the other register bits, then the byte (8-bits) containing both the unaltered and modified bits must be written back into the interface memory.

When modifying control bits in a register which also contains active status bits, host to DSP buffer synchronization is required (see BA1 and BA2 bits in Table 3-1).

3.1.2 Interface Memory Bit Definitions

Table 3-1 defines the individual bits in the interface memory. In the Table 3-1 descriptions, bits in the interface memory are referred to using the format Z:Q. The register number is designated by Z (00 through 1Fh), and the bit number by Q (0 through 7, 0 = LSB).

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-XX0-XX0
	1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1	--0X-0X-
Not Available	1D	—	—	—	—	—	—	—	—	XXXXXXXX
	1C	—	—	—	—	—	—	—	—	XXXXXXXX
	1B	—	—	—	—	—	—	—	—	XXXXXXXX
	1A	—	—	—	—	—	—	—	—	XXXXXXXX
	19	—	—	—	—	—	—	—	—	XXXXXXXX
	18	—	—	—	—	—	—	—	—	XXXXXXXX
	17	—	—	—	—	—	—	—	—	XXXXXXXX
	16	—	—	—	—	—	—	—	—	XXXXXXXX
RAM Access 2 Control & Status and Data Buffer	15	ACC2	0	0	0	IO2	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)								--------
	12	X RAM DATA 2 LSB (XDAL2)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
High Speed Status and Group 2 Control	0F	FED		—	—	—	—	CTSP	CDET	--XXXX--
	0E	—	—	—	—	—	—	—	—	XXXXXXXX
	0D	RX	PNDET	—	—	G2FGC	—	—	—	--XX0XXX
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	XX------
Programmable Interrupt Control	0B	ITBMSK*								00000000
	0A	TRIG*		ANDOR*	ITADRS*					00000000
High Speed Control	09	—	—	EQFZ	—	—	—	—	—	XX0XXXXX
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC*	—	—	—	---0-XXX
Mode Control#	07	RTSP	TDIS	PDM	—	EPT	SQEXT	T2	—	000X100X
	06	CONF								00010100
RAM Access 1 Control & Status and Data Buffers	05	ACC1	0	0	0	IO1	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES:
- * Not available in R6628-12.
- ** Not available in R6628-12 and R6628-13.
- \# These bits [except RTSP(all) and TDIS (R6628-13 and above)] require the setting of SETUP to become active.
- — This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).
- \- This symbol in the "Default Value " column indicates that the value is determined by operating conditions.

Figure 3-1a. R96MFX Interface Memory Map

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-XX0-XX0
	1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1	--0X-0X-
Not Available	1D	—	—	—	—	—	—	—	—	XXXXXXXX
	1C	—	—	—	—	—	—	—	—	XXXXXXXX
	1B	—	—	—	—	—	—	—	—	XXXXXXXX
	1A	—	—	—	—	—	—	—	—	XXXXXXXX
	19	—	—	—	—	—	—	—	—	XXXXXXXX
	18	—	—	—	—	—	—	—	—	XXXXXXXX
	17	—	—	—	—	—	—	—	—	XXXXXXXX
	16	—	—	—	—	—	—	—	—	XXXXXXXX
RAM Access 2 Control & Status, HDLC Control, and Data Buffers	15	ACC2	0	0	0	IO2	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)								--------
	12	X RAM DATA 2 LSB (XDAL2)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
High Speed Status and Group 2 Control	0F	FED		—	—	—	—	CTSP	CDET	--XXXX--
	0E	—	—	—	—	—	—	—	—	XXXXXXXX
	0D	RX	PNDET	—	—	G2FGC	—	—	—	--XX0XXX
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	XX------
Programmable Interrupt Control	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control and HDLC Control & Status	09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG	-000----
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC*	—	—	—	---0-XXX
Mode Control#	07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT	T2	HDLC	00001000
	06	CONF								00010100
RAM Access 1 Control & Status and Data Buffers	05	ACC1	0	0	0	IO1	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES:
* Not available in R6631-12.
# These bits [except RTSP(all) and TDIS (R6631-13 and above)] require the setting of SETUP to become active.
— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).
- This symbol in the "Default Value" column indicates that the value is determined by operating conditions.

Figure 3-1b. R96EFX DSP Interface Memory Map

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-XX0-XX0
	1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1	--0X-0X-
Not Available	1D	—	—	—	—	—	—	—	—	XXXXXXXX
DTMF Status	1C	EDET	DTDET	OTS	DTMFD	DTMF				--------
Not Available	1B	—	—	—	—	—	—	—	—	XXXXXXXX
	1A	—	—	—	—	—	—	—	—	XXXXXXXX
	19	—	—	—	—	—	—	—	—	XXXXXXXX
	18	—	—	—	—	—	—	—	—	XXXXXXXX
	17	—	—	—	—	—	—	—	—	XXXXXXXX
	16	—	—	—	—	—	—	—	—	XXXXXXXX
RAM Access 2 Control & Status and HDLC Control	15	ACC2	0	0	0	IO2	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)								--------
	12	X RAM DATA 2 LSB (XDAL2)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
High Speed Status	0F	FED		—	—	—	—	CTSP	CDET	--XXXX--
	0E	—	—	—	—	—	—	—	—	XXXXXXXX
	0D	RX	PNDET	—	—	—	—	—	—	--XXXXXX
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	XX------
Programmable Interrupt Control	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control and HDLC Control & Status	09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG	-000----
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC*	—	—	—	---0-XXX
Mode Control#	07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT	T2	HDLC	00001000
	06	CONF								00010100
RAM Access 1 Control & Status and Programmable Interrupt Control	05	ACC1	0	0	0	IO1	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES: * Not available in R6633-11.
These bits [except RTSP(all) and TDIS (R6633-12 and above)] require the setting of SETUP to become active.
— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).
- This symbol in the "Default Value " column indicates that the value is determined by operating conditions.

Figure 3-1c. R96DFX DSP Interface Memory Map

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-XX0-XX0
	1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1	--0X-0X-
Not Available	1D	—	—	—	—	—	—	—	—	XXXXXXXX
DTMF Status	1C	EDET	DTDET	OTS	DTMFD	DTMF				--------
Not Available	1B	—	—	—	—	—	—	—	—	XXXXXXXX
ADPCM Status	1A	EDETC	DTDETC	OTSC	DTMFDC	FRx	FSK7EC	DCDBA	CDBA	--------
Not Available	19	—	—	—	—	—	—	—	—	XXXXXXXX
	18	—	—	—	—	—	—	—	—	XXXXXXXX
	17	—	—	—	—	—	—	—	—	XXXXXXXX
	16	—	—	—	—	—	—	—	—	XXXXXXXX
RAM Access 2 Control & Status, HDLC Control, and Data Buffers	15	ACC2	0	AEOF	0	IO2	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)/VOICE BUFFER 2 MSB (VBUF2M)								--------
	12	X RAM DATA 2 LSB (XDAL2)/VOICE BUFFER 2 LSB (VBUF2L)								--------
	11	Y RAM DATA 2 MSB (YDAM2)/VOICE BUFFER 1 MSB (VBUF1M)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)/ VOICE BUFFER 1 LSB (VBUF1L)								--------
Modem Status and ADPCM Control	0F	FED		—	—	—	—	CTSP	CDET	--XXXX--
	0E	FSKFLS	DTMFE	DCDEN	CDEN	SDCDE	SCDE	FRZSL	TDTEN	--------
Modem Status	0D	RX	PNDET	—	—	—	—	—	—	--XXXXXX
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	XX------
Programmable Interrupt Control	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control and HDLC Control & Status	09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG	-000----
Modem Control & Status	08	FR3	FR2	FR1	12TH	PNSUC	FSK7E	—	PDEQZ	---0--X0
Mode Control *	07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT		HDLC	00001000
	06	CONF								00010100
RAM Access 1 Control & Status and Data Buffers	05	ACC1	0	0	0	IO1	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES: * A changed value in these registers (except RTSP and TDIS) require the setting of SETUP to become active.
— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).
- This symbol in the "Default Value" column indicates that the value is determined by operating conditions.

Figure 3-1d. R96VFX DSP Interface Memory Map

Table 3-1. Modem Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
12TH	08:4	0	**Select 12th Order.** When control bit 12TH is set, the tone detectors operate as one 12th order filter (uses FR3). When 12TH is reset, the tone detectors operate as three parallel independent 4th order filters (FR1, FR2, FR3). 12TH is valid in FSK, FSK and DTMF receiver, Group 2, voice, tone, or ADPCM mode (i.e., CONF = 2x, 40, 8x, or 9x) with RTS off and RTSP reset.
ABIDL	09:3	–	**Abort/Idle.** When the modem is configured as a transmitter and control/status bit ABIDL is set, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is reset, or continuous zeros if ZEROC is set. When ABIDL is reset, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is reset, or eight continuous zeros if ZEROC is set. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is set) and the modem will send at least eight continuous ones (if ZEROC is 0) or eight continuous zeros (if ZEROC is 1). To stop continuous one or zero transmission, ABIDL must be reset by the host. (HDLC only.) (See Section 5.1 and Figure 5-6.) When the modem is configured as a receiver and status bit ABIDL is set, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host. (HDLC only.) (See Section 5.1 and Figure 5-7.)
ACC1	05:7	1	**RAM Access 1.** When control bit ACC1 is set, the modem accesses the RAM associated with the address in ADD1 and the CR1 bit. WRT1 determines if a read or write is performed.
ACC2	15:7	0	**RAM Access 2.** When control bit ACC2 is set, the modem accesses the RAM associated with the address in ADD2 and the CR2 bit (provided parallel data mode and HDLC are not selected). WRT2 determines if a read or write is performed.
ADD1	04:0-7	17	**RAM Address 1.** ADD1 contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 LSB and MSB words (2:0-7 and 3:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (0:0-7 and 1:0-7, respectively).
ADD2	14:0-7	00	**RAM Address 2.** ADD2 contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
AEOF	15:5	0	**Automatic End of Frame.** When the modem is configured as an HDLC transmitter and AEOF control bit is set, the modem interprets an underrun condition as an end of frame and outputs the FCS and at least one ending flag. (HDLC only.) (R96VFX only.)
ANDOR	0A:5	–	**AND/OR Bit Mask Function.** When control bit ANDOR is set and the programmable interrupt is enabled, the modem will assert IRQ if all the bits in the register specified by ITADRS and masked by ITBMSK are ones. When ANDOR is reset and the programmable interrupt is enabled, the modem will assert IRQ if any one of the bits in the register specified by ITADRS and masked by ITBMSK is a one.
BA1	1E:0	–	**Buffer Available 1.** When set, status bit BA1 signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) (register 00:0-7). If the modem is in Voice Transmitter mode, the modem sets BA1 when the contents of register 00:0-7 have been transmitted. Setting BA1 can also cause IRQ to be asserted. The host writing to or reading from register 00 resets the BA1 and IA1 bits. (See IE1 and IA1.)
BA2	1E:3	–	**Buffer Available 2.** If the modem is in the parallel data mode or HDLC is selected, the modem sets status bit BA2 when it has read the transmit byte from DBUFF (register 10:0-7) when transmitting (buffer becomes empty), or it has written the received byte to DBUFF (register 10:0-7) when receiving (buffer becomes full). If the modem is not in parallel data mode and HDLC is not selected, the modem sets BA2 when it has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) (register 10:0-7). If the modem is in ADPCM mode and the coder or decoder is selected, the modem sets BA2 when it has written coder output to, or read decoder input from , VBUF1L (register 10:0-7). Setting BA2 can also cause IRQ to be asserted. The host writing to or reading from register 10 resets the BA2 and IA2 bits. (See IE2 and IA2.)

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
BR1	05:2	1	**Baud Rate 1.** When control bit BR1 is set, RAM access for ADD1 occurs at the baud rate; when BR1 is reset, RAM access occurs at the sample rate. This bit must be reset in FSK, FSK and DTMF receiver, Group 2, voice, tone, or ADPCM mode (i.e., CONF = 2x, 40, 8x, or 9x).
BR2	15:2	0	**Baud Rate 2.** When control bit BR2 is set, RAM access for ADD2 occurs at the baud rate; when BR2 is reset, RAM access occurs at the sample rate. This bit must be reset in FSK, FSK and DTMF receiver, Group 2, voice, tone, or ADPCM mode (i.e., CONF = 2x, 40, 8x, or 9x).
CDBA	1A:0	0	**Coder Buffer Available.** If the ADPCM codec is enabled (CDEN = 1 and DCDEN = 1), the modem sets status bit CDBA when the coder output buffer (VBUF2x, x = L and M) becomes full. The host must reset CDBA after reading VBUF2L. If the decoder is disabled (DCDEN = 0), status bits BA2 and CDBA will be set by the modem when the coder output buffers become full (VBUF1x = VBUF2x). (ADPCM only.)
CDEN	0E:4	0	**Coder Enable.** When control bit CDEN is set, the modem performs ADPCM coding. The coder output is placed into VBUF2x (x = L and M). If the decoder is disabled (DCDEN = 0), the coder output is also placed in VBUF1x. RTS must be off and RTSP must be reset if the decoder is enabled (DCDEN = 1) for the input to be received on RXA. If the decoder is disabled (DCDEN = 0), the modem accepts input from RXA regardless of the state of RTS and RTSP. ACC2 must be reset. When CDEN is reset, the modem does not perform ADPCM coding. (ADPCM only.)
CDET	0F:0	–	**Carrier Detected.** When status bit CDET is set, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is reset, the receiver is in the idle state or in the process of training.
CONF	06:0-7	14	**Configuration.** The CONF control bits select the modem configuration as follows:

CONF (Hex)	Configuration	Notes
14	V.29 9600 bps	1
12	V.29 7200 bps	1
11	V.29 4800 bps	1
0A	V.27 ter 4800 bps	2
09	V.27 ter 2400 bps	2
20	Transmit: V.21 Channel 2 300 bps (FSK)	3
	Receive: V.21 Channel 2 300 bps (FSK) and Tone Detector	3,6
21	Transmit: V.21 Channel 2 300 bps (FSK)	3
	Receive: V.21 Channel 2 300 bps (FSK), Tone Detector, and DTMF Receiver (sample rate = 9600 Hz)	3,6,7
40	Group 2	4
80	Transmit: Dual Tone	5
	Receive: Tone Detector	6
82	Transmit: 76.8K bps Voice mode (default sample rate = 9600 Hz)	8
	Receive: 76.8K bps Voice mode and Tone Detector	6,8
90	ADPCM 16k bps coder and 16k bps decoder, DTMF Receiver, and Tone Detector	9
91	ADPCM 24k bps coder and 16k bps decoder, DTMF Receiver, and Tone Detector	9
92	ADPCM 32k bps coder and 16k bps decoder, DTMF Receiver, and Tone Detector	9
94	ADPCM 16k bps coder and 24k bps decoder, DTMF Receiver, and Tone Detector	9
95	ADPCM 24k bps coder and 24k bps decoder, DTMF Receiver, and Tone Detector	9
96	ADPCM 32k bps coder and 24k bps decoder, DTMF Receiver, and Tone Detector	9
98	ADPCM 16k bps coder and 32k bps decoder, DTMF Receiver, and Tone Detector	9
99	ADPCM 24k bps coder and 32k bps decoder, DTMF Receiver, and Tone Detector	9
9A	ADPCM 32k bps coder and 32k bps decoder, DTMF Receiver, and Tone Detector	9

Notes:

1. **V.29.** When a V.29 configuration is selected, the modem operates as specified in CCITT Recommendation V.29 with concurrent receive single tone detection (FR3) (see Section 6) and FSK flag pattern (7E) detection (R96VFX only, see Section 3.2.5). FSK flag pattern detection is not performed during V.29 short train (R96VFX).

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
			2. **V.27 ter.** When a V.27 ter configuration is selected, the modem operates as specified in CCITT Recommendation V.27 ter with concurrent receive single tone detection (FR3) (see Section 6) and FSK flag pattern (7E) detection (R96VFX only, see Section 3.2.5). FSK flag pattern detection is not performed during V.27 ter short train.
			3. **V.21 Channel 2.** When a V.21 Channel 2 configuration is selected, the modem operates as specified in CCITT Recommendation V.21 channel 2.
			4. **Group 2 (R96MFX and R96EFX only)** .When Group 2 configuration is selected, the modem operates as specified in CCITT Recommendation T.3.
			5. **Dual Tone.** When the Dual Tone Transmit configuration is selected, the modem transmits single or dual frequency tones in response to RTS or RTSP. Tone frequencies and amplitudes are programmable in the DSP RAM (see Section 4.2).
			6. **Tone Detector.** When a Tone Detector configuration is selected and 12TH is set, the three 4th order tone detect filters are combined into a single 12th order tone detect filter (FR3). If 12TH is not set, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable (see Section 6).
			7. **DTMF Receiver (R96DFX and R96VFX only).** When a DTMF Receiver configuration is selected, the modem operates as a DTMF receiver (see Section 3.2.4).
			8. **Voice Mode.** When the Voice mode configuration is selected, the A/D or the D/A converter is available for voice reception or transmission (see Section 3.2.3). The voice mode receiver is also available in ADPCM coder/decoder configurations when the FRZSL bit is set (see Section 10.3.3).
			9. **ADPCM Coder/Decoder (R96VFX only).** When an ADPCM coder/decoder configuration is selected, the codec operates at 32k, 24k, or 16k bps (default sample rate = 8000 Hz) (see Section 10). Concurrent receiver FSK flag pattern (7E) detection may be enabled (see FSKFLS) (see Section 3.2.5).
			Note: ACC2 must be reset when the coder or decoder is enabled.
CR1	05:0	1	**Coefficient RAM 1 Select.** When control bit CR1 is set, ADD1 addresses Coefficient RAM. When CR1 is reset, ADD1 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is set, ADD2 addresses Coefficient RAM. When CR2 is reset, ADD2 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CRC	09:1	–	**Cyclic Redundancy Check error.** When status bit CRC is set and status bit EOF is set, the received frame is in error. When CRC is reset and EOF is set, the received frame is correct. CRC only changes immediately before EOF is set. (HDLC only.)
CTSP	0F:1	–	**Clear To Send Parallel.** When set, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at TXD (PDM = 0) or DBUFF (PDM = 1) will be transmitted. CTSP parallels the operation of the CTS pin.
DATA	0C:5	–	**Data Mode.** When status bit DATA = 1, the high speed transmitter/receiver is in the data mode.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode, the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first.
DCDBA	1A:1	0	**Decoder Buffer Available.** If the ADPCM decoder is enabled (DCDEN=1), the modem sets status bit DCDBA when the decoder input buffer (VBUF1x, x=L & M) becomes empty. The host must write the next 16-bit decoder input into VBUF1 then reset DCDBA. **Note:** Since status bit BA2 will be set by the modem when the decoder buffer is empty, the host may choose to ignore DCDBA. (ADPCM only.)

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DCDEN	0E:5	0	**Decoder Enable.** When control bit DCDEN is set, the modem performs ADPCM decoding on the VBUF1x (x = L and M) input. The decoder analog output is sent to TXA if RTS is on or RTSP is set, otherwise the modem accepts input from RXA. ACC2 must be reset. When control bit DCDEN is reset, the modem does not perform ADPCM decoding on the VBUF1x input. In this case, the modem accepts input from RXA regardless of the state of RTS and RTSP. (ADPCM only.)
DTDET	1C:6	–	**Dual Tone Detected.** When the modem receives a signal that satisfies all DTMF criteria except on-time, off-time, and cycle-time, DTDET will be set by the modem. The encoded DTMF value is available when DTDET is set. If the received signal is a valid DTMF signal, then DTDET will be set approximately 11 ms following the setting of EDET. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy any DTMF criteria. (DTMF only.)
DTDETC	1A:6	–	**Dual Tone Detected Copy.** The DTDETC bit copies the DTDET bit (1C:6). (ADPCM only.)
DTMF	1C:0-3	–	**DTMF Output Word.** When a DTMF tone is present such that status bit DTDET is set by the modem, the encoded DTMF output will be written into 1C:0-3. (DTMF only.) The DTMF symbol codes are:

DTMF Symbol	Encoded Output (Hex)	DTMF Symbol	Encoded Output (Hex)
1	0	3	8
4	1	6	9
7	2	9	A
*	3	#	B
2	4	A	C
5	5	B	D
8	6	C	E
0	7	D	F

Mnemonic	Memory Location	Default Value	Name/Description
DTMFD	1C:4	–	**DTMF Signal Detected.** Status bit DTMFD is set when a DTMF signal has been detected that satisfies all specified DTMF detect criteria. The host must reset this bit after reading DTMF. (DTMF only.)
DTMFDC	1A:4	–	**DTMF Signal Detected Copy.** The DTMFDC bit copies the DTMFD bit (1C:4). (ADPCM only.)
DTMFE	0E:6	0	**DTMF Receiver Enable.** When control bit DTMFE is set, the DTMF receiver is enabled in an ADPCM codec configuration. When DTMFE is reset, the DTMF receiver is disabled. (ADPCM only.)
EDET	1C:7	–	**DTMF Early Detection.** Status bit EDET is set by the modem when the received signal may be a DTMF tone. EDET is set approximately 20 ms after the DTMF signal energy is detected. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy any DTMF criteria. (DTMF only.)
EDETC	1A:7	–	**DTMF Early Detection Copy.** The EDETC bit copies the EDET bit (1C:7). (ADPCM only.)
EOF	09:2	–	**End Of Frame.** When the modem is configured as a transmitter and bit AEOF is 0, the EOF bit is a control bit. When AEOF is a 0, to convey to the modem that it is time to send the 16-bit FCS and ending flag of a HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (BA2 sets again). EOF will then be reset by the modem after it has recognized the setting of EOF by the host. When the modem is configured as a transmitter and bit AEOF is a 1, EOF is a status bit. In this case, the modem will interpret the underrun condition as the end of the frame, set EOF, and will output the 16-bit FCS and at least one ending flag. EOF is reset whenever a flag is transmitted. (HDLC only.) When the modem is configured as a receiver and status bit EOF is a 1, the modem has received a frame ending flag and bit CRC is updated. EOF must be reset by the host before receiving the ending flag of a following frame. (HDLC only.)

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
EPT	07:3	1	**Echo Protector Tone Enable.** When control bit EPT is set, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is reset, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 which transmits 20 ms of silence at the beginning of training.
EQFZ	09:5	0	**Equalizer Freeze.** When control bit EQFZ is set, updating of the receiver's adaptive equalizer taps is inhibited.
EQSV	09:6	0	**Equalizer Save.** When control bit EQSV is set, the adaptive equalizer taps are not zeroed when entering the training state, or when reconfiguring the modem except in ADPCM configurations (CONF = 9xh). Adaptive equalizer taps are also not updated during training. This bit is used in conjunction with the SHTR and EQFZ bits.
FED	0F:7,6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes. **FED** — **Energy Level** 0 — No energy 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold
FLAG	09:0	0	**FLAG Mode.** When the modem is configured as a transmitter and status bit FLAG is set, the modem is transmitting a flag sequence. When the modem is configured as a receiver and status bit FLAG is set, the modem has received a flag sequence. (HDLC only.)
FR1	08:5	–	**Frequency No. 1.** Status bit FR1 is set by the modem when energy is being detected above tone detector 1's turn-on threshold (default detection range = 2100 Hz ± 25 Hz). FR1 is operable in $\overline{\text{FSK}}$, FSK and DTMF receiver, voice, tone, or ADPCM mode (i.e., CONF = 2x, 8x, or 9x) with $\overline{\text{RTS}}$ off and RTSP reset.
FR2	08:6	–	**Frequency No. 2.** Status bit FR2 is set by the modem when energy is being detected above tone detector 2's turn-on threshold (default detection range = 1100 Hz ± 30 Hz). FR2 is operable in $\overline{\text{FSK}}$, FSK and DTMF receiver, voice, tone, or ADPCM mode (i.e., CONF = 2x, 8x, or 9x) with $\overline{\text{RTS}}$ off and RTSP reset.
FR3	08:7	–	**Frequency No. 3.** Status bit FR3 is set by the modem when energy is being detected above tone detector 3's turn-on threshold (default detection range = 462 Hz ±14 Hz). FR3 is operable in all receive modes with $\overline{\text{RTS}}$ off and RTSP reset.
FRx	1A:3	–	**Frequency No. 1, 2, or 3.** Status bit FRx is set by the modem if FR1, FR2, or FR3 is set. FRx is reset by the modem if FR1, FR2, and FR3 are reset. (ADPCM only.)
FRZSL	0E:1	0	**Freeze Slew Rate.** When control bit FRZSL is set, the modem will not change the slew rate. When FRZSL is reset, the AGC slew rate is controlled by the modem. When FRZSL is set, the host may implement the voice mode receiver described in Section 3.2.3 with CONF = 9xh. (ADPCM only.)
FSK7E	08:2	–	**FSK Flag (7E) Detected.** The modem sets status bit FSK7E when FSK flags have been detected in either high speed or ADPCM codec receiver modes. FSK7E is valid after bit FSKFLS transitions from set to reset (1 to 0) in the high speed modes. In the ADPCM codec receiver modes, the FSK 7E flag detector runs continuously unless disabled by the user (FSKFLS = 0). FSK7E is set when a flag is detected. FSK7E must be reset by the host if additional flags are to be detected. FSK7E is not valid in short train mode. (R96VFX only.)
FSK7EC	1A:2	–	**FSK Flag (7E) Detected Copy.** The FSK7EC bit copies the FSK7E bit (08:2). (ADPCM only.)

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
FSKFLS	0E:7	–	**FSK Flag (7E) Search.** In the high speed receiver modes, when status bit FSKFLS is set, the modem is searching for FSK flags. In the high speed mode this bit is set by the modem at the start of the FSK flag search, and reset by the modem when the FSK flag search is completed. (R96VFX only.) In the ADPCM receiver modes, FSK flag search is enabled when control bit FSKFLS is set by the host. FSK flag search is disabled when FSKFLS is reset by the host. The default state of FSKFLS is set in this mode. (R96VFX only.)
G2FGC	0D:3	0	**Group 2 Fast Gain Control.** When control bit G2FGC is set, a fast AGC rate (8.6 times standard) is selected (Group 2).
HDLC	07:0	0	**HDLC.** When control bit HDLC is set, the modem performs HDLC framing. To become active, the host must set HDLC and PDM followed by the setting of SETUP. When control bit HDLC is reset, the modem does not perform HDLC framing provided SETUP was set following the resetting of HDLC.
IA1	1E:6	–	**Interrupt Active 1.** When Interrupt Enable 1 is enabled (IE1 is set) and BA1 is set by the modem, the modem asserts IRQ and sets status bit IA1 to indicate that BA1 being set caused the interrupt. The host writing to or reading from register 00 resets IA1. (See IE1 and BA1.)
IA2	1E:7	–	**Interrupt Active 2.** When Interrupt Enable 2 is enabled (IE2 is set) and BA2 is set by the modem, the modem asserts IRQ and sets status bit IA2 to indicate that BA2 being set caused the interrupt. The host writing to or reading from register 10 resets IA2. (See IE2 and BA2.)
IE1	1E:2	0	**Interrupt Enable 1.** When control bit IE1 is set (interrupt enabled), the modem will assert IRQ and set IA1 when BA1 is set by the DSP. When IE1 is reset (interrupt disabled), BA1 has no effect on IRQ and IA1. (See BA1 and IA1.)
IE2	1E:5	0	**Interrupt Enable 2.** When control bit IE2 is set (interrupt enabled), the modem will assert IRQ and set IA2 when BA2 is set by the DSP. When IE2 is reset (interrupt disabled), BA2 has no effect on IRQ and IA2. (See BA2 and IA2.)
IO1	05:3	0	**Input/Output RAM 1 Select**. When control bit IO1 is set, ADD1 addresses IO RAM. When IO1 is reset, ADD1 addresses either coefficient or data RAM depending on the state of the CR1 bit. This bit must be set according to the desired RAM address. (See Table 4-1.)
IO2	15:3	0	**Input/Output RAM 2 Select**. When control bit IO2 is set, ADD2 addresses IO RAM. When IO2 is reset, ADD2 addresses either coefficient or data RAM depending on the state of the CR2 bit. This bit must be set according to the desired RAM address. (See Table 4-1.)
ITADRS	0A:0-4	–	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take affect. The address of the byte on which the modem asserts IRQ on a bit or bits in that byte is specified below:

Host Register (Hex)	ITADRS (Hex)	Host Register (Hex)	ITADRS (Hex)
00	00	10	08
01	10	11	18
02	01	12	09
03	11	13	19
04	02	14	0A
05	12	15	1A
06	03	16	0B
07	13	17	1B
08	04	18	0C
09	14	19	1C
0A	05	1A	0D
0B	15	1B	1D
0C	06	1C	0E
0D	16	1D	1E
0E	07	1E	0F
0F	17	1F	1F

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
ITBMSK	0B:0-7	–	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert $\overline{IRQ}$ on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
OTS	1C:5	–	**DTMF On-Time Satisfied.** Status bit OTS is set by the modem when the on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy any DTMF criteria.
OTSC	1A:5	–	**DTMF On-Time Satisfied Copy.** The OTSC bit copies the OTS bit (1C:5). (ADPCM only.)
OVRUN	09:7	–	**Overrun/Underrun.** When the modem is configured as a transmitter, and status bit OVRUN is set, a transmit underrun condition has occurred. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL will set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host resets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if BA2 is reset) or will transmit continuous flags. The modem will reset OVRUN every time it sets BA2. If AEOF is a 1, OVRUN is disabled. (HDLC only.) When the modem is configured as a receiver and status bit OVRUN is set, an overrun condition has occurred. To detect the next overrun condition, the host must reset this bit. (HDLC only.)
P1	0C:1	–	**P1 Sequence.** When the modem is configured as a high speed transmitter, status bit P1 = 1 indicates the P1 sequence is being sent. When P1 = 0, the P1 sequence is not being transmitted. When the modem is configured as a receiver, the P1 bit has no meaning.
P2	0C:2	–	**P2 Sequence.** When the modem is configured as a high speed transmitter, status bit P2 = 1 indicates the P2 sequence is being sent. When P2 = 0, the P2 sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit P2 = 1 indicates the search for the P2 to PN transition is occurring. When P2 = 0, the P2 to PN transition search is not occurring.
PDEQZ	08:0	0	**Programmable Digital Equalizer.** When the host has configured the modem as a high speed receiver and has set control bit PDEQZ, the programmable digital equalizer is enabled. When control bit PDEQZ is reset, the programmable digital equalizer is disabled. The programmable digital equalizer defaults to a Japanese 2 link delay equalizer. (R96VFX only.)
PDM	07:5	0	**Parallel Data Mode.** When control bit PDM is set and the modem is a transmitter, it accepts data for transmission from DBUFF (10:0-7) rather than the TXD input. When PDM is set and the modem is a receiver, the modem provides the received data to the host using DBUFF (10:0-7).
PIA	1F:7	–	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts $\overline{IRQ}$ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. PIA is reset when the host resets PIREQ.

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. When PIE is reset (interrupt disabled), ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on IRQ and PIA.
PIREQ	1F:3	–	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is set) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if control bit PIREQ has been previously reset by the host. PIREQ is set by the modem when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert IRQ.
PN	0C:3	–	**PN Sequence.** When the modem is configured as a high speed transmitter, status bit PN = 1 signals that the PN sequence is being sent. When PN = 0, the PN sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit PN = 1 indicates the PN portion of the training sequence is being received. When PN = 0, the PN portion of training is not being received.
PNDET	0D:6	–	**PN Detected.** When status bit PNDET is set, the receiver has detected the PN portion of the training sequence. When PNDET is reset, PN has not been detected.
PNSUC	08:3	–	**PN Success.** When status bit PNSUC is set, the receiver has successfully trained at the end of the PN portion of the high speed training sequence. When PNSUC is reset, a successful training has not occurred. PNSUC is still valid after the CDET bit is set. (See note in Figures 3-1a, 3-1b, and 3-1c.)
RTSP	07:7	0	**Request To Send Parallel.** The set state of RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is reset, and the turn-off sequence has been completed. RTSP parallels the operation of the hardware RTS control input. These inputs are "ORed" by the modem. (See note in Figure 3-1.)
RX	0D:7	–	**Receive State.** When status bit RX is set, the modem is in the receive state and is not transmitting.
SCDE	0E:2	0	**Silence Coder Enable.** When control bit SCDE is set and the ADPCM coder is enabled (CDEN = 1), the modem performs silence detection and deletion. When SCDE is reset, the modem does not perform silence detection and deletion. (ADPCM only.)
SCR1	0C:4	–	**Scrambled Ones.** When the modem is configured as a high speed transmitter, status bit SCR1= 1 indicates scrambled ones are being sent. When SCR1 = 0, scrambled ones are not being transmitted., When the modem is configured as a high speed receiver, status bit SCR1 = 1 indicates scrambled ones are being received. When SCR1 = 0, scrambled ones are not being received.
SDCDE	0E:3	0	**Silence Decoder Enable.** When control bit SDCDE is set and the ADPCM decoder is enabled (DCDEN = 1), the modem performs silence interpolation. When SDCDE is reset, the modem does not perform silence interpolation. Silence must have been previously deleted during coding. (ADPCM only.)
SETUP	1F:0	0	**Setup.** Control bit SETUP must be set by the host after the host writes a configuration code into the CONF bits (register 6:0-7) or changes a bit in register 7:0-5. Setting the SETUP bit informs the modem to implement the configuration change. The modem resets the SETUP bit when the configuration change request is recognized. The host should not set the SETUP bit when the RTSP bit is set or RTS is asserted.

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
SHTR	07:4	0	**Short Train.** When SHTR is set and CONF is either 1X or 0X, the modem will perform a V.29 or V.27 ter short training sequence, respectively. A successful V.29 or V.27 ter long train at the same data rate must precede the short train. The setting of the SHTR bit, along with the setting of the EQSV bit, must be followed by the setting of the SETUP bit.
SIDLE	0C:0	–	**Silence/Idle.** When the modem is configured as a high speed transmitter, status bit SIDLE = 1 indicates the modem is transmitting silence. When the modem is configured as a high speed receiver, status bit SIDLE = 1 indicates the modem is waiting for energy (idling).
SQEXT	07:2	0	**Squelch Extend.** When control bit SQEXT is set, the modem's receiver is inhibited from the reception of any signal for 140 ms after the transmitter turn-off.
T2	07:1	0	**T/2 Equalizer Select.** When control bit T2 is set, the receiver's adaptive equalizer is T/2 fractionally spaced. When T2 is reset, the receiver's adaptive equalizer is T spaced (T = 1 baud time). (All except R96VFX; the R96VFX is always T/2 spaced.)
TDIS	07:6	0	**Training Disable.** When control bit TDIS is set, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when RTS is on or RTSP is set. (See note in Figure 3-1.)
TDTEN	0E:0	1	**Tone Detector Enable.** When control bit TDTEN is set, the three programmable tone detectors/12th order programmable filter are/is enabled. If TDTEN is reset, then the three programmable tone detectors/12th order programmable filter are/is disabled. (ADPCM only.)
TRIG	0A:6-7	–	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled. The user has the option to be continuously interrupted whenever the interrupt condition is true (DC triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): **TRIG** — **Description** 00 — DC 01 — Positive Edge 10 — Negative Edge 11 — Edge
VBUF1L	10:0-7	–	**Voice Buffer 1 Least Significant Byte (LSB).** VBUF1L is the least significant byte of the 16-bit ADPCM decoder input buffer (DCDEN = 1) or coder output buffer (CDEN = 1 and DCDEN = 0). The modem reading or writing to this register sets the BA2 bit. The host reading or writing to this register resets the BA2 bit. The modem sets status bit CDBA when the modem writes to VBUF1L and sets status bit DCDBA when reading from VBUF1L. By setting IE2, the host can enable the assertion of IRQ upon the setting of BA2. Bit 0 of VBUF1L is the first bit of the 16-bit decoder input/coder output. (ADPCM only.)
VBUF1M	11:0-7	–	**Voice Buffer 1 Most Significant Byte (MSB).** VBUF1M is the most significant byte of the 16-bit ADPCM decoder input buffer (DCDEN = 1) or coder output buffer (CDEN = 1 and DCDEN = 0). Bit 7 of VBUF1M is the last bit of the 16-bit decoder input/coder output. VBUF1M should be read from or written to before VBUF1L. (ADPCM only.)
VBUF2L	12:0-7	–	**Voice Buffer 2 Least Significant Byte (LSB).** VBUF2L is the least significant byte of the 16-bit ADPCM coder output buffer. The modem writing to this register sets the CDBA status bit. The host reading this register does not reset the CDBA bit. Bit 0 of VBUF2L is the first bit of the 16-bit coder output. (ADPCM only.)
VBUF2M	13:0-7	–	**Voice Buffer 2 Most Significant Byte (MSB).** VBUF2M is the most significant byte of the 16-bit ADPCM coder output buffer. Bit 7 of VBUF2M is the last bit of the 16-bit coder output. VBUF2M should be read before VBUF2L. (ADPCM only.)

Table 3-1. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
WRT1	05:1	0	**RAM Write 1.** When control bits WRT1 is set, ACC1 is set, and BA1 is reset, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by ADD1 and CR1. (When the most significant bit of ADD1 is reset, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is reset and ACC1 is set, the modem reads data from its internal RAM from the locations addressed by ADD1 and CR1 and stores it into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2.** When control bits WRT2 is set, ACC2 is set, and BA2 is reset, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by ADD2 and CR2. (When the most significant bit of ADD2 is reset, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is reset and ACC2 is set, the modem reads data from its internal RAM from the locations addressed by ADD2 and CR2 and stores it into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.
XDAL1	02:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the least significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the least significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	03:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	00:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the least significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the least significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
YDAM1	01:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the most significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the most significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
ZEROC	09:4	0	**Zero Clamp.** When control bit ZEROC is set and ABIDL is set, the modem will transmit continuous zeros. When ZEROC is reset and ABIDL is set, the modem will transmit continuous ones. If ABIDL is reset, ZEROC is disabled. (HDLC only.)

3.2 SOFTWARE INTERFACE CONSIDERATIONS

3.2.1 Parallel Data Transfer

Register 10 in the interface memory is the Data Buffer (DBUFF). The modem and host synchronize parallel data transfer by observing the state of the Buffer 2 Available bit, BA2 (1E:3). RAM Access 2 is not available when the modem is in parallel data mode.

Receiving Parallel Data

In the parallel data mode (PDM=1), the modem writes to register DBUFF every eight bit times. The modem sets the BA2 bit when received data is available. The host resets the BA2 bit by reading DBUFF. After the modem sets BA2, the host must respond within eight bit times or else the modem writes over register DBUFF.

While receiving, if the energy drops below the turn-off threshold for a sufficient period of time, the modem writes the last bits of received data to register DBUFF before terminating the receive process.

The modem writes the first bit of received data to the least significant bit of register DBUFF, and writes the last bit of received data to the most significant bit of register DBUFF.

Transmitting Parallel Data

The modem reads register DBUFF every eight bit times when transmitting. The modem sets the BA2 bit when requesting transmit data. The host resets the BA2 bit by writing to DBUFF. After the modem sets BA2, the host must respond within eight bit times or else the modem retransmits the data in register DBUFF.

If RTSP bit is reset, or SETUP bit is set while transmitting, the modem sends all of the data previously read from register DBUFF before terminating the transmit process.

The modem transmits the least significant bit of register DBUFF first, and transmits the most significant bit of register DBUFF last.

The flowchart shown in Figure 3-2 may be used for parallel data transfer.

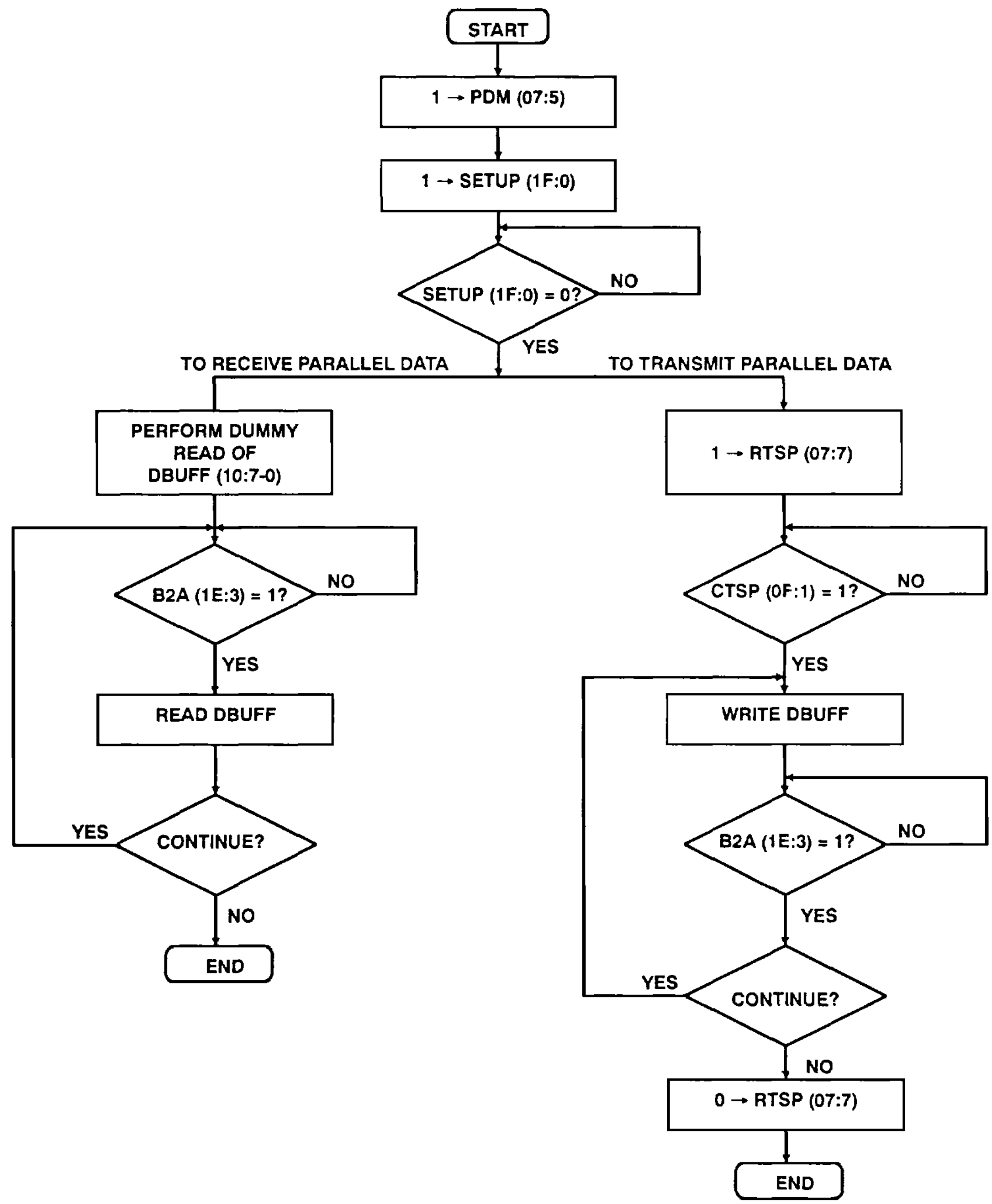


Figure 3-2. Parallel Data Transfer Routine

3.2.2 Programmable Interrupt Feature

The interface memory interrupt feature enables the host to select an interrupt to occur on any combination of bits within an interface memory register.

Programmable Interrupt Bits

The programmable interrupt routine runs at the sample rate in all transmit and receive modes. If the host sets the Programmable Interrupt Enable bit, PIE (1F:4), the modem sets the Programmable Interrupt Active bit, PIA (1F:7), and $\overline{\text{IRQ}}$ goes low when the interrupt condition is true. The Programmable Interrupt Request bit, PIREQ (1F:3), is set by the modem whenever the interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem is unable to reset this bit.

An interrupt may occur only within a single interface memory register based upon any combination of bits. For example, the host may select register 09h and generate an interrupt whenever bits 09:7, 09:4, and/or 09:3 are set, but may not select bits 08:7 and 09:2 to generate an interrupt. The register is selected by specifying the Interrupt Address, ITADRS (0A:0-4). (See ITADRS in Table 3-1.)

The Interrupt Bit Mask register, ITBMSK (0B:0-7), selects the bits to be tested in the interface memory register specified by ITADRS. For example, if ITBMSK is equal to FFh, all the bits are selected; if ITBMSK is equal to 0Fh, the four least significant bits are selected.

Programmable Interrupt Operating Modes

There are two operating modes (AND or OR) with each mode having four trigger options. The ANDOR bit selects the operating mode. The TRIG bits (0A:6-7) select the triggering option. (See ANDOR and TRIG bits in Table 3-1 for detail definition).

3.2.3 Voice Mode Operation

Voice Mode Transmitter (VMTX)
This mode allows the transmission of audio signals. Voice Mode Transmitter (VMTX) is entered when the configuration code is 82h, and the RTSP bit is set.

NOTE: The $\overline{RTS}$ hardware input signal can be asserted (low = true) or negated (high = false) instead of the RTSP bit set (1) or reset (0), respectively, whenever the RTSP bit state is specified.

The host must disable RAM Access 1 (i.e., reset ACC1 to a 0). The value in register 00 is sent to the D/A converter for transmission. The modem sets the Buffer 1 Available bit (BA1) every sample time to indicate that the value in register 00 has been transmitted. The BA1 bit is reset when the host writes the next byte.

Voice Mode Receiver (VMRX)
This mode allows the recording of audio signals. Voice Mode Receiver (VMRX) is entered when the configuration code is 82h and the RTSP bit is reset.

DSP RAM location ADCFLP is selected by the host for voice sample reception (see Section 4.2 and Table 4-1). The host reads the 8-bit A/D sample from register 00 using the ADCFLP access code. Reading the A/D sample simultaneously resets the BA1 bit.

In this mode, all tone detectors are functional. The slew rate is set to zero upon entering this configuration. After configuring the modem, the host must immediately write an AGC Slew Rate to DSP RAM. The AGC gain may be changed by writing to the AGC Gain Word and the maximum AGC gain may be changed by writing to the Receiver Sensitivity (MAXG). Also, the AGC slew rate is not changed in order to prevent clicking from being recorded. (See parameters 5, 6, and 21 in Section 4.2).

The voice mode can be set up for a different sampling rate than the default 9600 Hz.

The major steps required to perform voice mode recording and playback are described below.

Host Voice Mode Record Message Steps

General Procedure

1. Configure modem to Voice Mode Receiver (VMRX).
2. Change the sampling rate if other than 9600 Hz.
3. Designate AGC parameters.
4. RAM access read of 8-bit A/D samples.
5. Restore sample rate COUNTER1 prior to setting SETUP or setting RTSP.

Detail Procedure

1. Configure modem to VMRX. For the R96VFX, if the host sets bit FRZSL, VMRX may be implemented with the ADPCM Coder/Decoder configurations (i.e., CONF=9xh).

bit 07:5 = 0	PDM = 0 to allow RAM access 2.
bits 06:0-7 = 82h	CONF = 82h for VMRX.
bit 1F:0 = 1	Set SETUP on.
wait for bit 1F:0 = 0	Wait for SETUP off.

2. Change the sampling rate if other than 9600 Hz.

NOTE: If CONF = 9xh, set COUNTR1 to x3D0h (rather than x3D3h as shown for CONF = 8xh).

bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 2Bh	ADD2 = 2Bh for sample rate COUNTER1.
bits 11:0-7 = x3h	COUNTER1 MSB = x3h.
bits 10:0-7 = D3h	COUNTER1 LSB = D3h, reset BA2 off.
bits 15:0-7 = 8Ah	ACC2, IO2, and WRT2 on; BR2 and CR2 off.
wait for bit 1E:3 = 1	Wait for BA2 on. (COUNTER1= x3D3h)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 28h	ADD2 = 28h for sample rate COUNTER2.
bits 11:0-7 = xxh	COUNTER2 MSB = xxh.
bits 10:0-7 = xxh	COUNTER2 LSB = xxh, reset BA2 off.
bits 15:0-7 = 8Ah	ACC2, IO2, and WRT2 on; BR2 and CR2 off.
wait for bit 1E:3 = 1	Wait for BA2 on. (COUNTER2= xxxxh)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.

3. Designate AGC parameters.

bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 24h	ADD2 = 24h for Maximum Gain.
bits 11:0-7 = xxh	Maximum Gain MSB = xxh.
bits 10:0-7 = xxh	Maximum Gain LSB = xxh, reset BA2 off.
bits 15:0-7 = 83h	ACC2, WRT2, and CR2 on; IO2 and BR2 off.

wait for bit 1E:3 = 1	Wait for BA2 on. (Maximum Gain = xxxxh)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 15h	ADD2 = 15h for AGC Gain Word.
bits 11:0-7 = xxh	AGC Gain Word MSB = xxh.
bits 10:0-7 = xxh	AGC Gain Word LSB = xxh, reset BA2 off.
bits 15:0-7 = 83h	ACC2, WRT2, and CR2 on; IO2 and BR2 off.
wait for bit 1E:3 = 1	Wait for BA2 on. (AGC Gain Word = xxxxh)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 95h	ADD2 = 95h for AGC Slew Rate.
bits 11:0-7 = xxh	AGC Slew Rate MSB = xxh.
bits 10:0-7 = xxh	AGC Slew Rate LSB = xxh; reset BA2 off.
bits 15:0-7 = 82h	ACC2 and WRT2 on; IO2, BR2, and CR2 off.
wait for bit 1E:3 = 1	Wait for BA2 on. (AGC Slew Rate = xxxxh)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.

4. RAM access read of 8-bit A/D samples.

bits 05:0-7 = 00h	ACC1, IO1, BR1, WRT1, and CR1 off.
bits 04:0-7 = A0h	ADD1 = A0h for 8-bit A/D samples.
bits 05:0-7 = 80h	ACC1 on; IO1, BR1, WRT1, and CR1 off.
read bits 00:0-7	Reset BA1 off.
wait for bit 1E:0 = 1	Wait for BA1 on.
read bits 00:0-7	Read first 8-bit A/D sample.
:	:
wait for bit 1E:0 = 1	Wait for BA1 on.
read bits 00:0-7	Read last 8-bit A/D sample.
bits 05:0-7 = 00h	ACC1, IO1, BR1, WRT1, and CR1 off.

5. Restore sample rate COUNTER1 prior to setting bit SETUP or bit RTSP.

bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 2Bh	ADD2 = 2Bh for COUNTER1.
bits 11:0-7 = A3h	COUNTER1 MSB = A3h.
bits 10:0-7 = D3h	COUNTER1 LSB = D3h, reset BA2 off.
bits 15:0-7 = 8Ah	ACC2, IO2, and WRT2 on; BR2 and CR2 off.
wait for bit 1E:3 = 1	Wait for BA2 on. (COUNTER1= A3D3h)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.

Host Voice Mode Playback Message Steps

General Procedure

1. Configure modem to Voice Mode Receiver (VMRX).
2. Set RTSP to enter Voice Mode Transmitter (VMTX).
3. Change the sampling rate if other than 9600 Hz.
4. RAM access write of 8-bit D/A samples.
5. Restore sample rate COUNTER1 if sample rate is not 9600 Hz.
6. Reset RTSP off.

Detail Procedure

1. Configure modem to Voice Mode Receiver (VMRX).

bit 07:5 = 0	PDM = 0 to allow RAM access 2.
bits 06:0-7 = 82h	CONF = 82h for VMRX.
bit 1F:0 = 1	Set SETUP on.
wait for bit 1F:0 = 0	Wait for SETUP off.

2. Set RTSP to enter Voice Mode Transmitter (VMTX).

bit 05:7 = 0	ACC1 = 0 to disable RAM Access 1.
bits 00:0-7 = 00h	VMTX D/A samples = 00h.
bit 07:7 = 1	RTSP on.
wait for bit 0D:7 = 0	Wait for RX bit off indicating Voice Mode TX.

3. Change the sampling rate if other than 9600 Hz.

bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 2Bh	ADD2 = 2Bh for sample rate COUNTER1.
bits 11:0-7 = x3h	COUNTER1 MSB = x3h.
bits 10:0-7 = D3h	COUNTER1 LSB = D3h, reset BA2 off.
bits 15:0-7 = 8Ah	ACC2, IO2, and WRT2 on; BR2 and CR2 off.

wait for bit 1E:3 = 1	Wait for BA2 on. (COUNTER1= x3D3h)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 28h	ADD2 = 28h for sample rate COUNTER2.
bits 11:0-7 = xxh	COUNTER2 MSB = xxh.
bits 10:0-7 = xxh	COUNTER2 LSB = xxh, reset BA2 off.
bits 15:0-7 = 8Ah	ACC2, IO2, and WRT2 on; BR2 and CR2 off.
wait for bit 1E:3 = 1	Wait for BA2 on. (COUNTER2= xxxxh)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.

4. RAM access write of 8-bit D/A samples.

wait for bit 1E:0 = 1	Wait for BA1 on.
write bits 00:0-7	Write next TX sample and reset BA1 off.
.	.
.	.
wait for bit 1E:0 = 1	Wait for BA1 on.
bits 00:0-7 = 00h	Write last TX sample and reset BA1 off.

5. Restore sample rate COUNTER1.

bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.
bits 14:0-7 = 2Bh	ADD2 = 2Bh for COUNTER1.
bits 11:0-7 = A3h	COUNTER1 MSB = A3h.
bits 10:0-7 = D3h	COUNTER1 LSB = D3h, set BA2 off.
bits 15:0-7 = 8Ah	ACC2, IO2, and WRT2 on; BR2 and CR2 off.
wait for bit 1E:3 = 1	Wait for BA2 on. (COUNTER1= A3D3h)
bits 15:0-7 = 00h	ACC2, IO2, BR2, WRT2, and CR2 off.

6. Set RTSP.

bit 07:7 = 0	RTSP off.
wait for bit 0D:7=1	Wait for RX bit on for Voice Mode RX.

Voice Mode Application Notes

1. To remove any DC offset voltage that may be present at the transmitter output, an AC coupling 0.1 μF capacitor (20%, 50V) may be placed in series between the modem's TXOUT pin (QUIP pin no. 28, PLCC pin no. 34) and resistor R7 (34.8K ohms) in Figures 12-1 and 12-2.
2. When using the Voice Mode Receiver with prerecorded speech signals as input, the host should record these signals such that the peak voltage is 2.8V when measured at the modem's RXA input.
3. RAM access 1 must be disabled in the Voice Mode Transmitter. Use RAM access 2 for all RAM/IO read/write operations.
4. When changing the sample rate, always write to sample rate COUNTER1 before writing to sample rate COUNTER2 (see parameterss 43 and 44 in Section 4.2).
5. When the host sets bit SETUP or changes RTSP from off-to-on or on-to-off, parameters Maximum Gain, AGC Slew Rate, and AGC Gain Word assume their default values.

Selected Parameter Values

1. AGC Slew Rate.

   0008h represents slow AGC adaptation.

2. Maximum Gain and AGC Gain Word.

   72CCh represents 5 dB.
   660Ah represents 10 dB.
   4C88h represents 20 dB.
   3305h represents 30 dB.

3. Selected sample rates for R96MFX, R96EFX, and R96DFX.

Sample Rate	COUNTER1	COUNTER2
9600 Hz	A3D3h	1340h
8000 Hz	23D3h	E560h
7000 Hz	23D3h	C8B4h
6000 Hz	23D3h	AC0Bh

   Default sample rate is 9600 Hz.

4. Selected sample rates for R96VFX.

Sample Rate	COUNTER1	COUNTER2
9600 Hz	23D3h	FA3Bh
8000 Hz	23D3h	D087h
7000 Hz	23D3h	B676h
6000 Hz	23D3h	9C65h

   Default sample rate is 9600 Hz.

3.2.4 FSK/DTMF Receiver

Mode Selection and Description

Configuration code 21h enables the DTMF receiver to operate concurrently with the FSK receiver and the three tone detectors. Configuration code 9xh, with control bit DFMFE set, enables the DTMF receiver to operate concurrently with the ADPCM codec, three tone detectors, and FSK flag pattern (7E) detector. The encoded DTMF receiver output is written into the four least significant bits of register 1Ch.

The modem sets the DTMF Signal Detected status bit, DTMFD (1Ch:4), whenever a DTMF signal is successfully detected. The host must reset DTMFD after reading the register, otherwise, two or more successive detections of the same symbol may go unnoticed.

Other DTMF Reception Status Bits

Other status bits have been included in register 1Ch to facilitate host DTMF detection, primarily when used with the programmable interrupt. The Early Detection bit, EDET (1Ch:7), may set approximately 20 ms after signal energy is detected. Setting this bit informs the host that the received signal appears to be a DTMF signal, but the modem has not yet completed its processing.

The Dual Tone Detected bit, DTDET (1Ch:6), may set approximately 11 ms following EDET setting. DTDET is set when the received signal satisfies all DTMF criteria except on-time, off-time, and cycle-time. At this time the encoded DTMF receiver output is made available to the host in the DTMF Output Word (1Ch:0-3). If DTDET is not set, then the received signal has failed one or more criteria, and consequently the modem resets EDET and resumes its search.

After the on-time criteria is satisfied, the modem sets the On-Time Satisfied bit, OTS (1Ch:5). If the on-time is not satisfied, the modem resets bits EDET and DTDET and resumes its search. As soon as both the off-time and cycle-time are satisfied, DTMFD is set. If these times are not satisfied, then EDET, DTDET, and OTS are reset and the receiver resumes its search. Also following DTMFD setting, EDET, DTDET, and OTS are reset. The relationship between these status bits for a valid DTMF signal is illustrated in Figure 3-3.

If, after DTDET is set, the host resets DTDET before OTS sets, then the FSK/DTMF receiver is reset to its initial state except for the programmable DTMF parameters which retain their present values (see Section 4.2).

If, after OTS is set, the host resets OTS before DTMFD sets, then the FSK/DTMF receiver is reset to its initial state except for the programmable DTMF parameters which retain their present values (see Section 4.2).

See Table 13-1 for DTMF receiver performance characteristics.

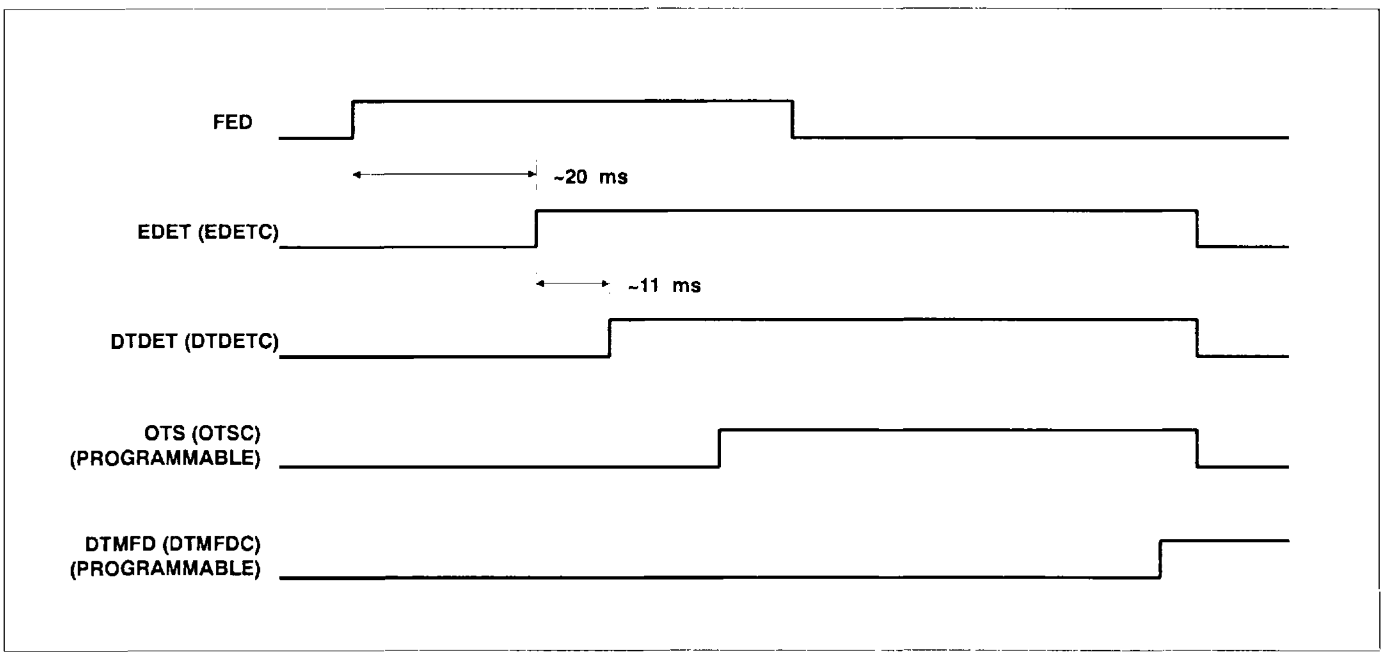


Figure 3-3. DTMF Receiver Status Bit Timing

3.2.5 FSK Flag Pattern (7E) Detector

In the R96VFX, the FSK flag pattern (7E) detector may be used to detect the presence of the T.30 FSK 7E flag preamble while the modem is configured in any ADPCM mode or high speed receiver mode other than short train (configuration codes 0xh, 1xh, and 9xh). Control bit FSKFLS and status bit FSK7E characterize the detection process (see Table 3-1 for bit descriptions).

In the high speed receiver configurations, the detection process will always start after the modem enters its receiver idle mode and a waiting period of 8 bauds after FED turns on (see Figure 3-4). The modem receiver normally enters the idle mode after any of the following events:

1. The host setting of SETUP bit.
2. After FED turns off with enough lapse time in data mode to return to the idle mode (approximately 30 ms in V.29).
3. After the modem detects a significant gain hit in the data mode (CDET on). The presence of an FSK signal when noise is above turn-on threshold will generate such a hit.

After the modem enters the idle mode, the modem will reset FSKFLS and FSK7E bits. If FED is on, then the modem will set FSKFLS and start the detection process. After the completion of the detection process, if the FSK 7E signal is present the modem will set FSK7E bit and reset the FSKFLS bit. The FSK7E bit will remain at this state until the modem enters the idle mode again or the host resets the bit.

The detector will not work properly if the modem is not allowed to complete the detection process, which lasts about 106.67 ms after FSKFLS is set.

In the event that the host sets the control bit TDIS after the modem enters its idle mode, the modem will quickly enter the data mode after FED turns on and, hence, not allow enough time for the detector to complete its detection process. Therefore, the TDIS bit must be reset to assure the proper function of the detector.

A simple example usage of the FSK flag pattern (7E) detector in a high speed receiver signal recognition algorithm is illustrated Figure 9-28.

When the modem is configured for the ADPCM mode, bit FSKFLS is set and the FSK flag pattern (7E) detector is enabled. When bit FSKFLS is set the detector runs continuously, and when it is reset the detector is disabled. When the detector completes its search bit FSKFLS is not reset as is the case in the high speed receiver. Bit FSK7E is set if the flag pattern is detected. The host must reset bit FSK7E to detect the next occurrence of FSK flag pattern.

3.2.6 High Speed Timing

Several status bits in the DSP interface memory are useful to the host for monitoring various receiver conditions. These bits are significant during training and data reception/transmission. Figure 3-5 illustrates the timing relationships between these bits.

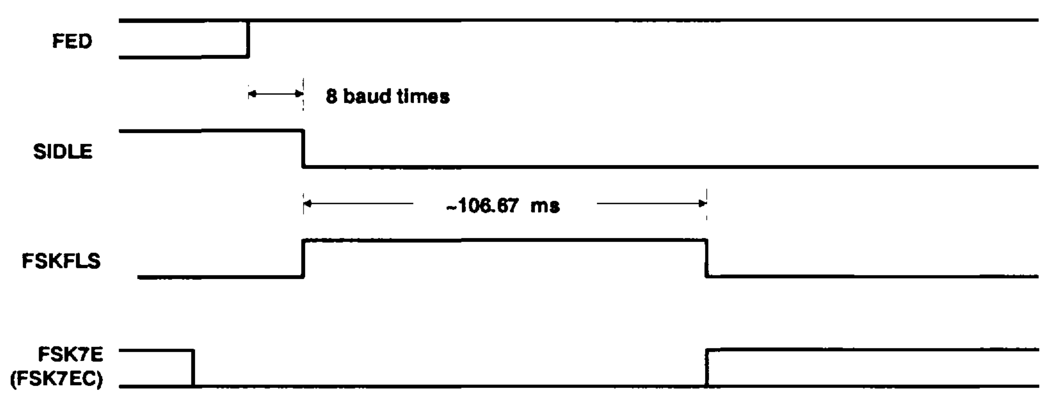
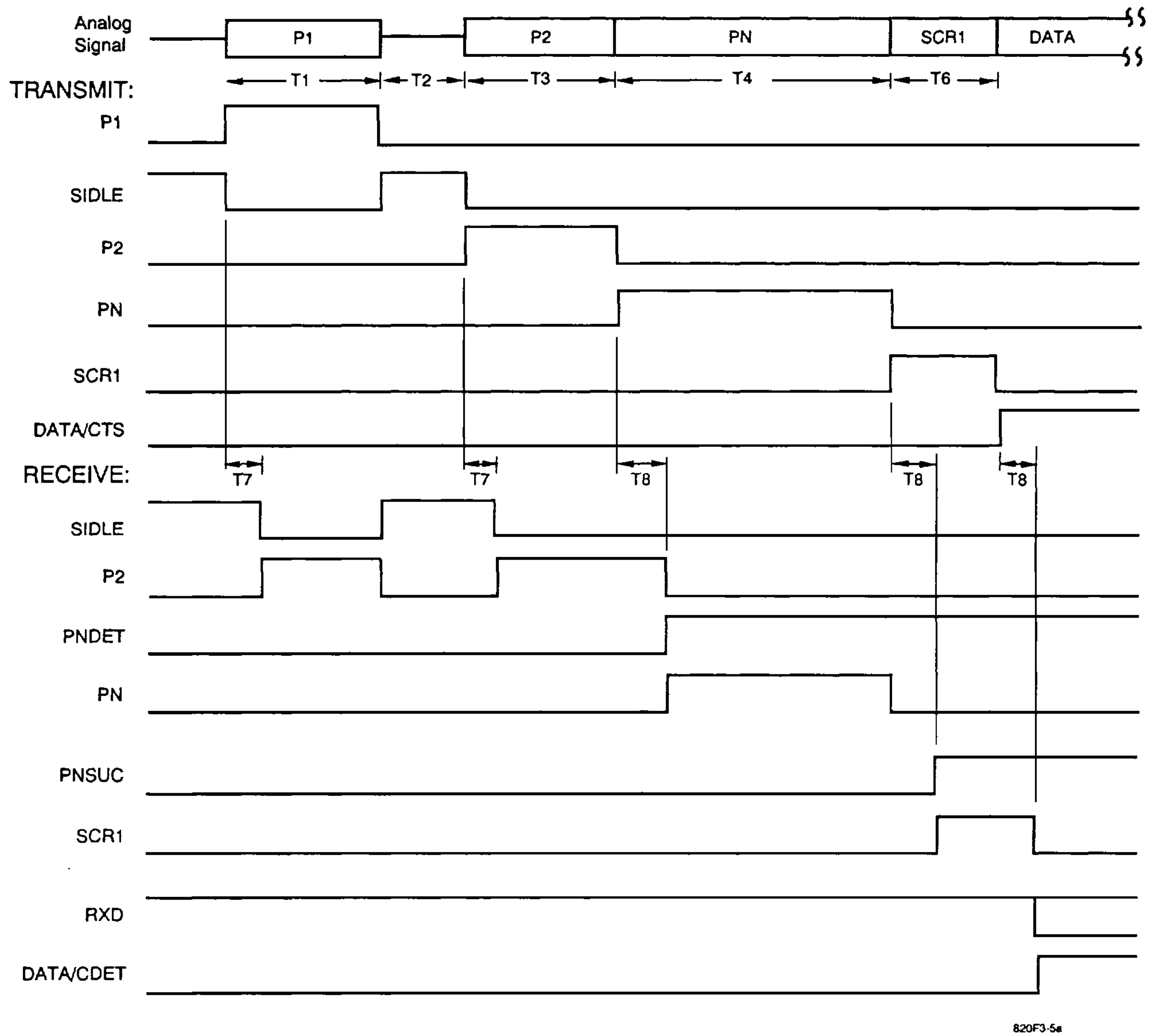
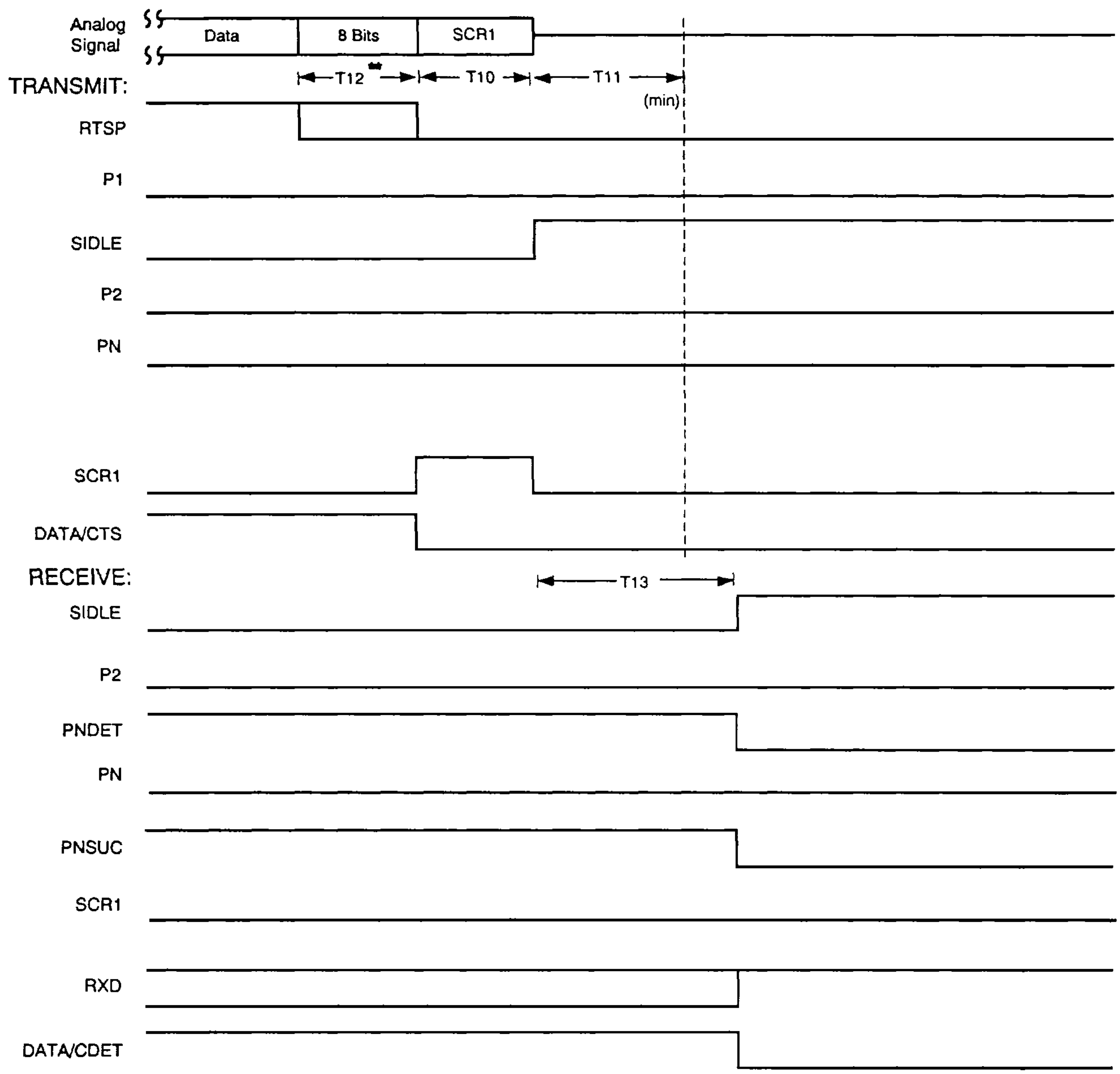


Figure 3-4. FSK 7E Flag Detector Timing



Mode	T1	T2	T3	T4	T6	T7	T8	Units
V.29	187.5	20	53.3	160.0	20.0	3.3	4.2	ms
V.29 Short Train	187.5	20	41.6	25.8	7.5	1.3	4.2	ms
V.27 ter, 4800 Long	187.5	20	31.2	671.0	5.0	5.0	6.3	ms
V.27 ter, 2400 Long	187.5	20	41.6	895.0	6.6	6.6	8.3	ms
V.27 ter, 4800 Short	187.5	20	8.8	36.3	5.0	1.9	6.3	ms
V.27 ter, 2400 Short	187.5	20	11.7	48.3	6.6	2.5	8.3	ms
Test conditions: Back to back; no impairments.								

Figure 3-5. High Speed Mode Status Bit Timing



Mode	T10	T11*	T13	Units
V.29	5	20	34	ms
V.27 ter, 4800	7	20	19	ms
V.27 ter, 2400	10	20	24	ms

* 140 ms if SQEXT = 1.

** In parallel mode data mode with HDLC bit off, turning $\overline{RTS}$ off immediately after loading the last byte (see Section 3.2.1): T12 = 8 bit times.

In parallel mode data mode with HDLC bit on, turning $\overline{RTS}$ off immediately after loading the last byte (see Section 5): T12 = 32 bit times (max.) if NFLAG = 0 (see Parameter 39 in Section 42.)

Figure 3-5. High Speed Mode Status Bit Timing (Cont'd)

3.2.7 Power-on/Reset DSP Test Mode

After Power-on or Reset, the modem enters into a test mode and calculates checksums on ROM, RAM and multiplier sections. The results of the checksums and ASCII values corresponding to the DSP device part number and code revision letter are written to the interface memory registers 10h through 1Bh approximately 10 ms after Power-on/Reset signal goes off. The contents will remain in these registers for about 5 ms or until register 10 is read by the host. Typical checksum and device part number values are listed in Table 3-2.

Table 3-2. Power-On Reset Self-Test Values

Contents	Register	R96MFX	R96EFX	R96DFX	R96VFX
Multiplier checksum upper word	1B	7B	7B	7B	7B
Multiplier checksum lower word	1A	11	11	11	11
RAM2 checksum upper word	19	81	81	81	53
RAM2 checksum lower word	18	28	28	28	09
RAM1 checksum upper word	17	B7	B7	B7	29
RAM1 checksum lower word	16	E0	E0	E0	9D
ROM checksum upper word	15	DA	DA	DA	41
ROM checksum lower word	14	DD	DD	DD	2B
DSP device upper number ASCII	13	30	30	30	31
DSP device lower number ASCII	12	30	31	33	34
ASCII value for " "	11	20	20	20	20
DSP device code revision number (Example shown = "A")	10	41	41	41	41

4 DSP RAM ACCESS

The modem DSP contains 16-bit words of random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

4.1 INTERFACE MEMORY ACCESS TO DSP RAM

The interface memory acts as an intermediary during host to DSP RAM, or DSP RAM to host, data exchanges. The address stored in DSP interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud or sample time, as selected by the BRx (x = 1 or 2) bit. The baud rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz for every mode except Group 2 (where it is 10368 Hz), voice mode, and ADPCM.

Two RAM Access bits in the DSP interface memory tell the DSP to access the X RAM and/or Y RAM. The transfer is initiated by the host setting the ACC1 and/or the ACC2 bit(s). The DSP tests these bits each baud or sample period.

4.1.1 Host Programmable Data

The DSP RAM access functions, codes, and registers are identified in Table 4-12. The parameter scaling is described in Section 4.2.

4.1.2 Host DSP Read and Write Procedures

The modem main RAM has four RAM banks: Data RAM Real, Data RAM Imaginary, Coefficient RAM Real, and Coefficient RAM Imaginary. The designation (x = 1, 2) indicates x may be replaced by either 1 or 2, with 1 and 2 referring to RAM Access 1 and 2, respectively. To access the main RAM, write the desired RAM access code into ADDx (x = 1, 2). Bits 0 through 6 of the access code specify the RAM location and bit 7 of the access code specifies a real (0) or imaginary (1) RAM location. The CRx (x = 1, 2) bit controls whether the coefficient RAM (1) or data RAM (0) is accessed. The BRx (x = 1, 2) bit controls whether the data is accessed at the baud rate (1) or the sample rate (0) (configurations 0x and 1x only).

If parallel data mode is selected (PDM = 1), with or without HDLC mode (HDLC = 1), RAM access associated with RAM Address 2 (RAM Access 2) is disabled and only RAM access associated with RAM Address 1 is available.

DSP RAM Read Procedure

The RAM read procedure is a 32-bit transfer from DSP RAM to the interface memory which transfers both the X RAM and Y RAM simultaneously. Figure 4-1 shows the read procedure flow chart.

1. Before reading from DSP interface memory, reset ACC1 and/or ACC2, then reset BA1 or BA2 by reading YDAL1 or YDAL2.
2. Reset WRT1 and/or WRT2 to inform the DSP that a RAM read will occur when ACC1 and/or ACC2 is set.
3. Load the RAM address into RAM Address 1 and/or RAM Address 2, then set CR1, BR1, and IO1 and/or CR2, BR2, and IO2 to desired values.
4. Set ACC1 and/or ACC2 to signal the DSP to perform the RAM read.
5. When the DSP has transferred the contents of RAM into the interface memory RAM Data registers, BA1 and/or BA2 will be set.
6. If IE1 and/or the IE2 is set, $\overline{IRQ}$ is also asserted when BA1 and/or BA2 set by the DSP. When $\overline{IRQ}$ is asserted, IA1 and/or IA2 is set to inform the host that setting of BA1 and/or BA2 was the cause.
7. Read XDAM1, XDAL1, YDAM1, AND YDAL1; and/or XDAM2, XDAL2, YDAM2, AND YDAL2; in this order. Note that reading YDAL1 resets IA1 and/or reading YDAL2 resets IA2 which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

DSP RAM Write Procedure

The RAM write procedure is a 16-bit transfer from interface memory to DSP RAM allowing the transfer of X RAM data or Y RAM data to occur each baud or sample time. Figure 4-2 shows the write procedure flow chart.

1. Before writing to DSP interface memory, reset ACC1 and/or ACC2; then reset BA1 or BA2 by reading YDAL1 or YDAL2, respectively.
2. Load the RAM address into RAM Address 1 and/or RAM Address 2, then set CR1, BR1, and IO1 and/or CR2, BR2, and IO2 to the desired values.
3. Set WRT1 and/or WRT2 to inform the DSP that a RAM write will occur when ACC1 and/or ACC2 is set.
4. Write the desired data into the interface memory RAM Data registers YDAL1 and YDAM1 and/or YDAL2 and YDAM2.
5. Set ACC1 and/or ACC2 to signal the DSP to perform the RAM write.
6. When the DSP has transferred the contents of the interface memory RAM Data registers into RAM, BA1 and/or BA2 will be set.
7. If IE1 and/or IE2 is set, $\overline{IRQ}$ is also asserted and IA1 and/or IA2 is set when BA1 and/or BA2 is set.
8. Reset IA1 and/or IA2 by writing to YDAL1 and/or YDAL2, which causes $\overline{IRQ}$ to return high if no other interrupt requests are pending.

Table 4-1. Modem DSP RAM Parameter Access Codes

No.	Function	BRx	CRx	IOx	ADDx	Read Reg. No.
1	Received Signal Samples	0	0	0	15	2,3
2	Received Signal Samples (Voice Mode)	0	0	0	A0	0
3	Received Signal Sample FSK[5]	0	0	0	31	2,3
4	Average Energy	0	0	0	14	2,3
5	AGC Gain Word	0	1	0	15	2,3
6	AGC Slew Rate Word	0	0	0	95	0,1
7	Tone 1 Frequency	0	1	0	21	2,3
8	Tone 1 Transmit Output Level	0	0	0	22	2,3
9	Tone 2 Frequency	0	1	0	22	2,3
10	Tone 2 Transmit Output Level	0	0	0	23	2,3
11	Transmit Output Level/Scaling	0	0	0	21	2,3
12	Equalizer Tap Coefficients[2]	1	1	0	3A - 61[1] 3A - 69[6]	0,1,2,3
13	Rotated Equalizer Output, Eye Pattern	1	1	0	17	0,1,2,3
14	Decision Points, Ideal	1	0	0	17	0,1,2,3
15	Error Vector	1	1	0	1D	0,1,2,3
16	Rotation Angle	1	1	0	0C	0,1
17	Frequency Correction	1	1	0	18	2,3
18	Eye Quality Monitor, EQM	1	1	0	0D	2,3
19	RLSD Turn-on Threshold	0	1	0	37	2,3
20	RLSD Turn-off Threshold	0	1	0	B7	0,1
21	Receiver Sensitivity, MAXG	0	1	0	24	2,3
22	Group 2 PLL Frequency Correction[3]	0	0	0	0D	2,3
23	Group 2 PLL Slew Rate[3]	0	0	0	18	2,3
24	Group 2 Zero Crossing Threshold, Negative[3]	0	0	0	19	2,3
25	Group 2 Zero Crossing Threshold, Positive[3]	0	0	0	99	0,1
26	Group 2 AGC Slew Rate[3]	0	1	0	05	2,3
27	Group 2 Black-White Threshold[3]	0	0	0	24	2,3
28	Group 2 Phase Limit[3]	0	0	0	1A	2,3
29	Minimum On Time (DTMF)[4]	0	1	0	1F	2,3
30	Minimum Off Time (DTMF)[4]	0	0	0	1F	2,3
31	Minimum Cycle Time (DTMF)[4]	0	0	0	9F	0,1
32	Maximum Dropout Time (DTMF)[4]	0	1	0	9F	0,1
33	Maximum Speech Energy (DTMF)[4]	0	1	0	1E	2,3
34	Frequency Deviation, Low Group (DTMF)[4]	0	0	0	1D	2,3
35	Frequency Deviation, High Group (DTMF)[4]	0	1	0	1D	2,3

Table 4-1. Modem DSP RAM Parameter Access Codes (Cont'd)

No.	Function	BRx	CRx	IOx	ADDx	Read Reg. No.
36	Negative Twist Control (DTMF)[4]	0	0	0	1E	2,3
37	Positive Twist Control (DTMF)[4]	0	0	0	9E	0,1
38	Maximum Energy Hit Time (DTMF)[6]	0	1	0	A3	0,1
39	Number of Additional Flags, NFLAG (HDLC)	0	1	0	85	0,1
40	FR1 Tone Detector Coefficients	0	1	0	25-2A	2,3
	FR1 Tone Detector Coefficients	0	1	0	A5-AA	0,1
41	FR2 Tone Detector Coefficients	0	1	0	2B-30	2,3
	FR2 Tone Detector Coefficients	0	1	0	AB-B0	0,1
42	FR3 Tone Detector Coefficients	0	1	0	31-36	2,3
	FR3 Tone Detector Coefficients	0	1	0	B1-B6	0,1
43	Sample Rate Counter 1, Most Significant Bit	0	0	1	2B	0,1
44	Sample Rate Counter 2, Least Significant Word	0	0	1	28	0,1
45	Decoder Reconstructed Speech Samples (ADPCM)[6]	0	0	0	5C	2,3
46	ADC Speech Sample Scaling Parameter (ADPCM)[6]	0	1	0	B9	0,1
47	Host ADC Speech Sample Scaling Parameter (ADPCM)[6]	0	1	0	BA	0,1
48	Host ADC Speech Sample (ADPCM)[6]	0	0	0	39	2,3
49	Sample Rate ROM Table Pointer, ROMPNT (ADPCM)[6]	0	1	0	39	2,3
50	White Noise Output Scaling Parameter, RANOISE (ADPCM)[6]	0	1	0	74	2,3
51	Minimum Silence Magnitude Threshold, MTHRESH (ADPCM)[6]	0	1	0	75	2,3
52	Detecting Silence in Speech Parameter, SILSPE (ADPCM)[6]	0	1	0	F6	0,1
53	Detecting Speech in Silence Parameter, SPESIL (ADPCM)[6]	0	1	0	F7	0,1
54	Minimum Silence Magnitude Adaptation Parameter, MADAPT (ADPCM)[6]	0	1	0	F8	0,1
55	Maximum Gain, dBTHR (ADPCM)[6]	0	0	0	B8	0,1

Notes:

1. R96MFX R6628-13 and subsequent, and other 9600 bps MONOFAX modems.
2. Equalizer Tap Coefficient addresses (ADDx) for R96MFX 6628-12 device are 38-5F.
3. R96MFX and R96EFX only.
4. R96DFX and R96VFX only.
5. R96MFX R6628-12 and R96EFX R6631-12 devices only.
6. R96VFX only.

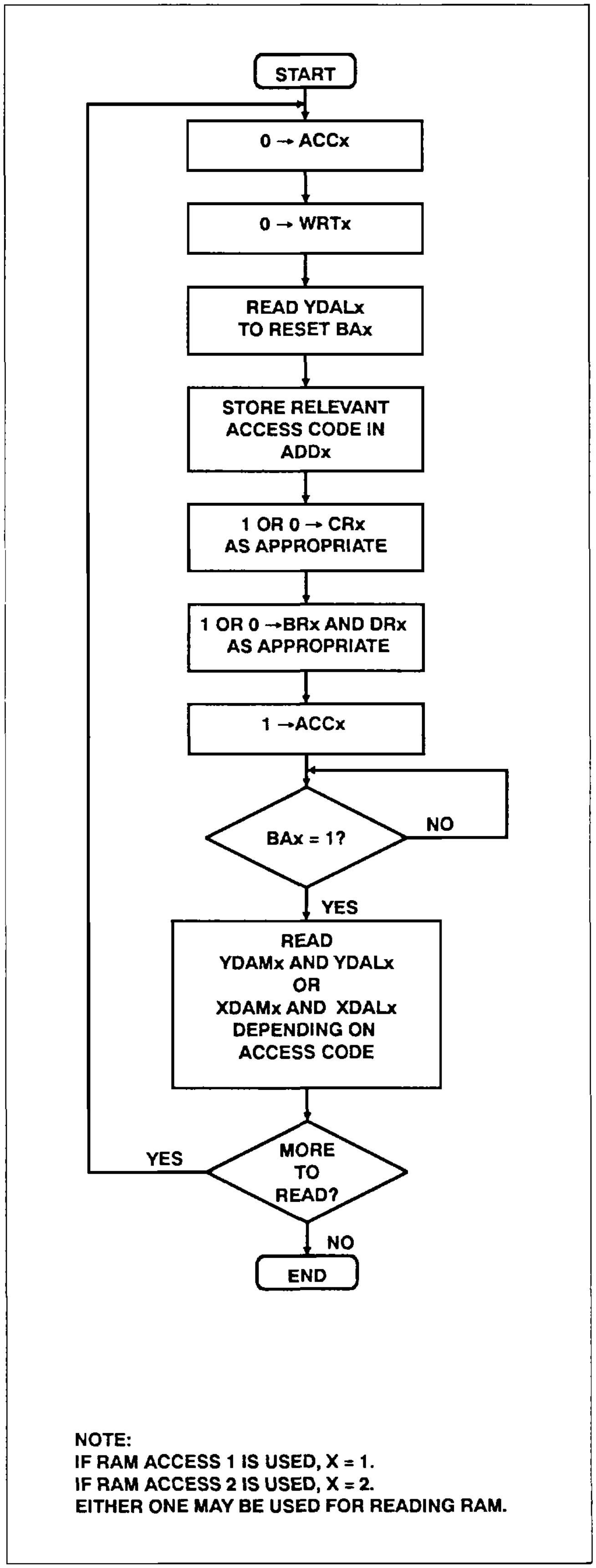


Figure 4-1. RAM Data Read Routine

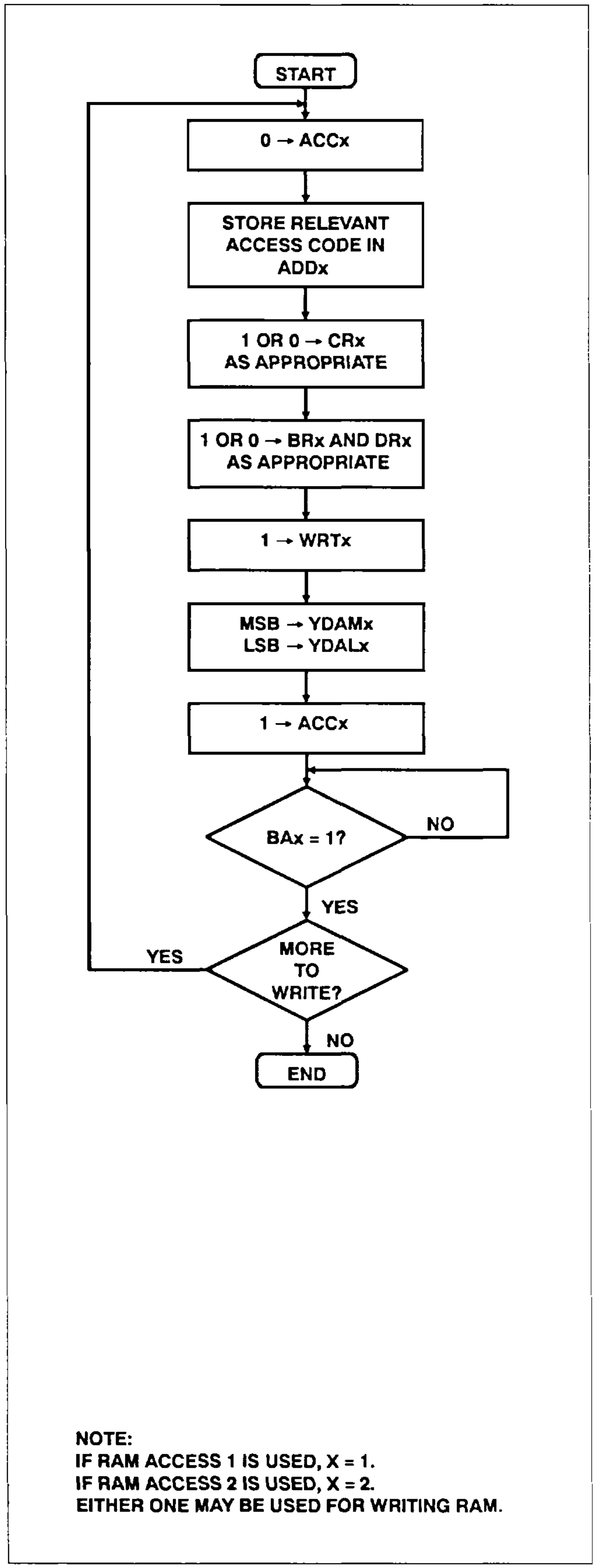


Figure 4-2. RAM Data Write Routine

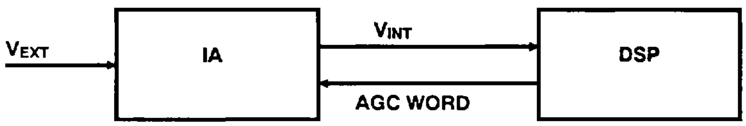
4.2 DSP RAM PARAMETER DEFINITIONS AND SCALING

No. 1 Received Signal Sample = A/D Sample Word
No. 3 Received Signal Sample FSK = A/D Sample Word

Format: 16 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word)h] x ($3.03/2^{15}$)

V_{EXT} = VINT + $LOG_{10}{-1}$ [AGC Gain (dB)/20]



No. 2 Received Signal Sample (Voice Mode) = A/D Sample Word

Format: 8 bits, signed, twos complement

Equation: V_{INT} (Volts)= [(A/D Sample Word)h] x ($3.03/2^{7}$)

V_{EXT} = V_{INT} + $LOG_{10}{-1}$ [AGC Gain (dB)/20]

No. 4 Average Energy

Format: 16 bits, twos complement, positive value

Equation: Post-AGC Average Power (dBm) = 10 Log [(Average Power Word)h/889h]

Pre-AGC Average Power (dBm) = Post-AGC Avg. Power in dBm - AGC gain in dB

Typical value: 0889h (corresponding to 0 dBm)

No. 5 AGC Gain Word

Format: 16 bits, unsigned

Equation: AGC Gain (dB) = 50[1 – (AGC Gain Word)h/2^{15}]

No. 6 AGC Slew Rate Word

Format: 16 bits, twos complement, positive value

The AGC Slew Rate Word can be approximated by the following equation.

Equation: AGC Slew Rate = [19968/(Sample Rate x AGC gain fall time constant in seconds)]h

Note: AGC gain tracks the input signal with an exponential function with respect to time, and its fall time is approximately 5 times faster than its rise time. The above equation was determined based upon a 40 dB change in input signal.

No. 7 Tone 1 Frequency
No. 9 Tone 2 Frequency

Format: 16 bits, unsigned

Equation: N = 2^{16}/Sample Rate x (Frequency in Hz) (Default Sample Rate = 9600 Hz)

Convert N to hexadecimal then store in RAM.

No. 8 Tone 1 Transmit Output Level
No. 10 Tone 2 Transmit Output Level

Format: 16 bits, twos complement, positive value

Calculate the transmit output level (power) of each tone independently by using the equation for Transmit Output Level (No. 11).

Convert these numbers to hexadecimal then store in RAM.

Total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.

No. 11 Transmit Output Level

Format: 16 bits, twos complement, positive value

Equation: Transmit Output Level = $18426\ [10^{(P_O/20)}]$

Where: P_O = output power in dBm with a 600 ohm load termination.
P_S = output power in dBm with a series 600 ohm resistor into a 600 ohm load ($P_S = P_O - 6$).

No. 11 ADPCM Decoder Output Scaling (ADPCM modes only)

Equation: Transmit Output Scaling = $2^{15}\ [10^{(P/20)}]$

Where: P = Scaling factor in dB.

Default: 0 dB (7FFFh)

Convert Transmit Output Level to hexadecimal and store in RAM.

No. 12 Equalizer Tap Coefficients

The equalizer tap coefficients can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers, they require two write operations per tap, one for the real part and one for the imaginary part.

Format: 16 bits, signed, twos complement, real
16 bits, signed, twos complement, imaginary

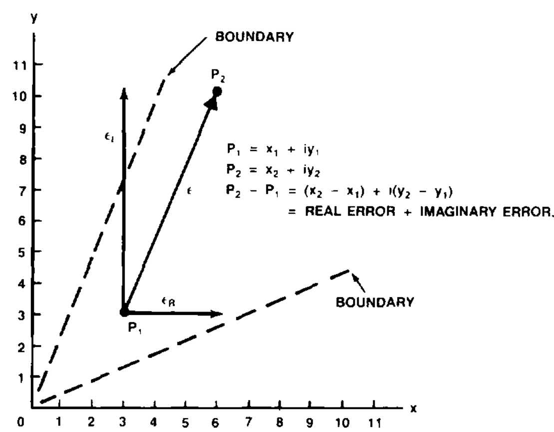
No. 13 Rotated Equalizer Output, Eye Pattern
No. 14 Decision Points, Ideal

Format: 16 bits, signed, twos complement, real
16 bits, signed, twos complement, imaginary

No. 15 Error Vector

Represents the difference between the received point (P2) and the nearest ideal point (P1).

Format: 16 bits, signed, twos complement, real
16 bits, signed, twos complement, imaginary



Error Vector Maximum Values

Configuration	Bit Rate (bps)	Registers 3 and 2 Real Error (Re)	Registers 1 and 0 Imaginary Error (Im)	Magnitude $\sqrt{(Re^2 + Im^2)}$
V.29	9600	< 0C00h	< 0C00h	< 0E66h
V.29	7200	< 2400h	< 2400h	< 1AD4h
V.29	4800	< 1C00h	< 1C00h	< 1C00h
V.27 ter	4800	< 1C00h	< 1C00h	< 1C00h
V.27 ter	2400	< 1C00h	< 1C00h	< 1C00h

No. 16 Rotation Angle

Represents instantaneous correction for phase and frequency errors.

Format: 16 bits, twos complement

Equation: Rotation Angle (degrees) = $[(\text{Rotation Angle Word})h/2^{16}] \times 180$ degrees

No. 17 Frequency Correction

Represents component of rotation angle caused by frequency error.

Format: 16 bits, twos complement

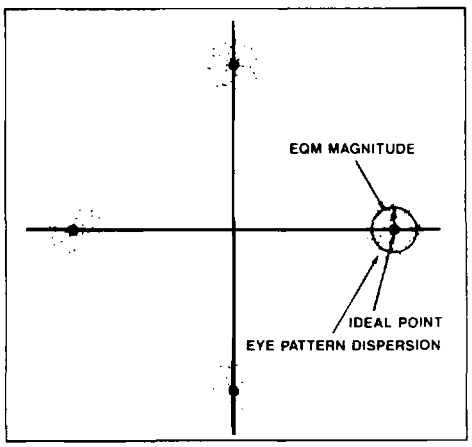
Range: FC00h to 0400h representing -37.5 Hz to +37.5 Hz

Equation: Frequency Correction (Hz) = $[(\text{Frequency Correction Word})h/2^{16}] \times$ Baud in Hz

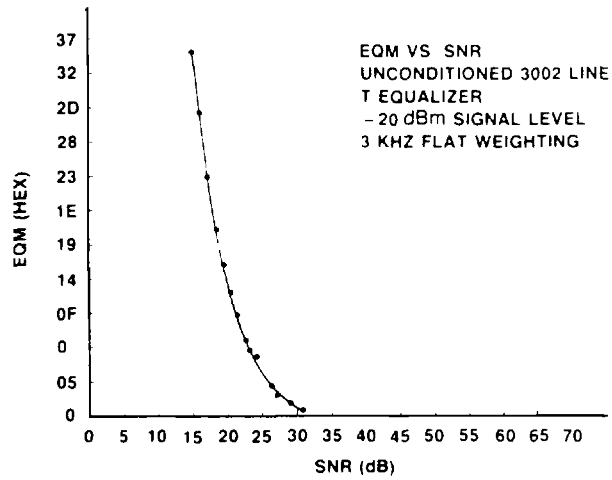
No. 18 Eye Quality Monitor, EQM

Equals the filtered squared magnitude of the error vector. Proportionality to bit error rate is determined by particular application. Stabilizes in approximately 700 baud times from RLSD going active.

Format: 16 bits, twos complement, positive value



Relationship of EQM to Eye Pattern



Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600

No. 19 RLSD Turn-On Threshold
No. 20 RLSD Turn-Off Threshold
No. 21 Receiver Sensitivity, MAXG

Three parameters can be programmed by the host to control the RLSD turn-on and turn-off thresholds: (1) Post-AGC Turn-on Threshold, (2) Post-AGC Turn-off Threshold, and (3) Receiver Sensitivity (MAXG) - AGC Gain Word Limit. Note that parameter dBTHR (No.55) specifies the maximum gain applied to the ADPCM coder input signal.

Format: 16 bits, twos complement, positive value

Equation: RLSD Turn-on Threshold = $2185\ [10^{(TON+MG)}]$

RLSD Turn-off Threshold = $2185\ [10^{(TOFF+MG)}]$

Receiver Sensitivity (MAXG) = 655.36 [50 - Gain Limit (dB)]

Where: TON is the turn-on threshold in dBm.
TOFF is the turn-off threshold in dBm.
$MG = 50[1 - (MAXG)h/2^{15}]/10$
MAXG is programmable in RAM and defaults to 0FC0h (4032).

No. 22 Group 2 PLL Frequency Correction

Format: 16 bits, twos complement

Range: FC6Ah to 0346h representing -140 Hz to +140 Hz

Equation: Frequency Correction (Hz) = (Frequency Correction Word)h x (0.167)

See Section 8.

No. 23 Group 2 PLL Slew Rate

Represents gain of first order term in phase locked loop. Directly proportional to PLL slew rate. See Section 8.

Format: 16 bits, twos complement, positive value

Default: 0800h

No. 24 Group 2 Zero Crossing Threshold, Negative
No. 25 Group 2 Zero Crossing Threshold, Positive

These two parameters represent limits on acceptable zero crossing for use by the carrier recovery loop. (See Section 8.)

Format: 16 bits, twos complement, positive value

Range: 0010h to 7000h for stable operation

Default: Negative Zero Crossing Threshold = 5000h
Positive Zero Crossing Threshold = 1480h

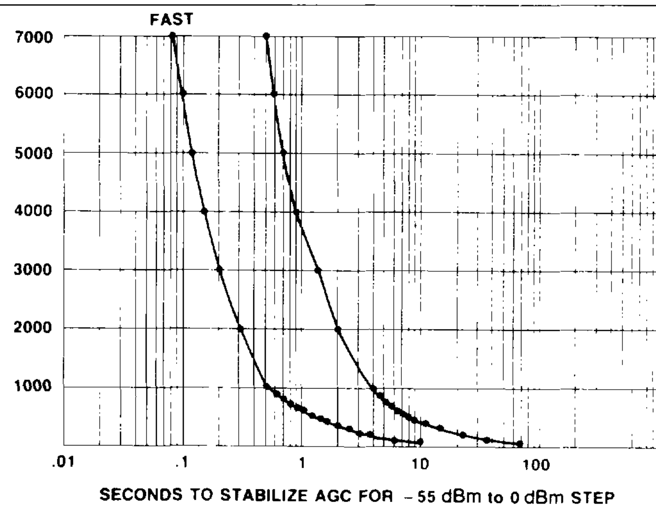
No. 26 Group 2 AGC Slew Rate

Can be adjusted by the host. See Section 8.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 0400h



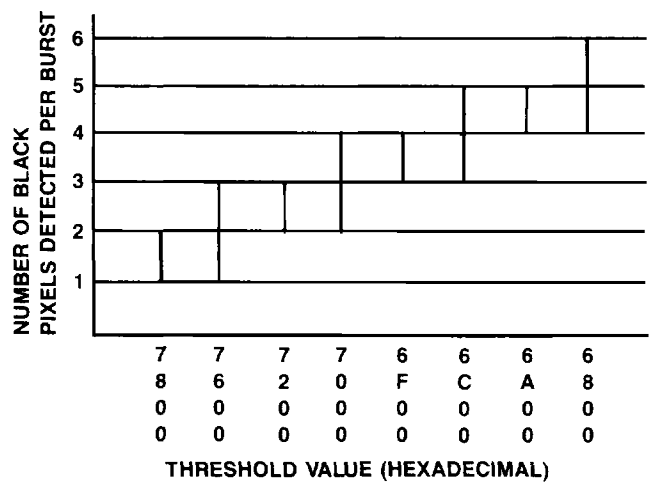
No. 27 Group 2 Black-White Threshold

Format: 16 bits, twos complement, positive value

Default: 7200h

Graph Notes:

1. 100 white pixels sent followed by 4 black pixels sent.
2. Results obtained at 0 dBm, no compromise equalizers in back-to-back connection.



No. 28 Group 2 Phase Limit

When phase error exceeds this limit, PLL updating is suspended. Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits. See Section 8.

Format: 16 bits, twos complement, positive value

Default: 5000h representing ±27.34 degrees

Equation: Phase Limit = $180° - [(\text{Phase Limit})h/2^{15} \times 180°]$

No. 29 Minimum On Time (DTMF)

The on-time is defined as the minimum period of time of the DTMF signal beginning when the signal is detected and ending when the energy is below the turn-off threshold. The on-time parameter cannot be set below 29.6 ms (0000h). The default on-time parameter is set for 40.0 ± 1 ms. The on-time will vary with signal level. To increase or decrease the on-time parameter value, convert the increase/decrease into hexadecimal and add/subtract to/from the current value.

Format:	16 bits, twos complement, positive value
Range:	0000h to 7FFFh
Equation:	Minimum On Time ± [(Increase/Decrease)Sample Rate]h

No. 30 Minimum Off Time (DTMF)

The minimum off time is defined as the minimum period of time of the DTMF signal beginning when the energy falls below the turn-off threshold and ending when a gain hit is detected. The off-time parameter is equal to the desired minimum off-time minus the drop out time. The default off time is set for 40.0 ± 1ms with a default dropout time parameter of 5.0 ms. To increase or decrease the off-time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format:	16 bits, twos complement, positive value
Range:	0000h to 7FFFh
Equation:	Minimum Off Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

No. 31 Minimum Cycle Time (DTMF)

The minimum cycle time is defined as the minimum period of the DTMF signal beginning when the signal is detected and ending when the next signal begins. The cycle time parameter is equal to the desired minimum cycle-time minus the dropout time. The default cycle time parameter is set for 93.0 ± 1 ms with a default drop out time parameter of 5.0 ms. To increase or decrease the cycle time parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format:	16 bits, twos complement, positive value
Range:	0000h to 7FFFh
Equation:	Minimum Cycle Time ± [(Increase/Decrease)Sample Rate]h (dropout time equal to 5.0 ms).

No. 32 Minimum Dropout Time (DTMF)

The minimum dropout time is defined as the maximum period of the DTMF signal beginning when the signal energy drops below the turn-off threshold and ending when the signal energy returns that is considered to be part of the on time. The default dropout time parameter is set to 5.0 ms.

Format:	16 bits, twos complement, positive value
Range:	0000h to 7FFFh
Equation:	[(Desired time)Sample Rate]h

No. 33 Maximum Speech Energy (DTMF)

This parameter specifies the maximum relative speech energy that may be detected and still receive DTMF signals. The speech energy is measured in the frequency region of second or third harmonics of the DTMF tones. To disable the speech energy detector, set this parameter to its full scale positive value (7FFFh). Decreasing the value of this parameter may degrade signal-to-noise ratio (SNR) performance, but may reduce false settings of status bit EDET due to speech signals. To increase or decrease the maximum speech energy parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format:	16 bits, twos complement, positive value
Range:	0000h to 7FFFh
Equation:	Maximum Speech Energy ± (Increase/Decrease)h

No. 34 Frequency Deviation, Low Group (DTMF)

This parameter controls the acceptable frequency range for the low group DTMF tones (697, 770, 852, and 941 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ± (Increase/Decrease)h

No. 35 Frequency Deviation, High Group (DTMF)

This parameter controls the acceptable frequency range for the high group DTMF tones (1209, 1336, 1477, and 1633 Hz). Increasing the value of this parameter increases the frequency range. The frequency range will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the current value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Frequency Deviation ± (Increase/Decrease)h

No. 36 Negative Twist Control (DTMF)

This parameter controls the acceptable negative twist for the DTMF signals. Decreasing this parameter increases the acceptable negative twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Negative Twist ± (Increase/Decrease)h

Default: 1420h

No. 37 Positive Twist Control (DTMF)

This parameter controls the acceptable positive twist for the DTMF signals. Decreasing this parameter increases the acceptable positive twist level. The twist will vary from one DTMF symbol to another. To increase or decrease the parameter value, convert the increase/decrease into hex and add/subtract to/from the default value.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: Positive Twist ± (Increase/Decrease)h

Default: 2800h

No. 38 Maximum Energy Hit Time (DTMF)

This parameter represents the duration of an allowed energy impulse during the off time measurement. The default value of 0000h means no gain hits will be tolerated during the off time.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Equation: [(Desired Time)(Sample Rate)]h

No. 39 Number of Additional Flags, NFLAG (HDLC)

This parameter (NFLAG) controls the number of flags between frames or at the end of the final frame. See Section 5.1.1 for more information.

Format: 16 bits, twos complement, positive value

Default: 0000h

Equation: Desired number of flags - 1

No. 40 FR1 Tone Detector Coefficients

See Section 6 for scaling information.

No. 41 FR2 Tone Detector Coefficients

See Section 6 for scaling information.

No. 42 FR3 Tone Detector Coefficients

See Section 6 for scaling information.

No. 43 Sample Rate Counter 1, Most Significant Bit = COUNTER1
No. 44 Sample Rate Counter 2, Least Significant Word = COUNTER2

These parameters together represent a 17-bit word with the most significant bit being the most significant bit of register COUNTER1 and the remaining 16 bits constituting register COUNTER2. The remaining bits of COUNTER1 must not be changed. Round result to nearest integer before converting to hex. Always write to COUNTER1 before COUNTER2.

Format: 17 bits, unsigned

Equation: COUNTER1msb + COUNTER2 = (2^{17})(1344)(Sample Rate)/(Crystal Frequency) + 0.5

If COUNTER1msb = 1 and configuration is 8xh, COUNTER1 = A3D3h.

If COUNTER1msb = 0 and configuration is 8xh, COUNTER1 = 23D3h.

If COUNTER1msb = 1 and configuration is 9xh, COUNTER1 = A3D0h.

If COUNTER1msb = 0 and configuration is 9xh, COUNTER1 = 23D0h.

Crystal Frequency: 26.39998M MHz (R96VFX); 24.00014 MHz (all except R96VFX)

No. 45 Decoder Reconstructed Speech Samples, D/A Sample Word (ADPCM)

The reconstructed speech samples are written to this RAM location every sample time and sent to the DAC if $\overline{RTS}$/RTSP is on.

Format: 16 bits, signed, twos complement

Equation: Vout(Volts)=[(D/A Sample Word)h]x$(3.03/2^{15})$

No. 46 ADC Speech Sample Scaling Parameter, ADCS (ADPCM)

The received signal sample is scaled by ADCS prior to ADPCM compression. If the host is providing ADC samples to the coder input, ADCS must be 0000h.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 2AABh

No. 47 Host ADC Speech Sample Scaling Parameter, HADCS (ADPCM)

The host provided received signal sample is scaled by HADCS prior to ADPCM compression. HDACS is valid only when the host provides received signal samples to the coder input, and must not otherwise be changed. A value of 8000h (= -1) represents no scaling.

Format: 16 bits, twos complement, negative value

Range: 0000h to 8000h

Default: 4000h (see Section 10)

No. 48 Host ADC Speech Sample (ADPCM)

The host provides received signal samples to the ADPCM coder input by writing to this RAM location.

Format: 16 bits, signed, twos complement

No. 49 Sample Rate ROM Table Pointer, ROMPNT (ADPCM)

When the host writes to this RAM location prior to ADPCM 9x configuration, the sample rate automatically changes to 9.6K, 8K, 7K, or 6K Hz. Also, DTMF receiver and FSK flag pattern (7E) detector parameters are initialized according to the chosen sample rate.

Equation:

ROMPNT	Sample Rate (Hz)
0000h	9600
0001h	8000
0002h	7000
0003h	6000

Default: 0001h, 8000 Hz sample rate at power-on

No. 50 White Noise Output Scaling Parameter, RANOISE (ADPCM)

This parameter controls the output level of the white noise inserted during silence intervals when the decoder is enabled.

Format: 16 bit, twos complement, positive value

Range: 0000h to 7FFFh

Equation: $RANOISE = [\sqrt{(10^{x/10}/15.3015)}] * (2^{15})$

where x is the desired output level in dBm.

Default: 0080h

No. 51 Minimum Silence Magnitude Threshold, MTHRESH (ADPCM)

If the background noise level is high, MTHRESH may be increased to allow more silence to be detected and deleted. Any signal with energy less than MTHRESH is detected as silence. However, a signal with energy greater than MTHRESH may or may not be detected as silence. Therefore, MTHRESH is the lower limit of a adaptive energy threshold where signals with energy above this threshold are speech and signals below this threshold are silence.

Format: 16 bits, twos complement, positive value

Equation: $MTHRESH = [\sqrt{(10^{x/10}/15.3015)}] * (2^{15})$

where x is the level in dBm.

Range: 0000h to 7FFFh

Default: 0032h, -44.6 dBm

No. 52 Detecting Silence in Speech Parameter, SILSPE (ADPCM)

SILSPE is used in determining when silence is detected during speech. To detect speech-to-silence transition slower, decrease SILSPE. A late transition will prevent the ends of spoken words from being deleted.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 5555h

No. 53 Detecting Speech In Silence Parameter, SPESIL (ADPCM)

SPESIL is used in determining when speech is detected during silence. To detect silence-to-speech transition faster, decrease SPESIL. An early transition will prevent the beginning of spoken words from being deleted. SPESIL must be greater than MADAPT.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 5000h

No. 54 Minimum Silence Magnitude Adaptation Parameter, MADAPT (ADPCM)

MADAPT controls the rate at which the silence-to-speech energy threshold adapts to the changing received signal energy. If MADAPT is too large, segments of a speech signal will be deleted resulting in unintelligible, choppy, speech. MADAPT must be less than SPESIL.

Format: 16 bits, twos complement, positive value

Range: 0000h to 7FFFh

Default: 5555h

No. 55 Maximum Gain, dBTHR (ADPCM)

This parameter specifies the maximum AGC gain applied to the ADPCM coder input signal only. Reduce the maximum gain if the background noise level is too high.

Format: 16 bits, twos complement, positive value

Equation: dBTHR = [63 - (63/50)G)h

where G is the desired maximum gain in dB.

Range: 0000h to 003Fh representing 50.0 dB to 0 dB maximum gain.

Default: 0025h representing 20.6 dB maximum gain.

5 HDLC FRAMING

The modem supports HDLC framing. The HDLC (High Level Data Link Control) protocol is a standard procedure used for data communications. SDLC (Synchronous Data Link Control) is a bit-oriented protocol which is a subset of HDLC. The same format is used in both protocols although all SDLC fields must be eight-bit octets. The MONOFAX modem uses the SDLC eight-bit octet format.

5.1 HDLC FRAMES

Data and control information on a HDLC link are transmitted via frames. These frames organize the information into a format specified by an ISO standard that enables the transmitting and receiving station to synchronize with each other. This format is shown in Figure 5-1.

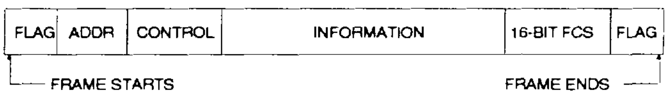


Figure 5-1. HDLC Frame

5.1.1 Frame Fields

Flags

All frames start and end with a flag sequence. The beginning flag and the ending flag are defined by the bit pattern 01111110 (7Eh). The ending flag for one frame can also serve as the beginning flag for the following frame. If separate ending and beginning flags are used, the final zero in the ending flag of one frame may also serve as the first zero of the beginning flag in the following frame. This process is known as "zero-sharing". The zero-sharing bit pattern is 011111101111110.

Address Field

The address field informs the receiver where the information is to go (if the primary station is transmitting) or where the message originated (if a secondary station is transmitting). This field is eight bits in length for the "basic" format.

For the "extended" format, the length is N number of octets, each octet having the first bit a binary zero with the exception of the last octet that begins with a binary one.

Broadcast Address = 11111111
Null Address = 00000000

Control Field

The control field defines the function of the frame. It may contain a command or response. The control field might also contain send or/and receive sequence numbers. This field can be in one of the following formats:

1. Information Transfer Format
2. Supervisory Format
3. Unnumbered Format

This field is normally eight bits in length. However, certain protocols allow for an "extended" control field. For example, it is 16 bits in length for modulo 128 operation of the LAP and LAPB procedures.

Information Field

The modem treats the address field, the control field, and any other transmitted data, except for the flags and the Frame Check Sequence, as the information field. The information field does not have a set length; however, this field follows the SDLC protocol in being in the format of eight bit bytes.

Zero Insertion

Since flags mark the beginning and ending of a frame, some method must be implemented to inhibit or alter the transmission of data that appear as flags. The method used is called "zero insertion". HDLC procedures require that a zero be transmitted following any succession of five continuous ones. This includes all data in the address, control, information and Frame Check Sequence fields. Use of zero insertion denies any pattern of 01111110 to ever be transmitted between beginning and ending flags.

Zero Deletion

When transmitting flags, zero insertion is disabled. During reception of data, after testing for flag recognition, the receiver removes a zero that immediately follows five continuous ones. This is termed "zero deletion". A one that follows five continuous ones signifies either a frame abort (i.e., at least seven ones with no zero insertion) or a flag (i.e., 01111110). The sixth one is, therefore, not removed.

Frame Check Sequence (FCS)

The purpose of the Frame Check Sequence (FCS) is to give a shorthand representation of the entire transmitted information field and to compare it to the identically generated shorthand representation of the received sequence. If any difference occurs, the received frame was in error and should be re-transmitted.

The FCS computation is done on all fields within the frame but does not include the flags. Cyclic Redundancy Check (CRC) is the method used. The polynomial is specified in CCITT T.30 and X.25 as follows:

$$x^{16} + x^{12} + x^5 + 1$$

The polynomial is implemented as shown in Figure 5-2.

The FCS is sent as two bytes of data immediately preceding the ending flag of the frame. The FCS register is first preset to all binary ones. The register is then modified by shifting in the data (no flags) contained in the address, control, and information fields. Following the last bit of data, the ones complement of the FCS register is transmitted as the 16-bit FCS. The FCS is transmitted with the highest order bit (x^{15}) first.

5.1.2 Frame Abortion, Frame Idle, And Time Fill

Frame abortion prematurely finishes transmission of a frame. This occurs by sending at least seven consecutive ones with no zero insertion. This abort pattern terminates a frame immediately and does not require a FCS or an ending flag.

An abort pattern followed by a minimum of eight additional consecutive ones idles the data link. Thus, seven to fourteen ones establish the abort pattern; fifteen or more ones constitute an idle pattern.

Interframe time fill is accomplished by transmitting continuous flags without zero-sharing between flags. Therefore, the transmitter must be capable of sending multiple flags to maintain the active state in the receiver if any time fill is required.

5.2 IMPLEMENTATION

A representation of the HDLC process is shown in Figure 5-3. The events are numbered in order of occurrence from one to four.

1. The beginning flag is transmitted. The receiver sees the flag and now becomes aligned with the transmitter. Both the receive and the transmitter FCS registers are preset to FFFFh.
2. The information field is transmitted. The data is also run through the FCS register before zero insertion. At the receive end, after the zero deletion algorithm, the data is presented to the user and then run through the FCS register.
3. The FCS is inverted and then transmitted. The transmitted FCS is passed through the receiver's FCS register. The shift register will contain 1111000010111000 if the frame has been received correctly.
4. The ending flag is transmitted.

The signal timing is illustrated in Figure 5-4.

5.2.1 Mode Selection

In order to use HDLC in the modem, the host processor must:

1. Set up the modem configuration.
2. Set the parallel data mode bit (PDM).
3. Set the HDLC mode bit.
4. Set the SETUP bit.

RAM Access 1 (using ADD1) remains available while RAM Access 2 (using ADD2) is unusable in the parallel data mode. HDLC transmission cannot be performed using the serial interface.

The format of the data input to the modem is in groups of 8-bit bytes. As in the parallel data mode, the least significant bit of the byte is transmitted first.

5.2.2 Transmission and Reception Rate

The HDLC as implemented in the modem runs under the following transmitter and receiver modes:

V.29
V.27 ter
V.21
V.21 with DTMF receiver

Note: In the high speed modes, any data patterns referred to in this guide are transmitted scrambled and received descrambled.

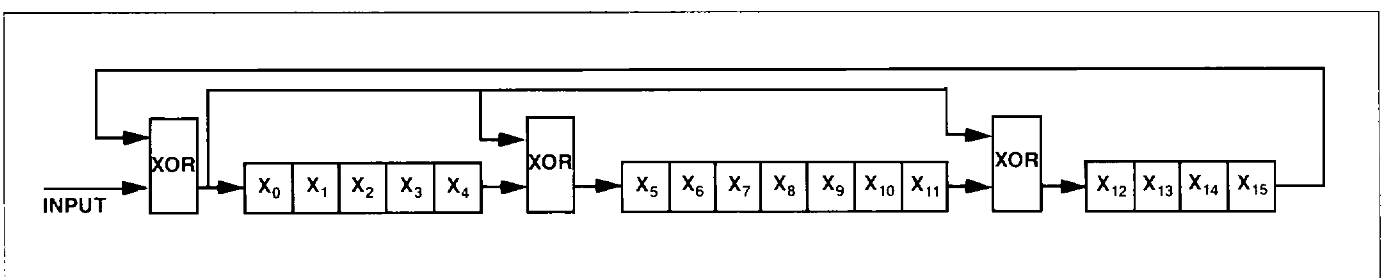


Figure 5-2. CRC Polynominal Implementation

5.2.3 Transmitter and Receiver Initialization

The HDLC transmitter and receiver is initialized differently than other modes upon power-up, reconfiguration, or turning on RTS input or RTSP bit. Table 5-1 shows the states of the interface memory bits for HDLC initialization.

5.2.4 Flag Transmission and Reception

The modem transmitter sends at least one flag as the opening flag of the first frame. As long as the user does not load the 8-bit transmit data register, DBUFF (register 10h), with data, the modem sends continuous flags with no zero-sharing (i.e., 0111111001111...). This facilitates transmission of the preamble as specified in T.30. Thus, the transmitter defaults to transmitting time-fill and, therefore, keeps the receiving link station active.

To assist the user in transmitting more than one flag between frames or at the end of the final frame, a counter (NFLAG) can be accessed through modem DSP RAM access (see Section 4.2). This counter is decremented directly in the signal processor's RAM. This means that the number written will only last for one group of flags. For example, FSK should have at least two beginning flags for the first frame and at least two ending flags for the final frame. However, frames between these two require only one flag.

Table 5-1. Transmitter and Receiver Initialization

Transmitter		Receiver	
ABIDL[2] =	0	ABIDL[2] =	0
AEOF[2,4] =	0	AEOF[2,4] =	0
BA2 =	1	BA2 Not Initialized	
CRC[1,2] =	0	CRC[2] =	0
EOF[2] =	0	EOF[2] =	0
FLAG =	0	FLAG =	0
OVRUN[2] =	0	OVRUN[2] =	0
ZEROC[2] =	0	ZEROC[2,3] =	0

Notes:
1. Not applicable in the transmitter.
2. Zeroed only upon power-up; unchanged elsewhere.
3. Not applicable in the receiver.
4. R96VFX only.

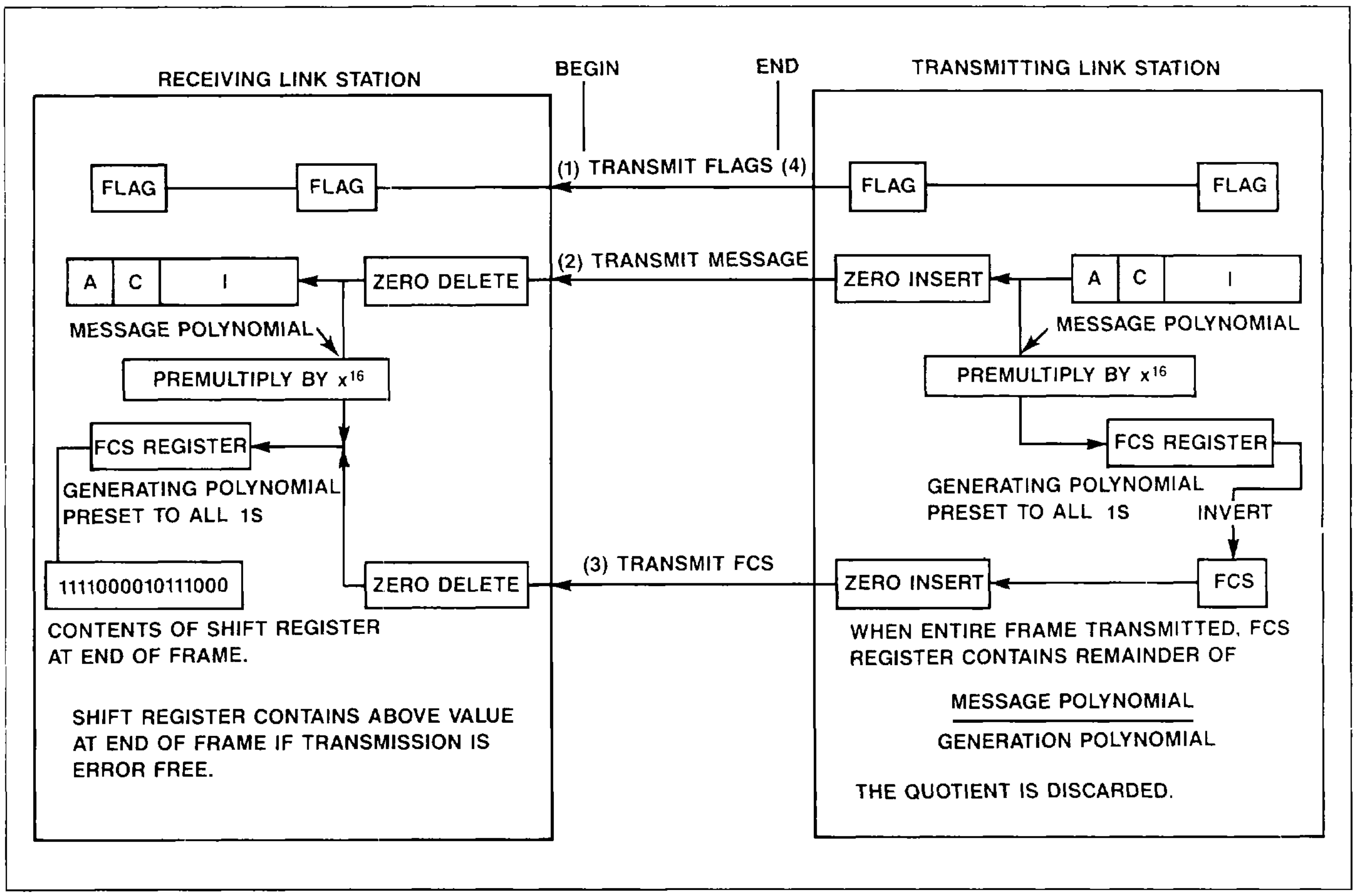
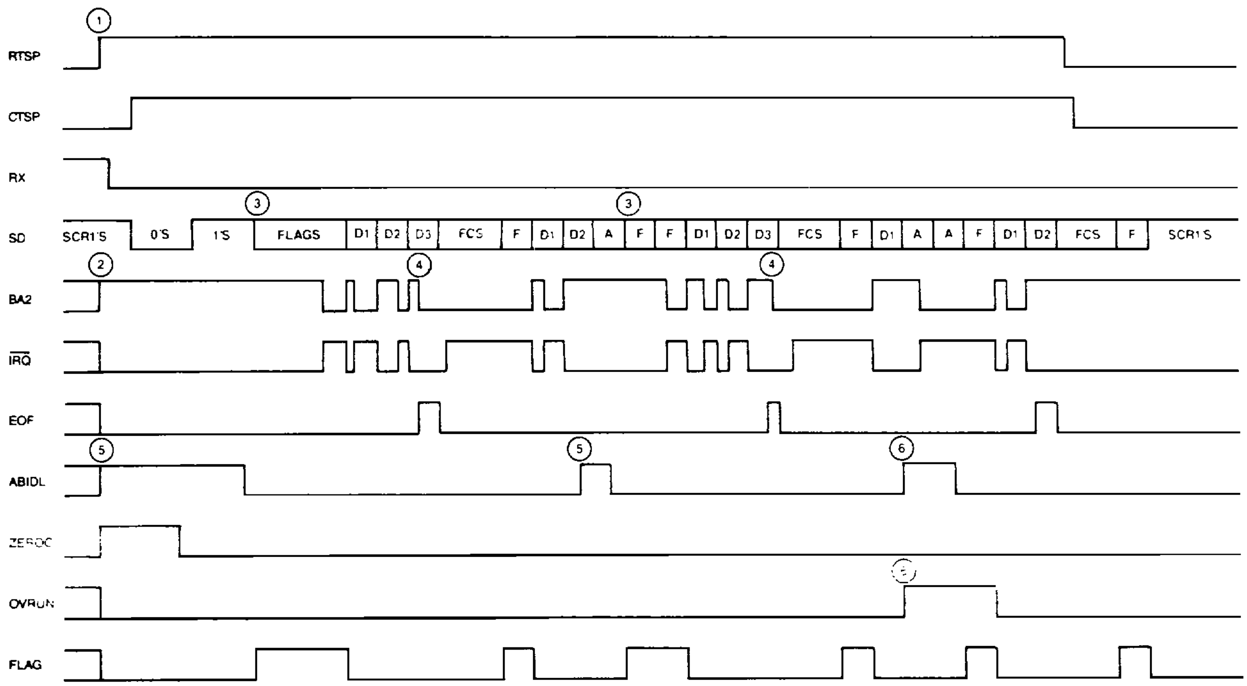


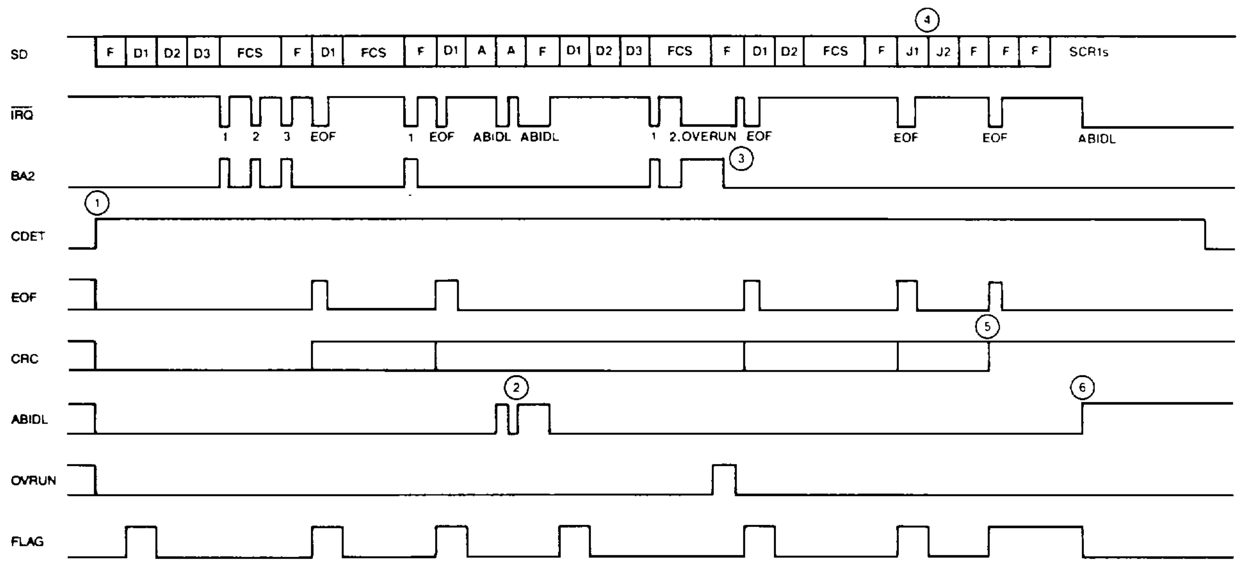
Figure 5-3. HDLC Process



Transmitter Mode Control

1. Upon setting RTSP, the host should initialize EOF, ABIDL, ZEROC, and OVRUN to the desired values.
2. BA2 is forced high 0.7 μs before RX(0D:7) goes low.
3. The host can send multiple flags by either waiting to load data into DBUFF or by doing a diagnostics write to RAM (see "Flag Transmission and Reception" Section). The host can then load the first byte when RX goes low for the first frame or after setting EOF for subsequent frames.
4. Load the first byte of the next frame after setting EOF.
5. The host sets and resets ABIDL here.
6. A transmit underrun occurs here. The modem sets ABIDL. The host must reset ABIDL.
7. AEOF is 0 in this example.

a. Transmitter



Receiver Notes

1. EOF, ABIDL, and OVRUN should be a known value before the data appears on RXD.
2. The host resets ABIDL in the middle of receiving an abort/idle sequence.
3. A receive overrun condition has occurred.
4. J1, J2 are junk (invalid) data.
5. CRC sets and EOF sets in response to the junk data between flags.
6. ABIDL remains high due to the incoming scrambled 1's turnoff sequence for high speed modes.

b. Receiver

Figure 5-4. HDLC Signal Timing

This is why the counter is decremented directly and one flag is transmitted as a default. Modem DSP RAM access should be setup as shown below:

ADD1 =	85h
BR1 =	0
CR1 =	1
IO1 =	0
WRT1 =	1

The value to write into YDAM1 and YDAL1 should be 1 less than the number of flags desired. This value can be written anytime after the RX bit returns to zero and before FLAG is set by the modem.

Using the FSK example above, assume three flags are to be transmitted at the beginning of the first frame and at the end of the final frame.

1. Turn on RTS.
2. Wait until the RX bit is reset by the modem.
3. Disable RAM Access 1 (reset ACC1).
4. Setup RAM Access 1 as above, write 00h into YDAM1, and write 02h into YDAL1.
5. Enable RAM Access 1 (set ACC1).
6. Wait until BA1 is set before resetting WRT1.
7. For the ending flag of the final frame, immediately after loading in the final byte of data or after setting EOF, again setup RAM Access 1 as above, write 00h into YDAM1, and write 02h into YDAL1.

Another method exists for sending extra flags. The host must simply do nothing since flags are transmitted as the default condition. In other words, after the final zero in a flag is transmitted, the modem looks to see if the host has loaded new data into DBUFF (BA2 is reset). If no new data is loaded before this time, another flag is sent. Therefore, if more than one flag is desired, the host must wait N-1 multiples of eight bit times after FLAG is set by the modem to load new data into DBUFF, where N is the number of flags. The host then has seven bit times in which to load new data and thus prevent another flag from being sent. For example, if three flags are desired between frames, the host must wait at least 16 bit times and not more than 23 bit times after FLAG is set by the modem.

As the default condition, the modem receiver continually searches for the flag data pattern. When one or more flags are detected, the interface memory status bit FLAG (09:0) is set. The flags themselves are not presented to the host through the DBUFF register. Therefore, as soon as a flag is observed, the modem examines the next byte of received data. If it is a flag, an abort/idle sequence, or a FCS, it is not given to the user. Instead, the appropriate status bits are set or reset.

The modem also has the capability to detect consecutive flags with zero-sharing.

5.2.5 Information Field Transmission and Reception

For information field transmission, the host should wait for CTSP (0F:1) to transition high. The host must then load the data into DBUFF and then wait for the data available bit BA2 (1E:3) to be set by the modem before loading in the next byte of data. If AEOF is 0 and the next byte is not loaded into DBUFF within the next eight bit times, the modem will set OVRUN (09:7), indicating an underrun condition has occurred. To tell the modem that the host wants to end the frame, the host must set EOF as soon as the modem has taken the last byte of the frame (BA2 sets). When the modem recognizes EOF being high, the modem will reset EOF and will transmit the FCS and closing flag. Once the host sets EOF, the host may load in the first byte of data of the next frame into DBUFF. If the host wants to end transmission, the host must wait for EOF to return low before turning off RTS or RTSP.

The automatic frame ending feature (R96VFX only) can be used to more easily facilitate the use of a DMA interrupt system. With this feature, data is transmitted as described in the above paragraph. However, when AEOF (15:5) is set by the host, the ending of the frame occurs "automatically", i.e., without the host having to perform any handshaking. When the host is finished sending the data in the frame, the host should wait until EOF is set to a 1 by the modem. The modem will then send the 16-bit FCS and at least one ending flag. When EOF is set to a 1 by the modem, the host can then load in the first byte of data of the next frame. EOF will be set to a 0 by the modem at the beginning of flag transmission. Therefore, the underrun condition as described in the previous paragraph is the exact same condition that causes the 16-bit FCS and ending flag to be transmitted when AEOF is set to a 1.

In the receiver, only the information field data between flags is passed to the user through the DBUFF register by the use of the handshaking bit BA2. The user must wait for BA2 to be set by the modem and then take the data. If AEOF is 0 and the host does not read the data within eight bit times, OVRUN will set indicating an overrun condition, and the data in DBUFF will be overwritten by the next byte.

Furthermore, no flags, abort/idle sequence, or FCSs are given to the user via the DBUFF register. Since these fields are not presented to the user, there is at least a 16-bit time delay in the reception of data when receiving these fields. This allows the FCS and ending flag, continuous flags, or the abort/idle sequence to be flushed out of the internal buffers.

5.2.6 FCS and Ending Flag Transmission and Reception

If AEOF is 0, the host ends a frame by loading in his last byte of data into DBUFF, waiting until the modem has taken it (BA2 sets), and then setting EOF. After setting EOF, the host may load in the first byte of data of the next frame into DBUFF. When the modem recognizes that the host wants to end the frame, the modem will reset EOF. To terminate data transmission, the host may turnoff RTS or RTSP when the modem resets EOF. After resetting EOF, the modem will automatically transmit the 16-bit FCS and at least one flag that signifies the end of the current frame and, if another frame follows, the beginning of the next frame.

For the case when AEOF is set to a 1 (automatic end of frame), the host ends a frame by loading in the last byte of data and waiting until EOF is set to a 1 by the modem. The host may then load in the first byte of data of the next frame. To terminate data transmission, the host may turn off RTS or RTSP when the modem sets EOF to a 1. The modem will then automatically transmit the 16-bit FCS and at least one flag that signifies the end of the current frame and, if another frame follows, the beginning of the next frame. The modem will set EOF to a 0 upon sending a flag.

Upon the receipt of an ending flag in the current frame (which may also be the beginning flag of the next frame), the modem examines the data in the FCS register and compares it to the remainder. If the FCS register remainder is correct, CRC (09:1) is reset. Conversely, if the remainder is incorrect, the CRC bit is set. This is the only time CRC is updated (except upon power-up). Following this determination, the modem sets EOF. Thus, once the modem sets EOF, the host can examine CRC to determine whether or not an erred frame was received. It is left to the host to reset the EOF bit. If the user does not reset EOF before the end of the next frame, the host will not get any indication that the following frame has ended.

5.2.7 Abort/Idle Sequence

The act of prematurely terminating the transmission of a frame is called aborting transmission. The transmitting station aborts a transmission by sending a minimum of seven 1s with no zero insertion (see CCITT Recommendation X.25).

Abort/Idle Sequence Transmission

An abort/idle sequence can be sent by the host setting the bit ABIDL (09:3) in the interface memory (Figure 5-5a and Figure 5-6). This stops any normal frame transmission, as well as continuous flag transmission, and sends continuous ones. After the setting of ABIDL is detected, the modem first completes the transmission of the current byte of data. Immediately after this transmission, the modem sends eight consecutive ones [1]. (Numbers in brackets refer to events in the transmission abort/idle sequence shown in Figure 5-5a.) After these eight bit times, if ABIDL is still set, eight ones are sent again [2]. To discontinue this sequence, ABIDL must be reset [3]. Then, if no new data is loaded into DBUFF, continuous flags are sent [4]. If new data is loaded into DBUFF (BA2 is reset), the modem sends a beginning flag and then the data in DBUFF [5]. The modem will also recognize the setting of ABIDL while transmitting the FCS, thereby allowing the receiver to recognize that the transmitted frame should be discarded.

The modem also has the ability to send continuous zeros. To accomplish this, ABIDL and ZEROC (09:4) must be set. The modem completes the transmission of the current byte and then sends eight consecutive zeros [6]. After this time, if ABIDL remains set, eight zeros are sent again. To discontinue this sequence, ABIDL must be reset or, if continuous ones are desired, ZEROC only must be reset [7]. However, if no new data is loaded in DBUFF and ABIDL is reset, continuous flags are sent regardless of the state of ZEROC. Then, if new data is loaded into DBUFF (BA2 is reset), the modem sends a beginning flag and then the data in DBUFF.

Abort/Idle Sequence Reception

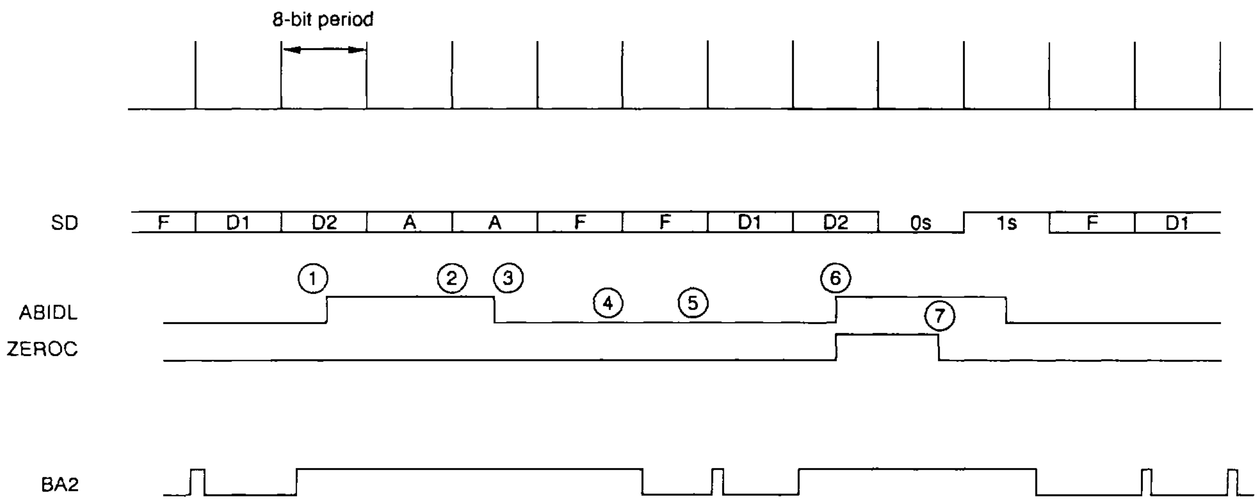
The modem in HDLC mode not only continually searches for flags, but also continually searches for an abort/idle sequence. When the receive modem encounters this data pattern, it sets the abort/idle receive bit ABIDL [8] (Figure 5-5b and Figure 5-7). It is left up to the host to reset this bit. However, receiver processing will continue unaffected by the state of this bit [9].

The reception of data immediately following the abort/idle sequence is treated as invalid and is not presented to the user. Therefore, to re-establish transmitter and receiver synchronization, the receiver must see at least one flag. At least one flag and three bytes of data must be received following the abort sequence before any data is given to the host.

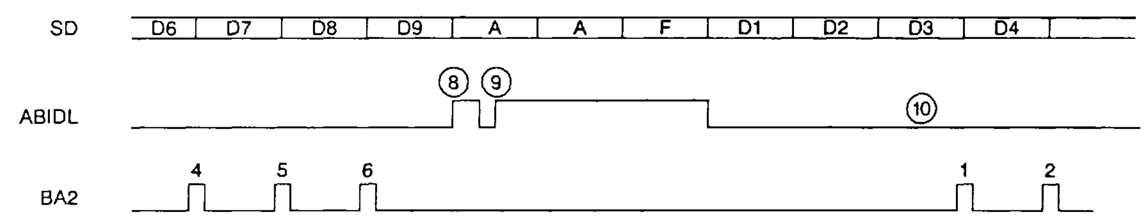
5.2.8 Underrun and Overrun Conditions

A bit in the interface memory OVRUN (09:7) is used to indicate to the host processor that a transmit underrun condition has occurred. If the host does not load in a new byte of data within eight bit times, OVRUN and ABIDL will be set by the modem and the modem will automatically send a minimum of eight continuous ones. This abort sequence will continue until the host resets ABIDL. After the host resets ABIDL, the modem will finish sending the current byte of ones and will then send a flag. At the end of sending a flag, if BA2 is reset, the modem will interpret the data in DBUFF as being the first byte of the next frame. After uploading this data for the first byte of the frame, the modem will reset OVRUN. The modem will always reset OVRUN every time it sets BA2, except upon transmitter HDLC initialization. (The underrun condition is not applicable when AEOF = 1.)

In the receiver, the OVRUN bit will inform the host that an overrun condition occurred. The overrun condition takes place when the receiver fails to take the byte of data in DBUFF within eight bit times. The modem will thus overwrite the data in DBUFF and, if the host has not taken the data (BA2 is not reset), the modem will set OVRUN. To detect further overrun occurrences, the host must reset this bit.



a. Transmitting



Note: ABIDL can be reset by the host when it detects a flag condition

b. Receiving

820F5-5

Figure 5-5. Abort/Idle Sequence Timing

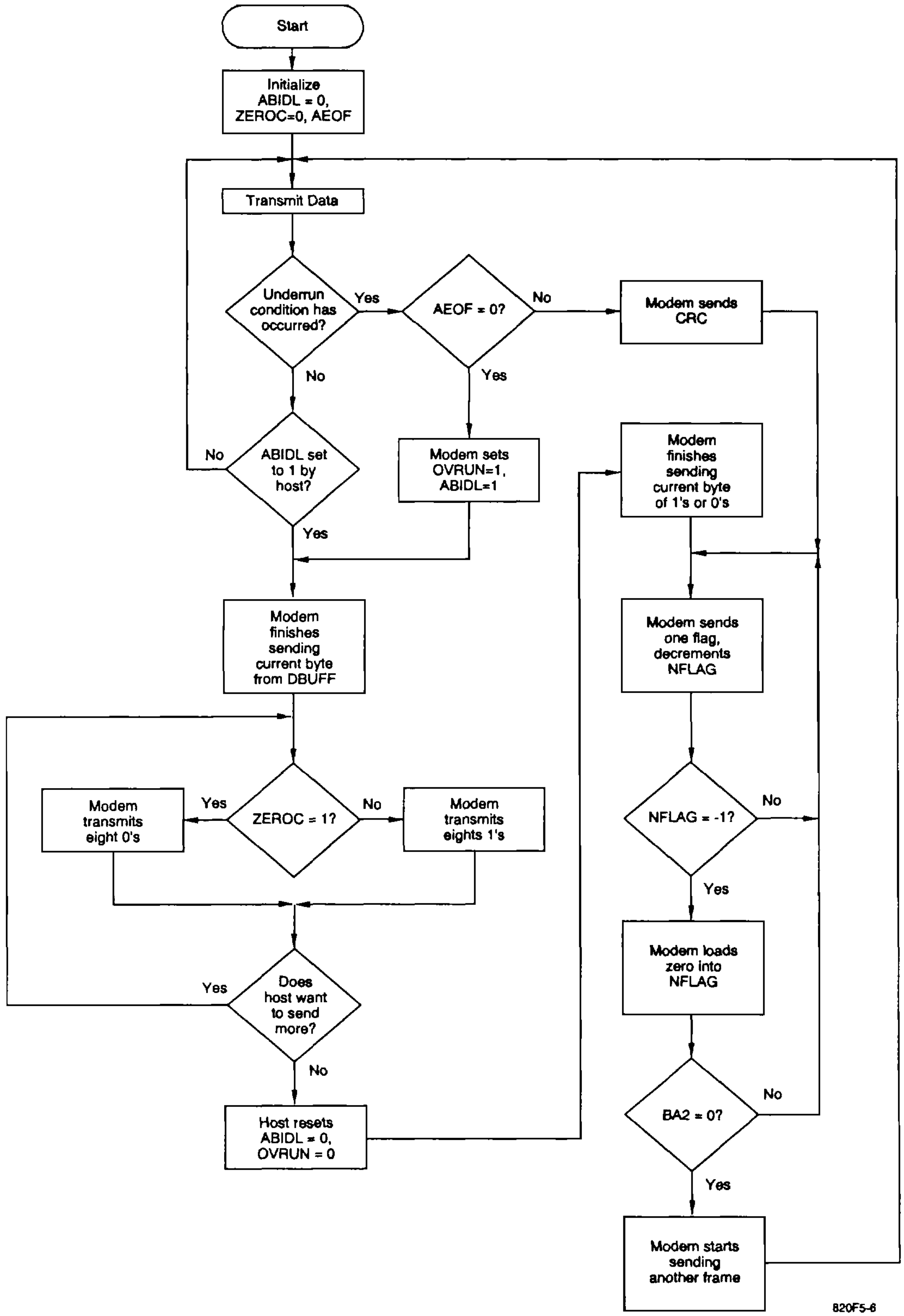


Figure 5-6. Abort/Idle Transmission Sequence Flowchart

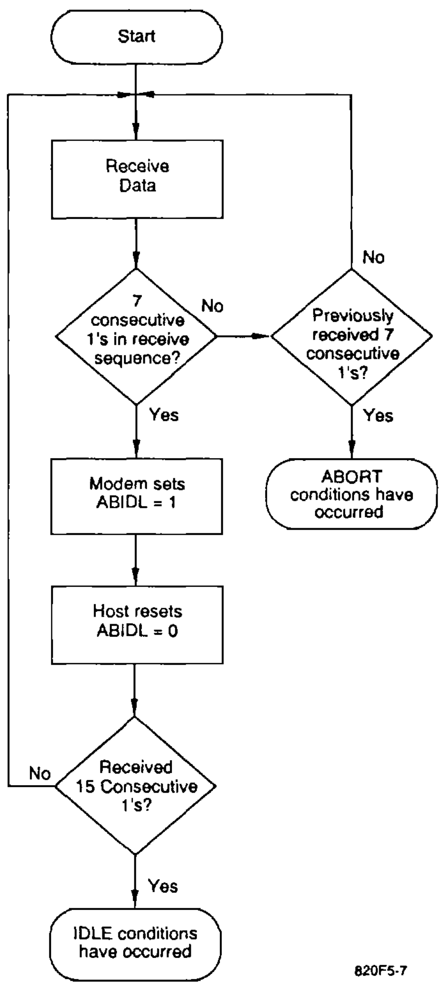


Figure 5-7. Abort/Idle Reception Sequence Flowchart

5.2.9 Transmit Mode Control

After power-up, reconfiguration, or turning $\overline{RTS}$ input or RTSP bit on, the host must wait for $\overline{CTS}$ output or CTSP bit to turn on before starting frame transmission.

There are two ways in which the user can signal the modem to exit current HDLC execution. The first way is by setting the SETUP bit which tells the modem that a new configuration is desired. The second way is by turning off $\overline{RTS}$ input or by resetting the RTSP bit in the interface memory. In both cases, the following events will occur:

1a. **When AEOF is set to a 0 and if exiting after making sure the modem took the data in DBUFF, setting EOF to a 1, and then waiting for EOF to be set to a 0 by the mode,** the modem sends the last byte of data followed by the 16-bit FCS sequence and a closing flag. The modem then either goes through the turn-off sequence (if RTS output or RTSP bit is turned off), or sets up the new configuration (if SETUP is set to a 1).

1b. **When AEOF is a set to a 1 and if exiting after making sure the modem sets EOF to a 1,** the modem sends the last byte of data followed by the 16-bit FCS sequence and a closing flag. The modem then either goes through the turn-off sequence (if RTS output or RTSP bit is turned off), or sets up the new configuration (if SETUP is set to a 1).

2. **If exiting during the transmission of an abort sequence**, the modem finishes sending the last byte of the abort sequence, then either goes through the turn-off routine or sets up to a new configuration.

5.3 EXAMPLE APPLICATION

Refer to Section 3 for a description of the bits associated with the HDLC and programmable interrupt functions.

Transmitter Example

1. Set the modem configuration to the desired speed for transmitting, enable HDLC, parallel data mode, and RTSP. (AEOF defaulted to 0).
2. Wait until CTSP goes low and returns to a high level.
3. Place the first byte of data into DBUFF. The modem transmits a flag followed by this byte of data.
4. As soon as BA2 is set, load in the next byte of data. This must occur within eight bit times of BA2 being set.
5. After all information but the last byte is given to the modem, load in the last byte of data in the frame as in step 4.
6. To end the frame, the host must load in the last byte of data into DBUFF, wait for BA2 to be set, and then set EOF.
7. Repeat steps 3 through 6 for all frames to be transmitted.
8. When the last byte of the final frame is loaded into register DBUFF, wait for BA2 to return high. Then set EOF and wait for EOF to return low before resetting RTSP. The modem transmits the last byte followed by the 16-bit FCS and at least one closing flag, depending upon if DSP RAM access was used to write into the flag counter RAM location as mentioned previously. The modem then goes through its normal turn-off routine.

Receiver Example

The steps to perform a typical HDLC reception are:

1. Set the modem configuration to the desired speed for receiving, enable HDLC, and parallel data mode.
2. Perform a dummy read of DBUFF to reset BA2.
3. Wait until the modem has properly configured.
4. Monitor, through interrupts, the EOF, ABIDL, and BA2 bits in the interface memory.
5. Wait for an interrupt. If it is caused by BA2 being set, read the data in DBUFF. This indicates that the first byte of the first frame is ready for host reading. If the interrupt is caused by EOF being set, check CRC to determine if the current frame is in error and reset EOF. If the interrupt is caused by ABIDL, the modem is receiving the abort/idle sequence. The current frame that was aborted is invalid. The modem does not set the CRC bit or the EOF bit in this case since no FCS checking is done.
6. Continue waiting for interrupts and take appropriate action when the interrupts are received.

6 TONE DETECTOR FILTER TUNING

This section describes a method of tuning the filters in the modem for tone detection.

6.1 PROGRAMMABLE TONE DETECTORS

The modem includes three independently programmable tone detectors (F1, F2, and F3). All tone detectors are operational when the modem is configured in FSK, FSK and DTMF receiver, Voice mode receiver, ADPCM, Group 2, or tone configuration (with RTSP and RTS off). Tone detector F3 is also operational in all of the high speed configurations. Upon power-up, the tone detectors are centered at 2100 Hz (F1), 1100 Hz (F2), and 462 Hz (F3) in non-Group 2 configurations. For Group 2 characteristics, see *Tone Detectors in Group 2* section (Section 6.2).

In each of the three detectors, two second-order biquadratic filters can be programmed for a variety of frequency responses. The modem sets interface memory bits FR1, FR2, and FR3 when tone detectors 1, 2, and 3 detect energy above their respective threshold. This application note presents a method of tuning these detectors to any frequency in the 400 Hz – 3k Hz band.

By setting bit 12TH in the modem DSP interface memory, the three tone detectors are cascaded to form a programmable 12th-order filter. In this case, the modem sets only the FR3 bit when energy is above the threshold. Bit 12TH is not operational in the high speed modes.

6.1.1 Computation of Tone Detector Coefficients

Each tone detector consists of two second-order filters in cascade, an energy averaging filter, and a threshold comparator. A diagram of a tone detector is shown in Figure 6-1.

Filter 1 has a transfer function:

$$H_1(Z) = \frac{2(\alpha_0 + \alpha_1 Z^{-1} + \alpha_2 Z^{-2})}{1 - 2\beta_1 Z^{-1} - 2\beta_2 Z^{-2}} \qquad \text{(Eq. 1)}$$

Filter 2 has a transfer function:

$$H_2(Z) = \frac{2(\alpha'_0 + \alpha'_1 Z^{-1} + \alpha'_2 Z^{-2})}{1 - 2\beta'_1 Z^{-1} - 2\beta'_2 Z^{-2}} \qquad \text{(Eq. 2)}$$

The energy averaging filter has a transfer function:

$$H_3(Z) = \frac{\alpha''}{1 - \beta'' Z^{-1}} \qquad \text{(Eq. 3)}$$

The output of the energy averager is fed to a threshold comparator that sets interface memory bit FR1, FR2, or FR3 if the output is equal to or greater than 1/8 of full scale, otherwise, the bits are reset.

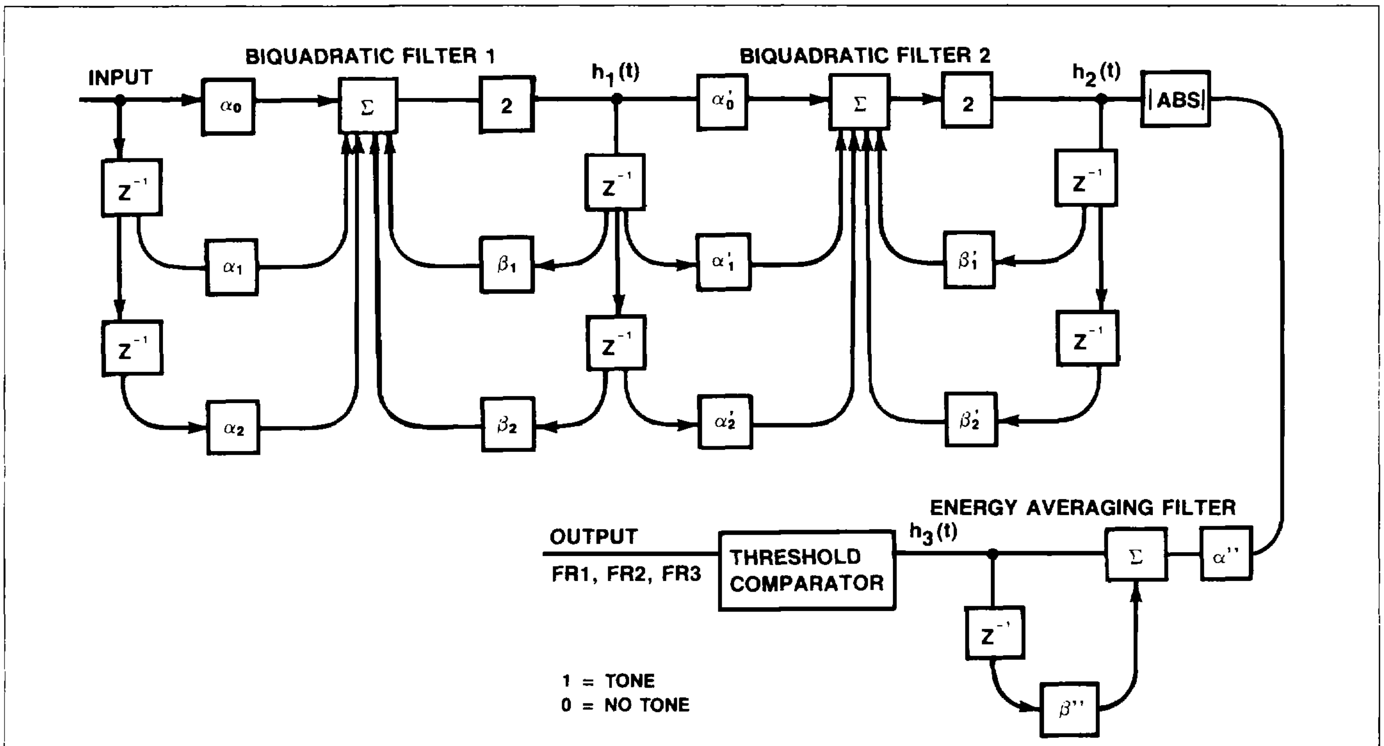


Figure 6-1. Modem Tone Detection Diagram

Upon power up, each of the biquadratic filters has a typical frequency response as shown in Figure 6-2. When cascaded, they form a bandpass filter with a narrow bandwidth as shown in Figure 6-3.

Given the transfer functions $H_1(Z)$ and $H_2(Z)$, an analytical method is required to compute their coefficients for any frequency in the 400 Hz – 3 kHz band. First, consider $H_1(Z)$. This transfer function can be rewritten as:

$$H_1(Z) = \frac{2(\alpha_0 Z^2 + \alpha_1 Z + \alpha_2)}{Z^2 - 2\beta_1 Z - 2\beta_2} \qquad \text{(Eq. 4)}$$

which has a conjugate pair of poles:

$$P_1 = \beta_1 + j\sqrt{(\beta_1^2 + 2\beta_2)}$$

and

$$P_2 = \beta_1 - j\sqrt{(\beta_1^2 + 2\beta_2)}$$

Upon power up, these poles lie on a circle of radius 0.994030884 on the Z-plane. The radius of the tone detector circle was chosen so that each filter has a high Q without being unstable (i.e., poles must lie inside the unit circle for stability). Figure 6-4 shows a Z-plane pole-zero diagram for an arbitrary conjugate pole pair on the tone detector circle. The angle $\theta = 360° \ (f_O/f_S)$, where f_O is the desired center frequency and f_S is the sample rate. The sample rate is 9600 Hz in high speed and FSK modes, 10386 Hz in Group 2, defaults to 9600 Hz in tone and voice modes, and defaults to 8000 Hz in ADPCM modes.

The following equations are derived from the angle and magnitude of the position vector pointing to a pole pair located at the desired angle:

$$\cos^{-1}(\beta_1/r) = \theta = 360° \times f_O/f_S \qquad \text{(Eq. 5)}$$

$$\sqrt{[\beta_1^2 + (-\beta_1^2 - 2\beta_2)]} = r = 0.994030884 \qquad \text{(Eq. 6)}$$

Solving for β_1 and β_2:

$$\beta_1 = r\cos(360° \times f_O/f_S) \qquad \text{(Eq. 7)}$$

$$\beta_2 = -r^2/2 \qquad \text{(Eq. 8)}$$

In deriving these equations, only $H_1(Z)$ was considered. However, the tone detector consists of two identical filters in cascade when bit 12TH equals zero. Referring to Figure 6-3, shifting filter 1 and filter 2 above and below the desired center frequency, a response with the desired bandwidth is achieved. Furthermore, since the α_1, α'_1, α_2 and α'_2 coefficients default to zero upon power-up, α_0 controls the amplitude response, and one may set $\alpha_0 = \alpha'_0$ to uniformly raise or lower the overall cascade response.

From Equation 8, we see that:

$$\beta_2 = \beta'_2 = -r^2/2 = -0.494048699$$

Rewriting Equation 7 in terms of the offsets f_A and f'_A we obtain:

$$\beta_1 = r\cos[360° \ (f_O - f_A)/f_S] \qquad \text{(Eq. 9)}$$

$$\beta'_1 = r\cos[360° \ (f_O + f'_A)/f_S] \qquad \text{(Eq. 10)}$$

The frequency offset is approximately 72% of B/2 (half the bandwidth) for most applications:

$$f'_A \approx 0.72\ (B/2) \qquad \text{(Eq. 11)}$$

The value of f_A should be equal to f'_A. However, f_A may be chosen 1% smaller than f'_A to compensate for the fact that the overall cascade response is not perfectly symmetrical, i.e., near D.C. (see Figure 6-5).

The values for the coefficients α_0 and α'_0 that set $|H(f_O)|$ = 0 dB in equations 1 and 2 were measured and plotted versus center frequency f_O as shown in Figure 6-6. Three equations corresponding to three linear approximations result:

$$\alpha_0 = \alpha'_0 = \frac{(104/319)f_O - 78.62}{32767} \qquad 400 \le f_O \le 1100 \text{ Hz} \qquad \text{(Eq. 12a)}$$

$$\alpha_0 = \alpha'_0 = \frac{(44/275)f_O + 104}{32767} \qquad 1100 \le f_O \le 1650 \text{ Hz} \qquad \text{(Eq. 12b)}$$

$$\alpha_0 = \alpha'_0 = \frac{(4/45)f_O + 221}{32767} \qquad 1650 \le f_O \le 3000 \text{ Hz} \qquad \text{(Eq. 12c)}$$

By leaving α_1, α_2, α'_1, and α'_2 at zero, the filter acts like the filter in the R96F/R96FI/R96MD. A more sophisticated filter design method may be used to set zeros using α_1, α_2, α_1', and α'_2.

6.1.2 Energy Averaging Filter

The coefficients of the energy averaging filter are determined by a Z-domain approximation to an RC circuit of transfer function $H(S) = 1/(1 + S\tau)$:

$$\alpha'' = \frac{1}{1 + f_S\tau} \qquad \text{(Eq. 13)}$$

$$\beta'' = \frac{1}{(1 + 1/f_S\tau)} \qquad \text{(Eq. 14)}$$

Upon power up, α'' and β'' are set for τ= 0.1 seconds. Unless different tone detector response times are required, these coefficients need not be changed. In Group 2, voice mode, and ADPCM modes, the coefficients should be changed to compensate for a f_S not equal to 9600 Hz.

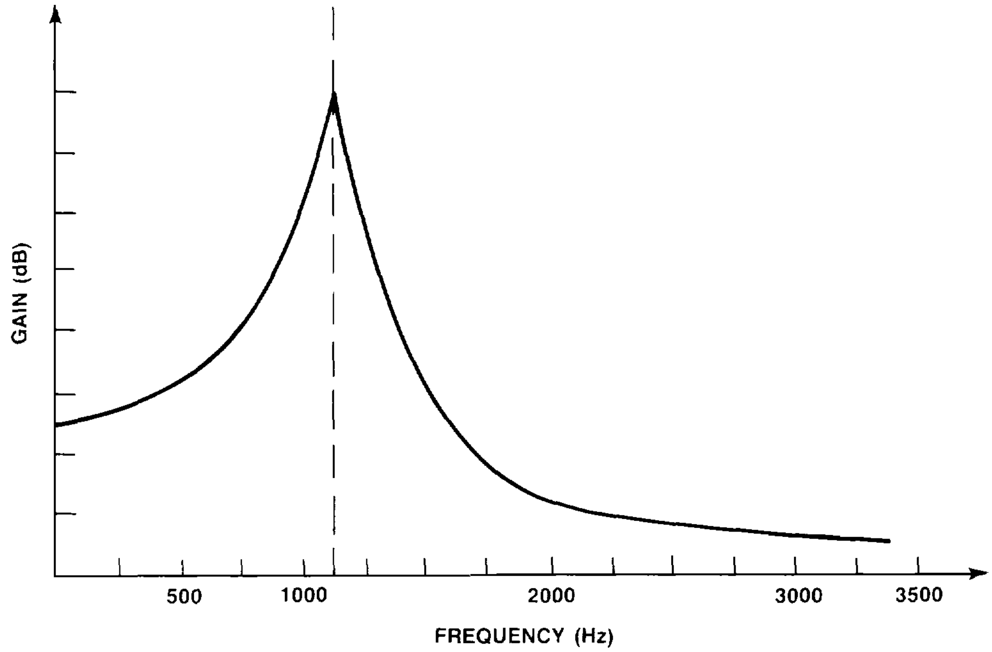


Figure 6-2. Typical Single Filter Response

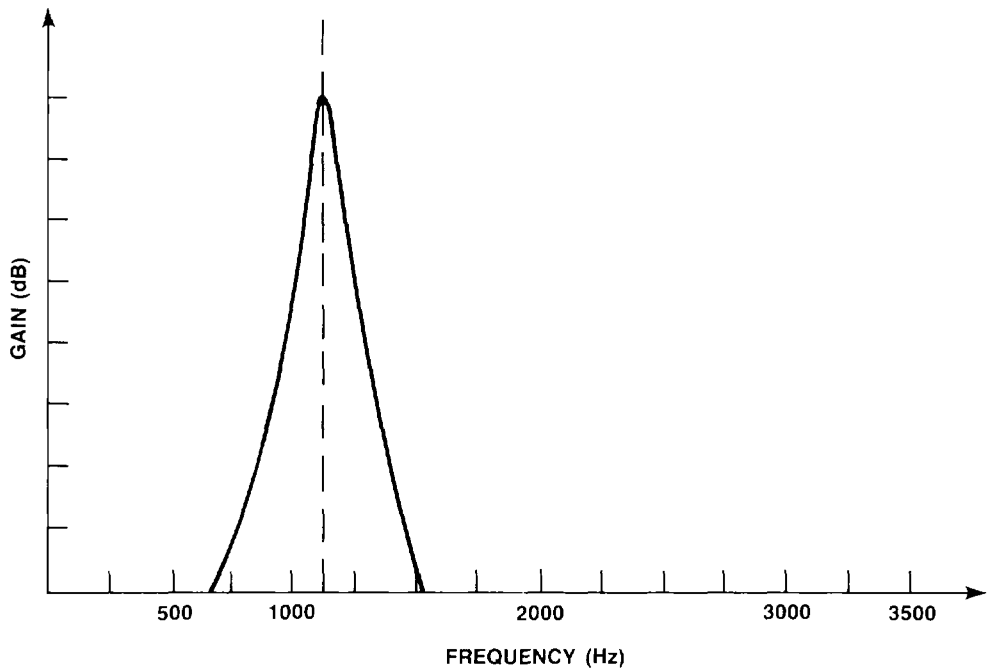


Figure 6-3. Typical Cascade Filter Response

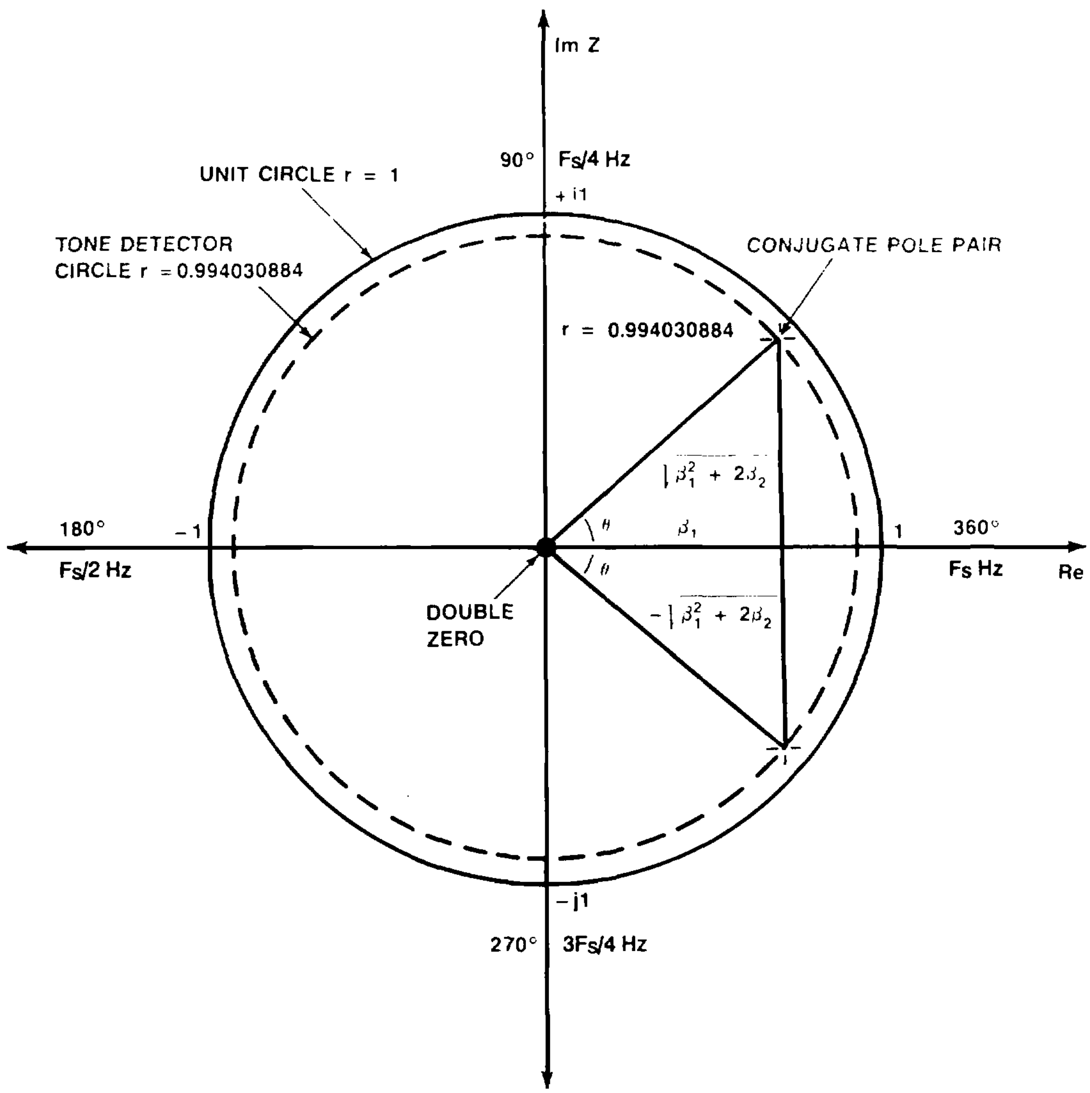


Figure 6-4. Z-Plane Pole-Zero Diagram

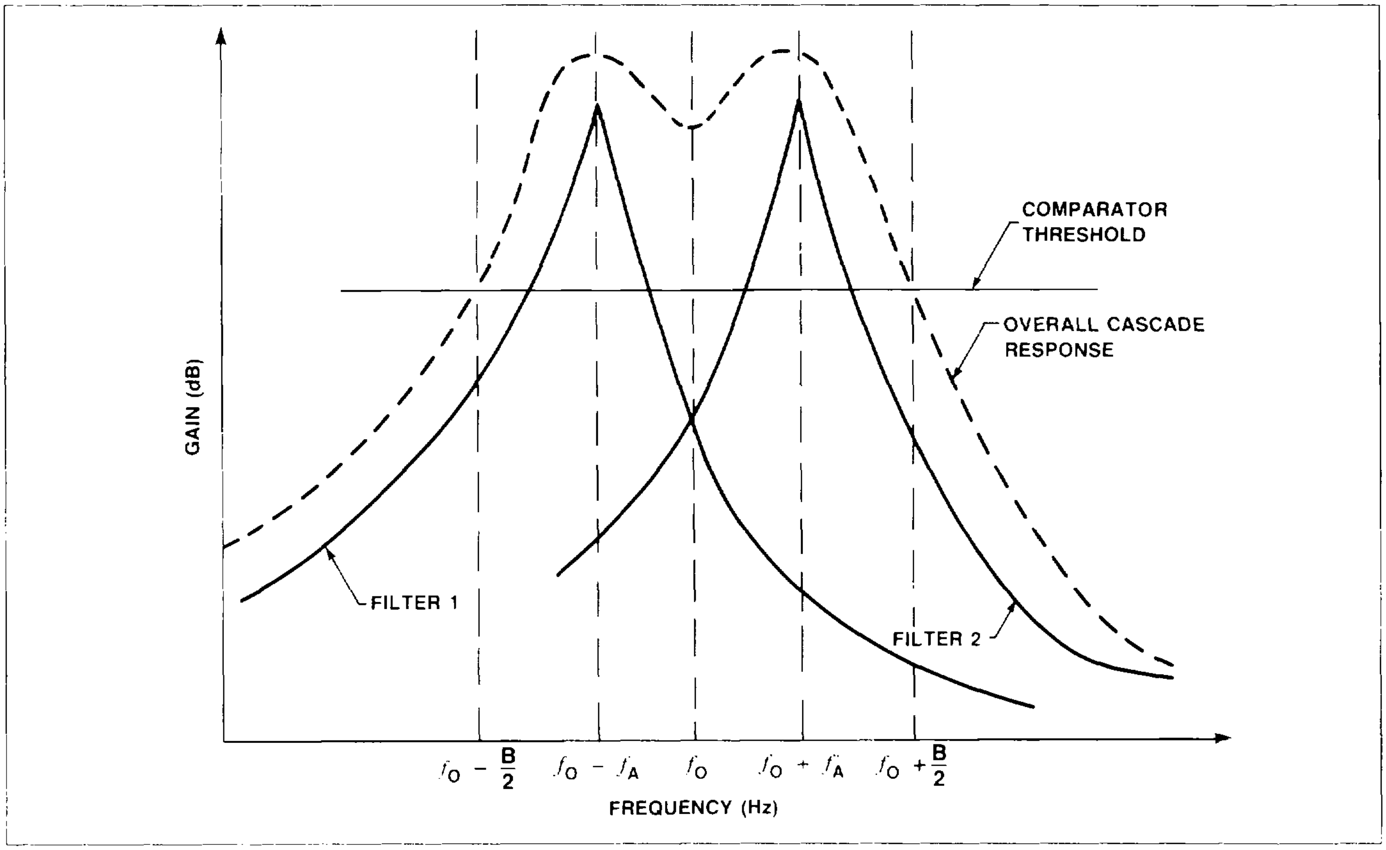


Figure 6-5. Bandwidth and Offset Frequencies

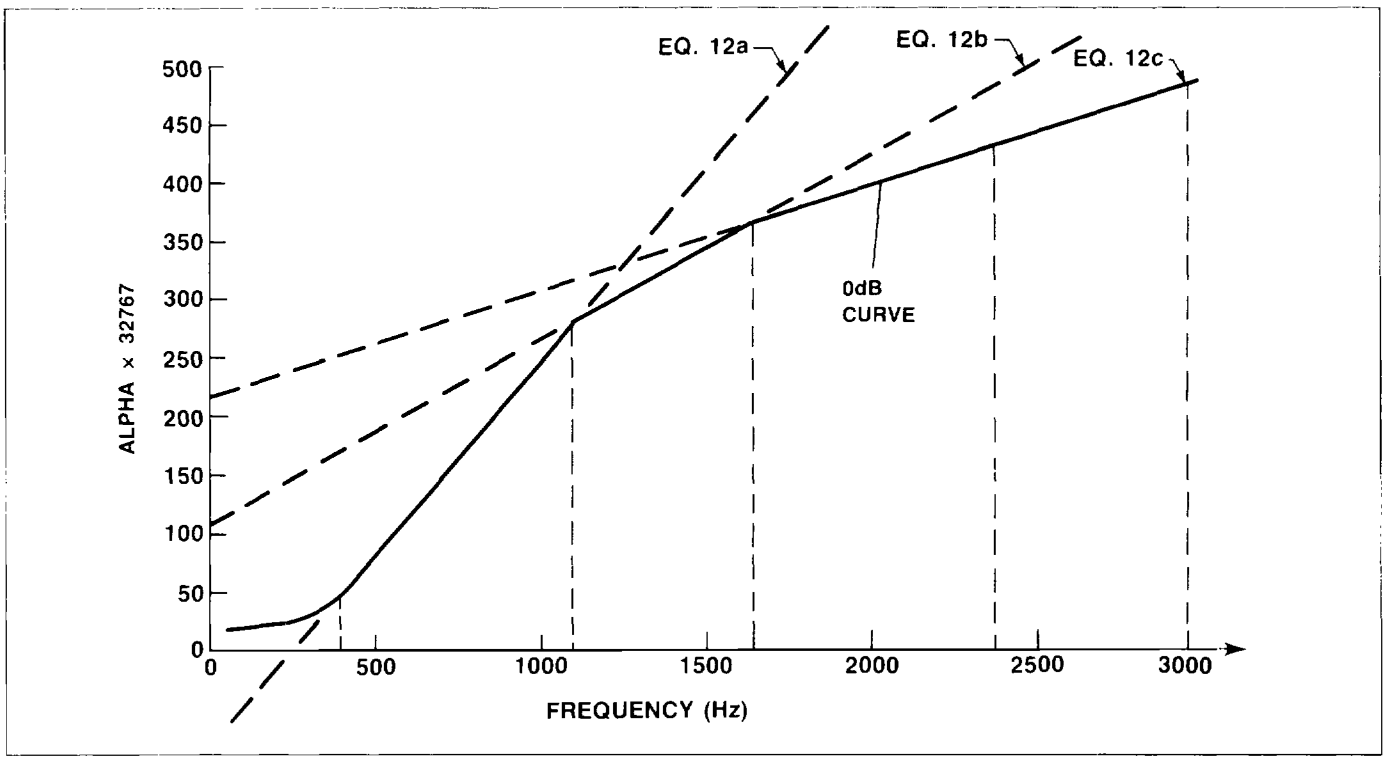


Figure 6-6. Alpha-zero Center Frequency

6.1.3 Filter Coefficients

Table 6-1 contains the RAM access codes for all filter coefficients. Refer to Section 4.1.2 for the proper procedure for writing new coefficients into the RAM locations.

Table 6-2 contains the computed values of the filter coefficients, including those of default frequencies 462 Hz, 1100 Hz, and 2100 Hz. The value 32767 (7FFFh) is full scale in the DSP's machine units (i.e., 32767 = unity). Coefficients may range from −1 to +1 (8001h to 7FFFh) in machine units).

6.2 TONE DETECTORS IN GROUP 2

Because the sampling rate in Group 2 is 10368 Hz, the tone detector coefficients must be re-programmed when using Group 2. The energy averaging filter coefficients change as follows:

$$\alpha'' = \frac{1}{1 + 10368\tau}$$

$$\beta'' = \frac{1}{(1 + 1/10368\tau)}$$

For a tone detector response time of 0.1 seconds (τ=0.1 sec.), set α'' = 0020h and β'' = 7FE0h.

The Group 2 receiver uses a different Automatic Gain Control (AGC) algorithm. For optimum tone detector response time, the Group 2 AGC should be run in the fast mode [G2FGC (bit 0D:3) = 1].

Use the filter coefficients in Table 6-3 to detect Group 2 signals. The frequencies listed are those used in Group 2 transmission (i.e., 1650 Hz: CFR tone; 1100 Hz: EOM tone). To detect frequencies besides those selected, configure the modem in non-Group 2 mode and use equations accordingly.

Table 6-1. Filter Coefficent RAM Access Codes

Coefficient Name	RAM Access Code (Hex) Tone 1	Tone 2	Tone 3	Read Register
α_0	25	2B	31	2,3
α_1	26	2C	32	2,3
α_2	27	2D	33	2,3
α'_0	28	2E	34	2,3
α'_1	29	2F	35	2,3
α'_2	2A	30	36	2,3
β_1	A6	AC	B2	0,1
β_2	A7	AD	B3	0,1
β'_1	A9	AF	B5	0,1
β'_2	AA	B0	B6	0,1
α''	A8	AE	B4	0,1
β''	A5	AB	B1	0,1

Notes:

1. In all cases, CRx (x= 1, 2) = 1
   BRx (x= 1, 2) = 0
   IOx (x= 1, 2) = 0
2. If the most significant bit (MSB) of the address is a 0, the data is written to XRAM; if the MSB is a 1, the data is written to YRAM.

Table 6-2. Calculated Coefficient Values

Frequency Detected	Coefficient Name	Coefficient Value (Hex)	Coefficient Value (Decimal)
2100 Hz ±25 Hz	$\alpha_0 = \alpha'_0$	0198	408/32767
	β_1	1A4A	6730/32767
$f_A \cong 18$ Hz	β'_1	175A	5978/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1850 Hz ±24 Hz	$\alpha_0 = \alpha'_0$	0180	384/32767
	β_1	2E37	11831/32767
$f_A \cong 18$ Hz	β'_1	2B69	11113/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1650 Hz ±23 Hz	$\alpha_0 = \alpha'_0$	0170	368/32767
	β_1	3D48	15688/32767
$f_A \cong 18$ Hz	β'_1	3AA6	15014/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1100 Hz ±30 Hz	$\alpha_0 = \alpha'_0$	0118	280/32767
	β_1	60BE	24754/32767
$f_A \cong 19$ Hz	β'_1	5E9C	24220/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
462 Hz ±14 Hz	$\alpha_0 = \alpha'_0$	0048	72/32767
	β_1	79F3	31219/32767
$f_A \cong 10$ Hz	β'_1	7974	31092/32767
	$\beta_2 = \beta'_2$	C083	–16253/32767

Table 6-3. Calculated Coefficient Values for Group 2

Frequency Detected	Coefficient Name	Coefficient Value (Hex)	Coefficient Value (Decimal)
1850 Hz ± 24 Hz	α_0	0060	96/32767
	α'_0	0180	384/32767
$f_A \cong 18$ Hz	β_1	388C	14476/32767
	β'_1	360C	13836/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1650 Hz ±23 Hz	α_0	0045	69/32767
	α'_0	0175	368/32767
$f_A \cong 18$ Hz	β_1	45EA	17898/32767
	β'_1	4349	17300/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
1100 Hz ±30 Hz	α_0	003A	58/32767
	α'_0	0118	280/32767
$f_A \cong 19$ Hz	β_1	64E4	25828/32767
	β'_1	6314	25364/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
462 Hz ± 14 Hz	α_0	0014	20/32767
	α'_0	0048	72/32767
$f_A \cong 10$ Hz	β_1	7A7D	31357/32767
	β'_1	7A0F	31247/32767
	$\beta_2 = \beta'_2$	C0C4	–16188/32767
For all frequencies in	α''	0020	32/32767
Group 2 mode.	β''	7FE0	32736/32767

7 DTMF DIALING WITH AUTO DIALER

The modem includes tunable oscillators that can be used to perform dual-tone multi-frequency (DTMF) dialing. The frequency and amplitude of each oscillator output is under host control. A programmable tone detector can also be used in call establishment to recognize an answer tone.

This section describes the method of oscillator and filter tuning by the host processor and provides an example of an autodialer routine that may be programmed into the host.

7.1 DTMF REQUIREMENTS

EIA Standard RS-496, paragraph 4.3.2, specifies requirements that ensure proper DTMF signaling through the public switched telephone network (PSTN). These tones consist of two sinusoidal signals, one from a high group of frequencies and one from a low group of frequencies, that represent each of the pushbutton telephone characters shown in Table 7-1.

Signal power is defined for the combined tones as well as for the individual tones. Both maximum and minimum power requirements are functions of loop current. By combining the various requirements of RS-496, compromise power levels can be determined that meet the power specification for all U.S. lines (when driving the PSTN from a 600 ohm resistive source). The high frequency tone should be at a higher power level than the low frequency tone by approximately 2 dB. The maximum combined power, averaged over the pulse duration, should not exceed +1 dBm. The minimum steady state power of the high frequency tone should not be less than –8 dBm.

Table 7-1. DTMF Signals

Low Frequency	High Frequency			
	1209 Hz	1336 Hz	1477 Hz	1633 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

When connecting the modem circuit to the PSTN by means of a data access arrangement (DAA) set for permissive mode, the DAA gain is –9 dB. The modem circuit must, therefore, drive the DAA input with +1 dBm of steady state high frequency power and –1 dBm of steady state low frequency power in order to meet all of the listed conditions. Since +0.5 dBm is the maximum undistorted power level for individual tones generated by the modem, the user may need to add gain in front of the DAA during DTMF dialing.

The required duration of the DTMF pulse is 50 ms minimum. By experience, a pulse duration of approximately 95 ms is more reliable. The required interval between DTMF pulses is 45 ms minimum and 3 seconds maximum. Again, by experience, an interdigit delay of approximately 70 ms is preferred.

The remaining requirements of RS-496, relative to DTMF dialing, are not influenced by the host processor. These requirements are all met by the modem's oscillators.

7.2 SETTING OSCILLATOR PARAMETERS

The oscillator frequency and output power are set by the host computer in DSP RAM using the microprocessor bus and diagnostic data routine.

To generate a DTMF tone, place the modem into TONE configuration (CONF = 80h). The user must program the frequencies and the levels of each tone. To set the frequency of tone 1, write a 16-bit hexadecimal number into RAM using RAM access code 21h with BRx=0 and CRx=1. When setting the frequency of tone 2, use the same procedure with the RAM access code 22h with BRx=0 and CRx=1. Set the power levels of tone 1 by writing a 16-bit hexadecimal number into RAM using RAM access code 22h with BRx=0 and CRx=0. The RAM access code for the power level of tone 2 is 23h with BRx=0 and CRx=0.

The hexadecimal numbers written into these RAM locations are scaled as follows:

Frequency number = 6.8267 (desired frequency in Hz)

Power number = $18426^{[10(P_O/20)]}$

Where P_O = output power in dBm with a 600 ohm load termination. If terminating with a series 600 ohm resistor into a 600 ohm load, add 6 dB to the output power before using the above equation.

These decimal numbers must be converted to hexadecimal form then stored in RAM (see RAM data write routine).

Hexadecimal numbers for DTMF generation are listed in Table 7-2. Power levels are selected to give the desired output power for each tone (–1 dBm for the high frequency tone and –3 dBm for the low frequency tone if terminated with a series 600 Ω resistor into a 600 Ω load) while compensating for modem filter characteristics.

Table 7-2. DTMF Parameters

Digit	ADDx	CRx	BRx	Value (Hex)
0	21	1	0	1918
	22	1	0	23A0
	22	0	0	65AB
	23	0	0	7FFF
1	21	1	0	1296
	22	1	0	203D
	22	0	0	65AB
	23	0	0	7FFF
2	21	1	0	1296
	22	1	0	23A0
	22	0	0	65AB
	23	0	0	7FFF
3	21	1	0	1296
	22	1	0	2763
	22	0	0	65AB
	23	0	0	7FFF
4	21	1	0	1488
	22	1	0	203D
	22	0	0	65AB
	23	0	0	7FFF
5	21	1	0	1488
	22	1	0	23A0
	22	0	0	65AB
	23	0	0	7FFF
6	21	1	0	1488
	22	1	0	2763
	22	0	0	65AB
	23	0	0	7FFF
7	21	1	0	16B8
	22	1	0	203D
	22	0	0	65AB
	23	0	0	7FFF
8	21	1	0	16B8
	22	1	0	23A0
	22	0	0	65AB
	23	0	0	7FFF
9	21	1	0	16B8
	22	1	0	2763
	22	0	0	65AB
	23	0	0	7FFF

Table 7-2. DTMF Parameters (Cont'd)

Digit	ADDx	CRx	BRx	Value (Hex)
*	21	1	0	1918
	22	1	0	203D
	22	0	0	65AB
	23	0	0	7FFF
#	21	1	0	1918
	22	1	0	2763
	22	0	0	65AB
	23	0	0	7FFF
A	21	1	0	1296
	22	1	0	2B8C
	22	0	0	65AB
	23	0	0	7FFF
B	21	1	0	1488
	22	1	0	2B8C
	22	0	0	65AB
	23	0	0	7FFF
C	21	1	0	16B8
	22	1	0	2B8C
	22	0	0	65AB
	23	0	0	7FFF
D	21	1	0	1918
	22	1	0	2B8C
	22	0	0	65AB
	23	0	0	7FFF

7.3 DETECTING ANSWER TONE

Frequency detector bit FR1 (08:5) can be used to detect a 2100 Hz answer tone when connection to the remote modem is successful. Bit FR1 goes active (one) when energy above the turn-on threshold is present at 2100 Hz ±25 Hz. At the end of the answer tone, FR1 returns to zero and data transmission can begin. Note that FR1 is not functional in V.29 or V.27 ter configurations.

7.4 COMPLETE CALLING SEQUENCE

A complete calling sequence consists of several steps including modem configuration, telephone number selection, DTMF transmission, and answer tone detection. A sample flow chart for implementing an auto-dialer in host software is illustrated in Figure 7-1.

The auto-dialer routine may be entered at one of two points; either AUTO DIAL or REDIAL. When entering at AUTO DIAL, the host prompts the user to enter a phone number, which is then stored in the phone number buffer. When entering at REDIAL, the routine dials the number previously stored in the phone number buffer and does not issue a user prompt.

Interrupts not required during dialing are disabled to prevent errors in real time delays. Interrupt status is saved to allow restoring these interrupts when dialing is complete. The current modem configuration is saved prior to selecting the DTMF Transmit configuration, then restored at the completion of the auto-dialer routine to allow data transfer.

The commands for off-hook and request coupler cut through are typical of signals required by data access arrangements that may be connected to the modem for switched network operation.

Since the number to be dialed varies in length depending on the requirements of various PBX equipment, domestic telephone companies, and foreign PTTs, the number buffer must allow for numbers of different length. The method used in Figure 7-1 to determine the end of valid bytes in the buffer is zero recognition. After the last digit is entered, the carriage return must place a 00h (ASCII NUL character) in the buffer. All other bytes must be non-NUL ASCII characters. Only numeric characters (ASCII 30 through 39) are printed and dialed. Non-numeric characters are tested for comma and NUL. Comma causes a 2-second pause in dialing to allow for known delays in the telephone network or PBX. NUL ends the dialing portion of the routine and begins the answer tone detection portion. All other characters are ignored.

The answer tone detection logic allows 30 seconds for 2100 Hz recognition. If answer tone is not recognized within this time limit, the call is aborted. If answer tone is recognized, the routine jumps to the data handling software.

7.5 SINGLE TONE GENERATION

In OEM equipment that combines the features of a modem with those of a telephone handset, the tone generators may be used to generate a caller reassurance tone (or even music) while the caller is kept on hold. To generate a single tone, make sure one of the oscillators is set to zero frequency or zero amplitude while the other oscillator is set to the desired frequency and amplitude. Common parameters for single tone generation are listed in Table 7-3.

Table 7-3. Common Single Tone Parameters

Parameter	Frequency	Value (Hex)
CED	2100 Hz	3800
CNG	1100 Hz	1D55

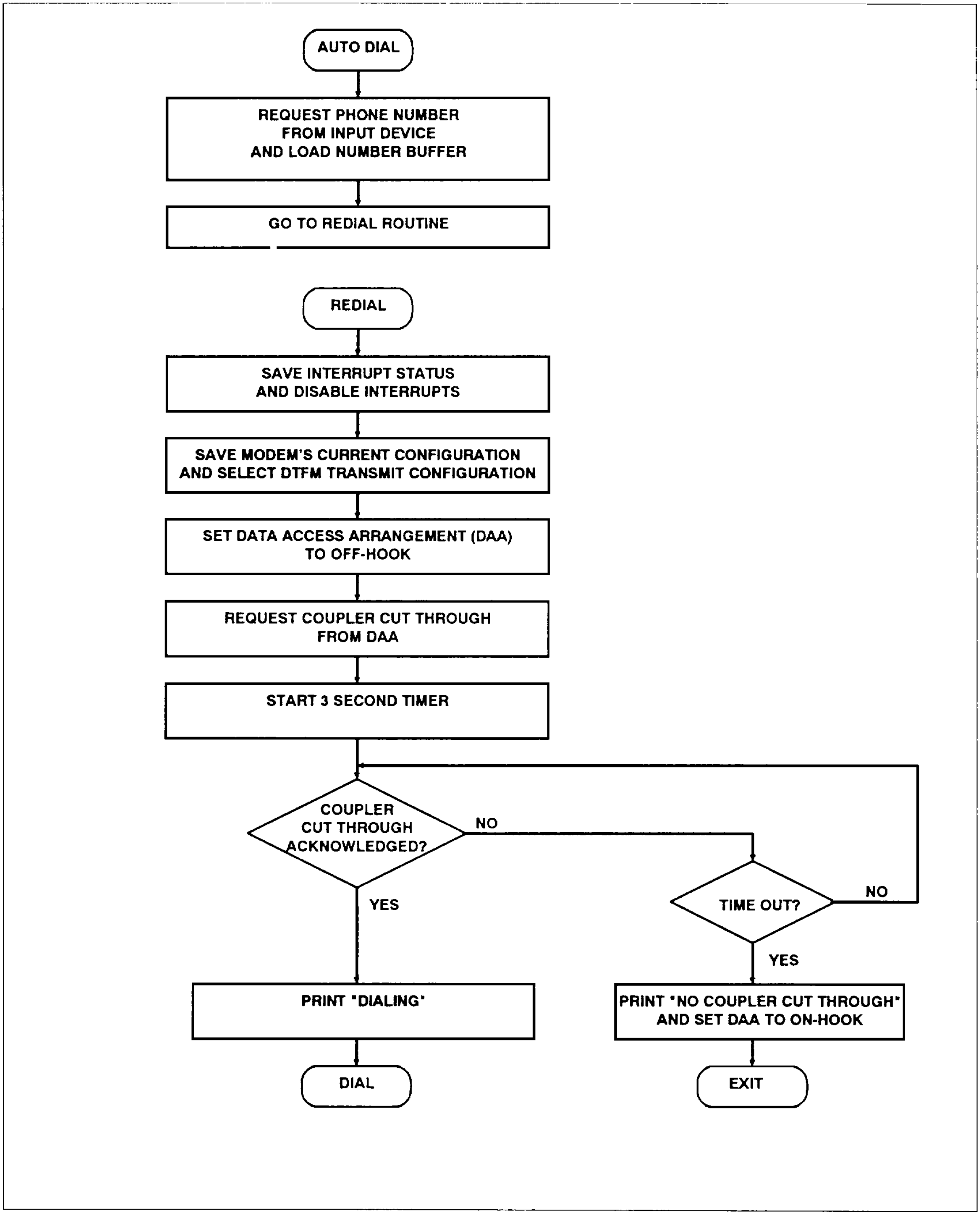


Figure 7-1. Autodialer Flow Chart

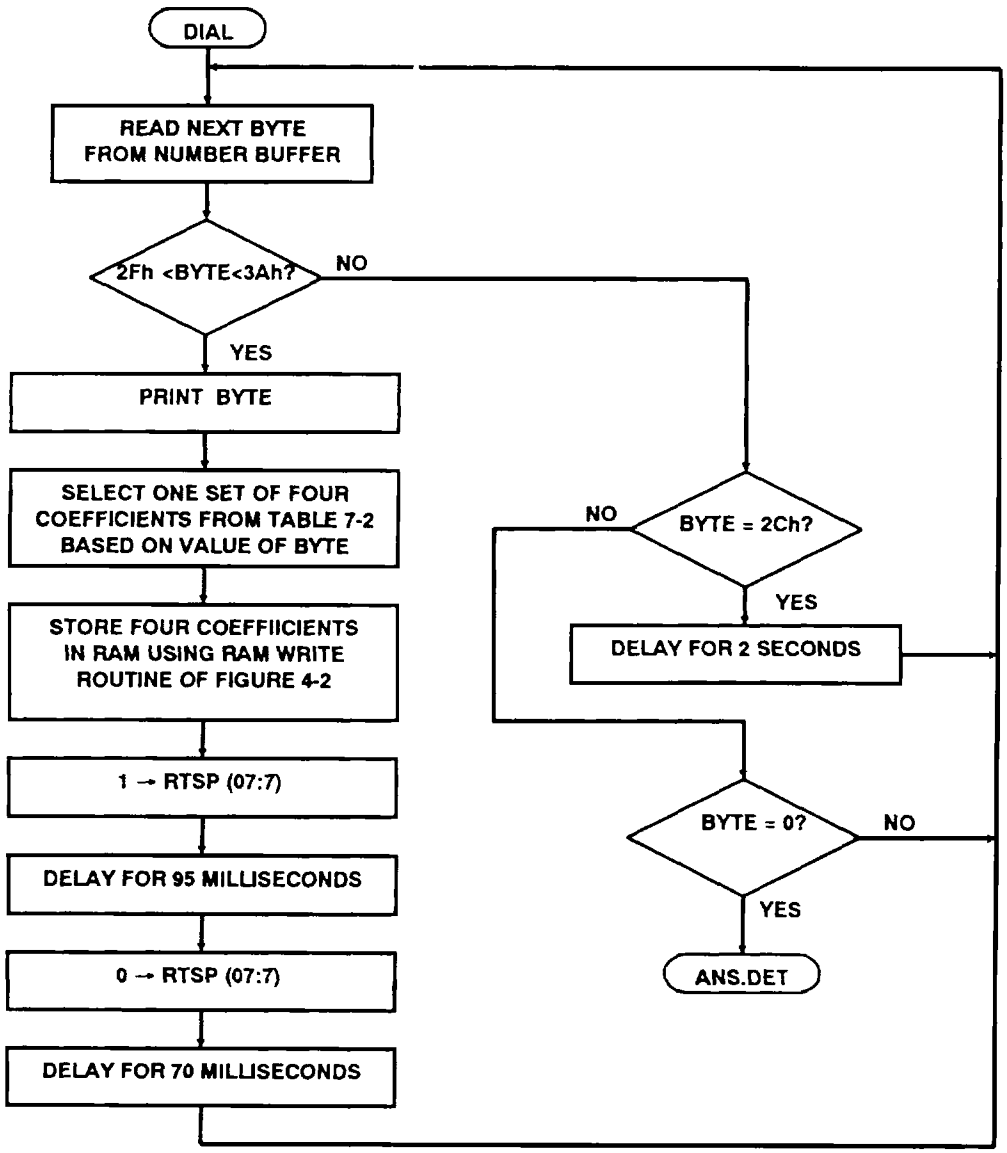


Figure 7-1. Autodialer Flow Chart (Cont'd)

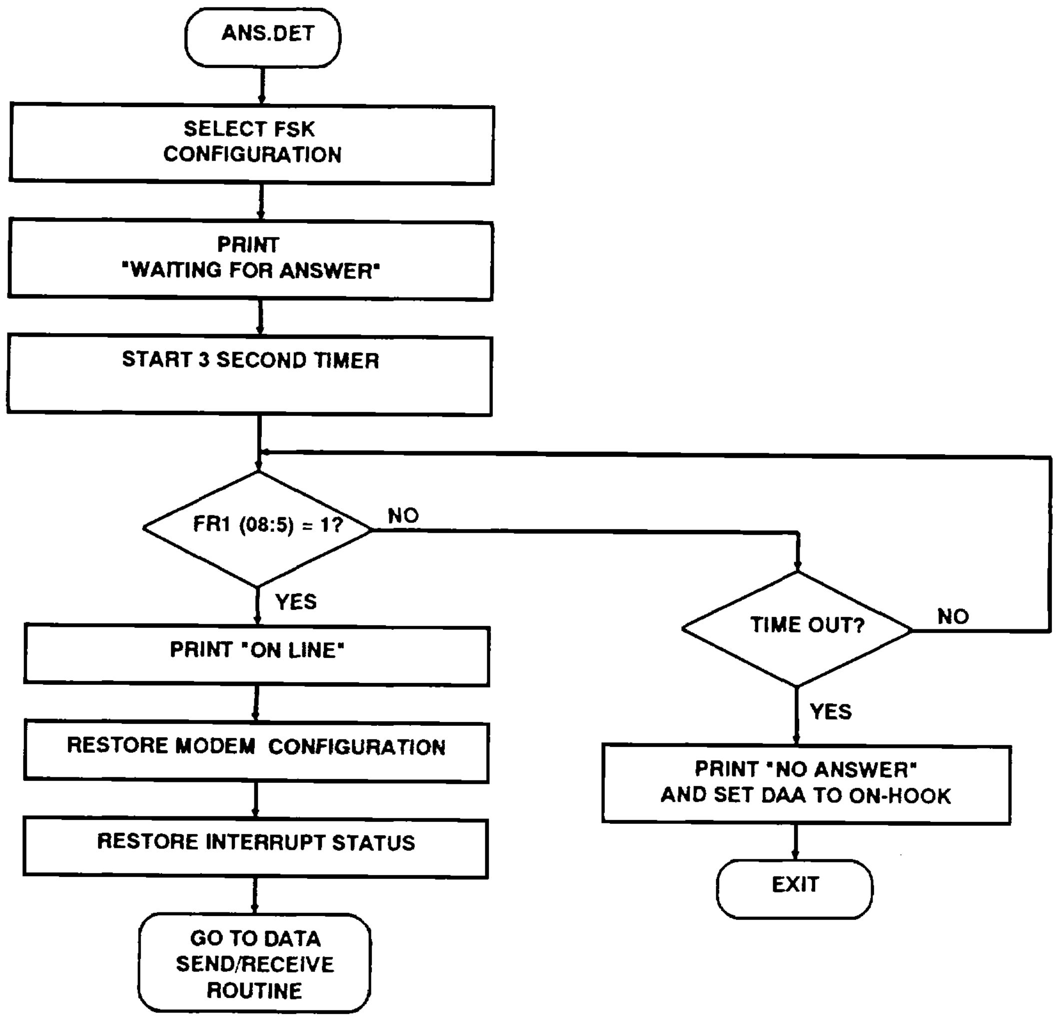


Figure 7-1. Autodialer Flow Chart (Cont'd)

8 RECOMMENDED RECEIVE SEQUENCE FOR GROUP 2 FACSIMILE

The modem includes a transmit and receive configuration that is compatible with the transmission scheme of Group 2 facsimile equipment. In order to achieve the best results with Group 2 reception, the following procedure is recommended. The step numbers are keyed to points in Figure 8-1.

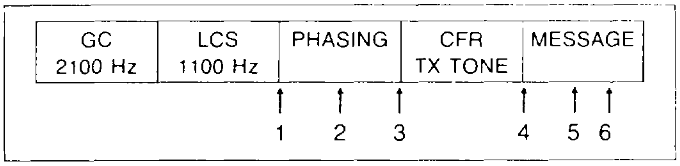


Figure 8-1. Group 2 Facsimile Sequence

8.1 METHOD

1. Enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Write 0038h using access code 0Dh, CRx = 0. This action sets the Group 2 phase-locked-loop (PLL) for a frequency correction of 9 Hz, causing the phase term to drift rapidly to overcome any tendency to slow phase recovery.
   b. Write 4000 using access code 19h, CRx = 0, and 7FFFh using access code 99h, CRx = 0. This action allows the Group 2 PLL to accept the greatest number of samples for carrier recovery during phasing.
   c. Write 2000h using access code 05h, CRx = 1. This action sets the AGC slew rate for very fast acquisition.
   d. Set control bit G2FGC (0D:3) to a one to select fast AGC state.
2. After phasing is detected, wait approximately 2 seconds for the AGC circuit to settle. Then:
   a. Write 0000h using access code 05h, CRx = 1. This action stops AGC tracking in order to preserve the present AGC setting.
   b. Reset control bit G2FGC (0D:3) to a zero to select slow AGC state. This action changes the Group 2 PLL characteristics to match reduced AGC response.
   c. Read and save the 16-bit value from registers 3 and 2 using access code 0Dh, CRx = 0. This value represents the frequency error term from the Group 2 PLL.
   d. Verify that phasing signal is still being received. This action guarantees that AGC value was frozen during phasing signal.
   e. If step d above determines that phasing signal is present, allow transmission of CFR. If phasing signal is not present, suppress CFR.
3. Exit Group 2 configuration.
4. At completion of CFR transmission, re-enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Repeat step 1.b.
   b. Repeat step 2.a.
   c. Add 0038h to the value saved in step 2.c above and write the sum using access code 0Dh, CRx = 0. This action forces a 9 Hz error as in step 1.a.
5. Wait for start of Group 2 message transmission. Then:
   a. Write 0400h using access code 05h, CRx = 1. This action restores the AGC slew rate to the default value.
   b. After 2 lines, write the value saved in step 2.c using access code 0Dh, CRx = 0. This action removes the 9 Hz forced frequency error without waiting for the phase-locked-loop to complete the correction. This step is optional as the correction will eventually be completed, but, depending on the percentage of white in the document being sent, the correction may take from 4 to 6 lines (100 ms of white required).
6. After approximately 6 to 10 seconds of message reception, perform either step a or step b below:
   a. Write 6100h using access code EFh, and 0600h using access code 19h, CRx = 0. This action places narrow limits on the received signal used for carrier recovery during message reception and reduces the chance of errors caused by repeated patterns in the message.
   b. Synchronize the modem's Group 2 PLL to the facsimile machine's blanking signal as follows:
      (1) Freeze the phase-locked-loop during data by:
         (a) Writing 7FFFh using access code 19h, CRx = 0.
         (b) Writing 0000h using access code 99h, CRx = 0.
      (2) Enable the phase-locked-loop during the white margins by:
         (a) Writing 4000h using access code 19h, CRx = 0.
         (b) Writing 7FFFh using access code 99h, CRx = 0.

(c) The sequence of writing in step 6.b is important and must be performed as described. Option 6.b requires more action by the host processor, but it eliminates the possibility of data patterns affecting carrier recovery.

8.2 PARAMETER SCALING

1. Access code 0Dh, CRx = 0 represents frequency error, i.e., the deviation of received carrier from 2100 Hz.

   LSB = 0.167 Hz; Range = ± 140 Hz.

2. Access code 18h, CRx = 0 represents the Group 2 PLL slew rate for the first order term. The number is directly proportional to slew rate. The range of stable operating values is 0010h to 7000h.

3. Access code 05h, CRx = 0 represents the AGC slew rate.

   Range = 0000h to 7FFFh.

   Scaling: See Section 4.

4. Access codes 19h and 99h, CRx = 0, represent limits on acceptable zero crossing for use by the carrier recovery loop. The carrier recovery loop uses several nonlinear controls in attempting to lock the zero crossing of the local carrier to those of the transmitter. Since Group 2 facsimile uses VSB transmission, it is necessary to either reconstruct the upper sideband or exclude those zero crossings that represent frequencies other than 2100 Hz. The modem excludes unwanted zero crossings by testing the effective slope of the waveform as it crosses zero. In Figure 8-2, points A and B represent samples taken about a zero crossing over a sample period T, where T = 1/10,368 seconds.

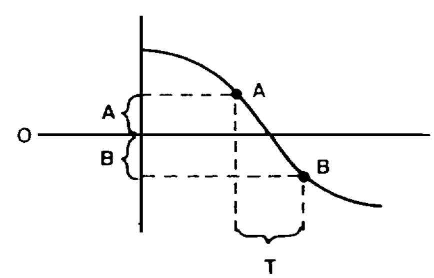


Figure 8-2. Samples of Zero Crossing

The magnitude of [|A| + |B|] is directly proportional to the slope of line segment AB and is, therefore, an indicator of frequency. If H represents the value stored at 19h, CRx = 0 and L represents the value at 19h, CRx = 0, then 1 – [|A| + |B|] + H + L must be greater than positive full scale or the frequency is excluded for being too high.

The average value for 1 – [|A| + |B|] with an all white transmission and back-to-back connection is 19A1h ± 0543h.

5. Access code 1Ah, CRx = 0 allows host control of the limits placed on phase error correction. When the phase error exceeds the limit set by 1Ah, CRx = 0, PLL updating is suspended. The default value of 5000h corresponds to a limit of ± 27.34 degrees. A zero in 1Ah, CRx = 0 causes the PLL to update for any phase error. By setting. By resetting 1Ah, CRx = 0 to a zero, it may be unnecessary to force a frequency offset in the receive sequence.

For systems using step 6.a in the receive sequence, reception of messages containing a large amount of black may be improved by setting 1A, CRx = 0 to zero. 1A, CRx = 0 scaling is:

Phase limit = 360° – (2100/10386) x A

Where A = [7FFFh - (1Ah, CRx = 0 value)h]/7FFFh

Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits, etc.

8.3 BLACK/WHITE THRESHOLD

The modem receives a Group 2 baseband signal that contains density (gray scale) information in the amplitude modulation. In order for this information to be used on a Group 3 facsimile machine, the modem converts the gray scale to black/white baseband form. The threshold at which the black/white decision is made determine the density of the received page.

Access code 24h, CRx = 0 represents the Group 2 black/white threshold. This location defaults to 7200h at POR time. The number may be increased or decreased by the host to achieve a page weighted more toward white or toward black, respectively.

9 T.30 IMPLEMENTATION

9.1 GENERAL

CCITT Recommendation T.30 details procedures for facsimile transmission over the PSTN. This standard describes how to initiate, complete, and end a fax transmission. This section describes methods to set up host software to implement T.30 with the R96EFX, R96DFX, or R96VFX MONOFAX modem.

A basic block diagram of a Group 3 facsimile machine is shown in Figure 9-1. The MONOFAX modem performs the modulation/demodulation process. The fax machine manufacturer must implement the interface between the modem (T.30), the data compression/decompression (T.4), and the interface to the scanner and printer.

There are five phases (A-E) to the T.30 facsimile protocol. Phase A is the call setup, in which both facsimile machines connect to the line. Phase B is a pre-message procedure which consists of identification and command sections. The actual high speed message transmission occurs during Phase C. This is followed by the post-message procedure or Phase D. Both facsimile machines release the line in Phase E.

Figure 9-2 illustrates a typical Group 3 facsimile procedure. This example on T.30 describes a facsimile call where the calling unit (originate) transmits a documents to a called unit (answer). Phase E is not included in this example since it is the call release and both ends hang up.

9.1.1 Phase A

T.30 specifies that call establishment can be realized one of four ways. The four methods of call establishment are: manual-to-manual, manual-to-automatic, automatic-to-manual, and automatic-to-automatic. Manual corresponds to operator or human intervention while automatic means machine only. The explanation that follows describes an automatic-to-automatic example.

The calling unit, or originating fax, first transmits a calling tone (CNG) to indicate it is a non-speech terminal. Figure 9-3 describes how to set up the modem to generate a 1100 Hz (CNG) tone. Figure 9-4 describes how to set up the modem to detect a 1100 Hz tone. The called unit, or answering fax, then responds with a called station ID (CED). Figures 9-5 and 9-6 describe how to accomplish this task. The end of Phase A is signified after the called unit sends a 2100 Hz (CED) tone and the calling unit has detected this tone. Some facsimile manufacturers do not configure the modem to detect these tones. In this case, the modem looks for the preamble of flags (see phase B).

9.1.2 Phase B

The pre-message procedure consists of the handshake. One machine sends an identification signal and the other machine responds with a command signal. A training check is sent at a high speed and the receiving machine informs the transmitting machine if the training check was successful. This usually occurs at V.21 300 bps Frequency Shift Keying (FSK) modulation in HDLC format.

HDLC stands for High level Data Link Control. It is a standard procedure used for data communications. HDLC is a bit-oriented protocol (normally used in synchronous communications) that defines how the data being sent over the data link is organized and arranged.

When using the HDLC protocol, the data is transmitted via frames. These frames organize the data into a format specified by an ISO (International Standards Organization) standard that enables the transmitting and receiving station to synchronize with each other. Figure 9-7 illustrates the HDLC frame structure used for the facsimile protocol.

The preamble is a series of HDLC Flags for one second ±15%. The flag sequence defines the beginning and ending of a frame. The address field is required to provide identification for multi-point addressing. For PSTN the format is 11111111. The control field's purpose is to provide the capability of encoding the commands and responses. The format is 1100X000 (X=0 non-final frame; X=1 final frame).

The HDLC information field provides the specific information for the control and message interchange between the two stations. In the fax protocol the format for the information field consists of two parts, the Facsimile Control Field (FCF) and the Facsimile Information Field (FIF).

The FCF contains information regarding the type of information being exchanged and the position in the overall sequence. The acronyms, functions, and format for FCF commands are defined in the T.30 Recommendation. The FIF contains additional information which further clarifies the facsimile procedure. Some examples of some information communicated with the FIF are: group capability, data rate, vertical resolution, coding scheme, recording width, recording length, and minimum scan line time.

The Frame Check Sequence (FCS) follows the FIF. The modem automatically generates the FCS or Cyclic Redundancy Check (CRC). The frame ends with an ending 7E flag. It is recommended that more than one ending flag be transmitted.

After the modem has been configured for FSK, the Digital Identification Signal (DIS) is transmitted by the called unit. The DIS informs the calling unit about the called unit's capabilities such as group capability (G1, G2, G3), data rate, vertical resolution, coding scheme (Modified Huffman, Modified Read), recording width, recording length, and minimum scan line time. The calling unit then re-

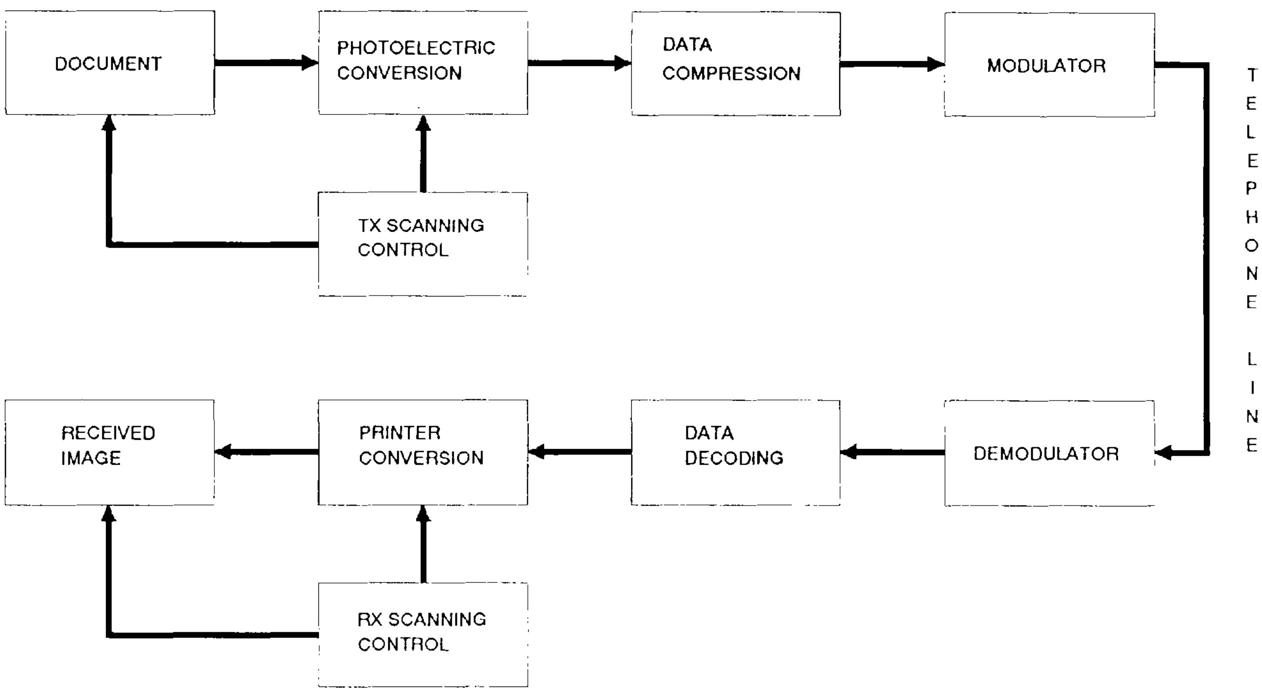


Figure 9-1. Basic Block Diagram of G3 Facsimile

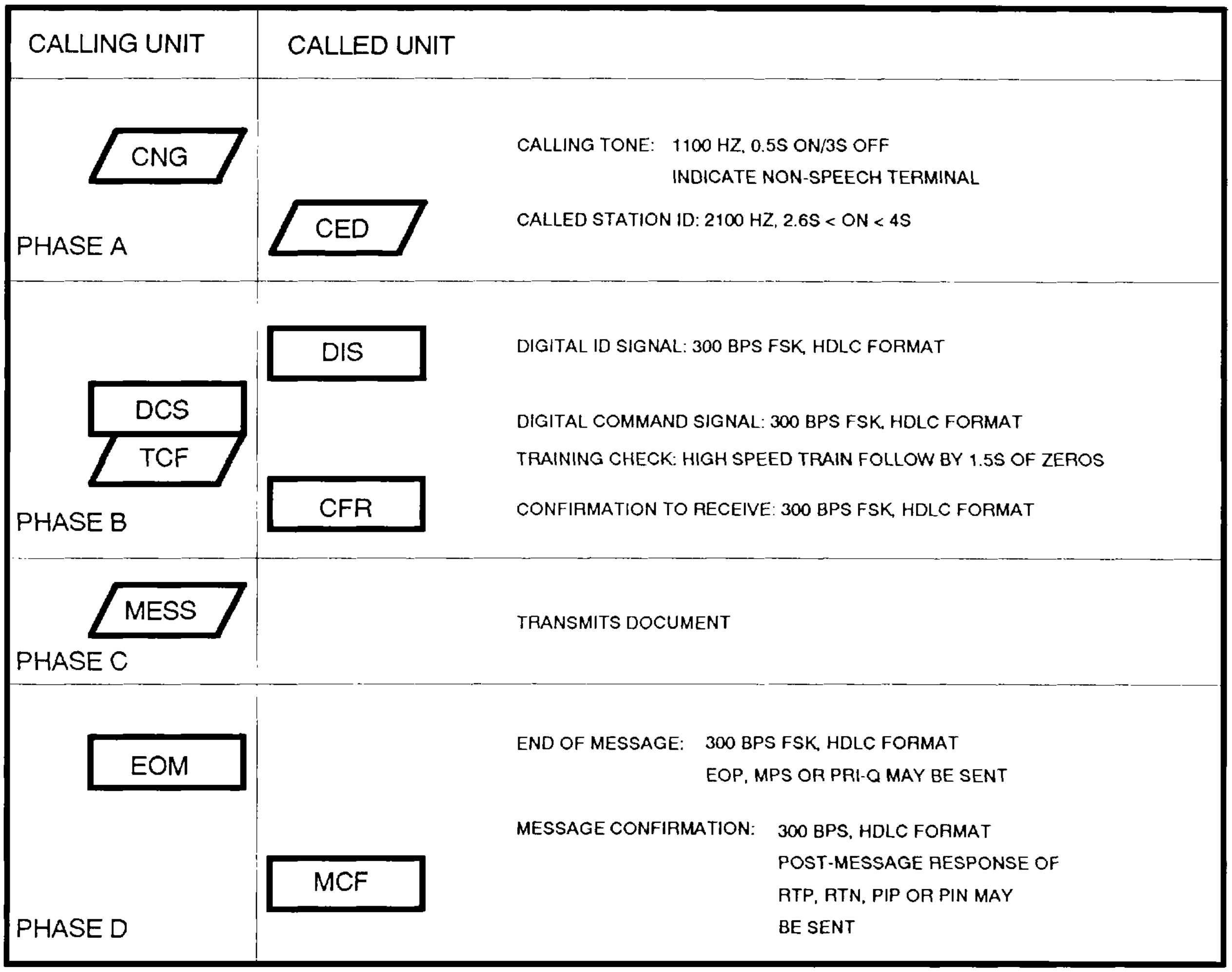


Figure 9-2. G3 Facsimile Procedure

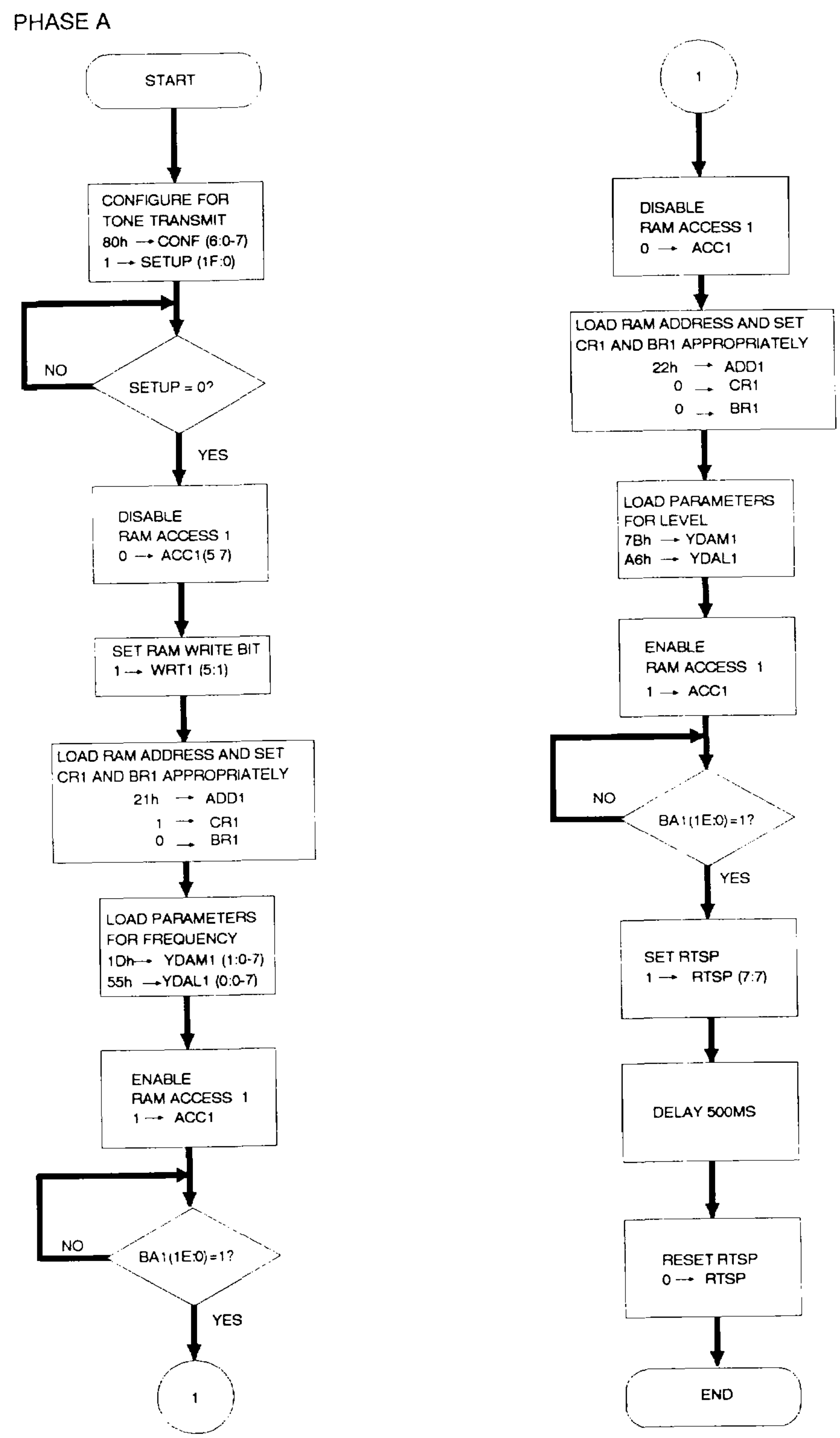


Figure 9-3. Transmit Calling Tone (CNG) 1100 Hz

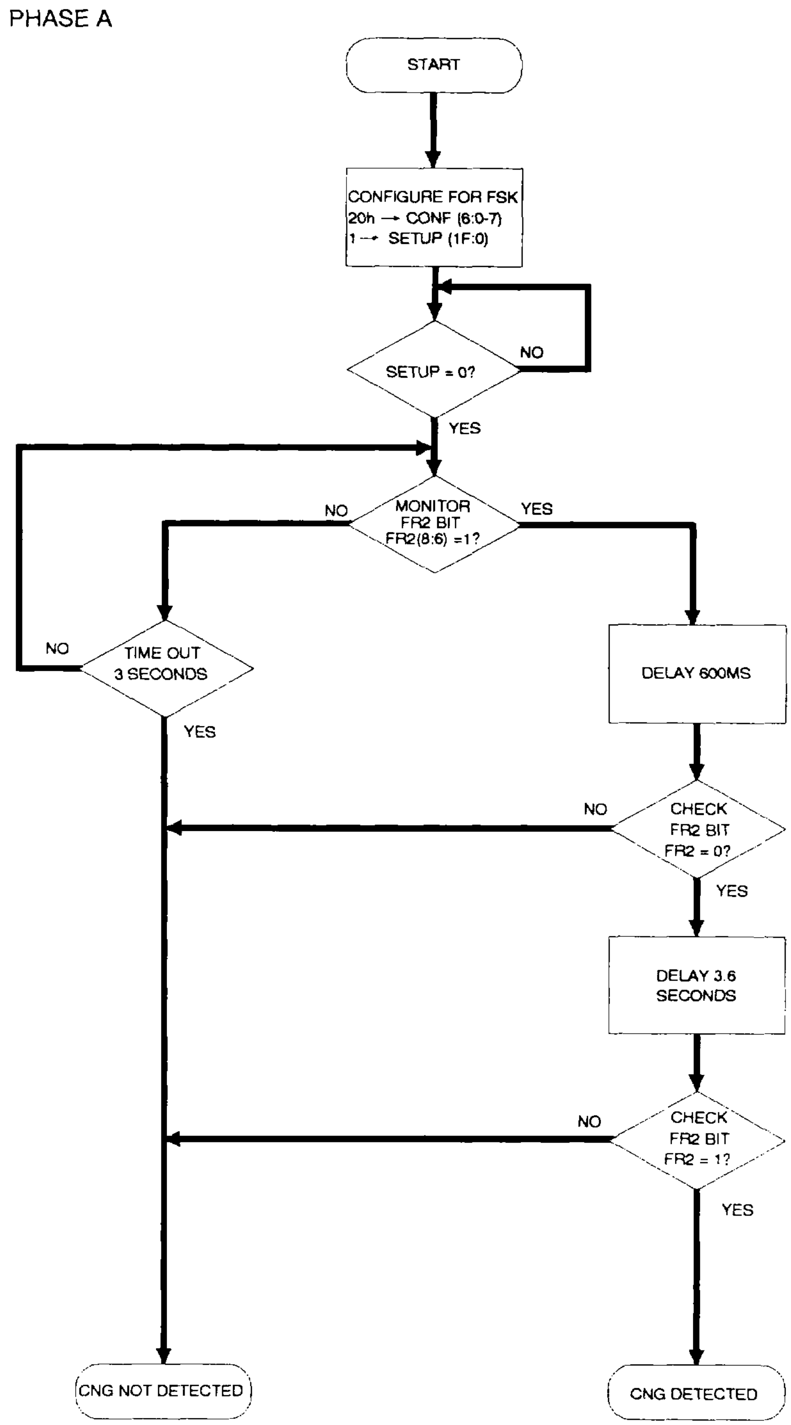


Figure 9-4. Detecting CNG Tone (1100 Hz)

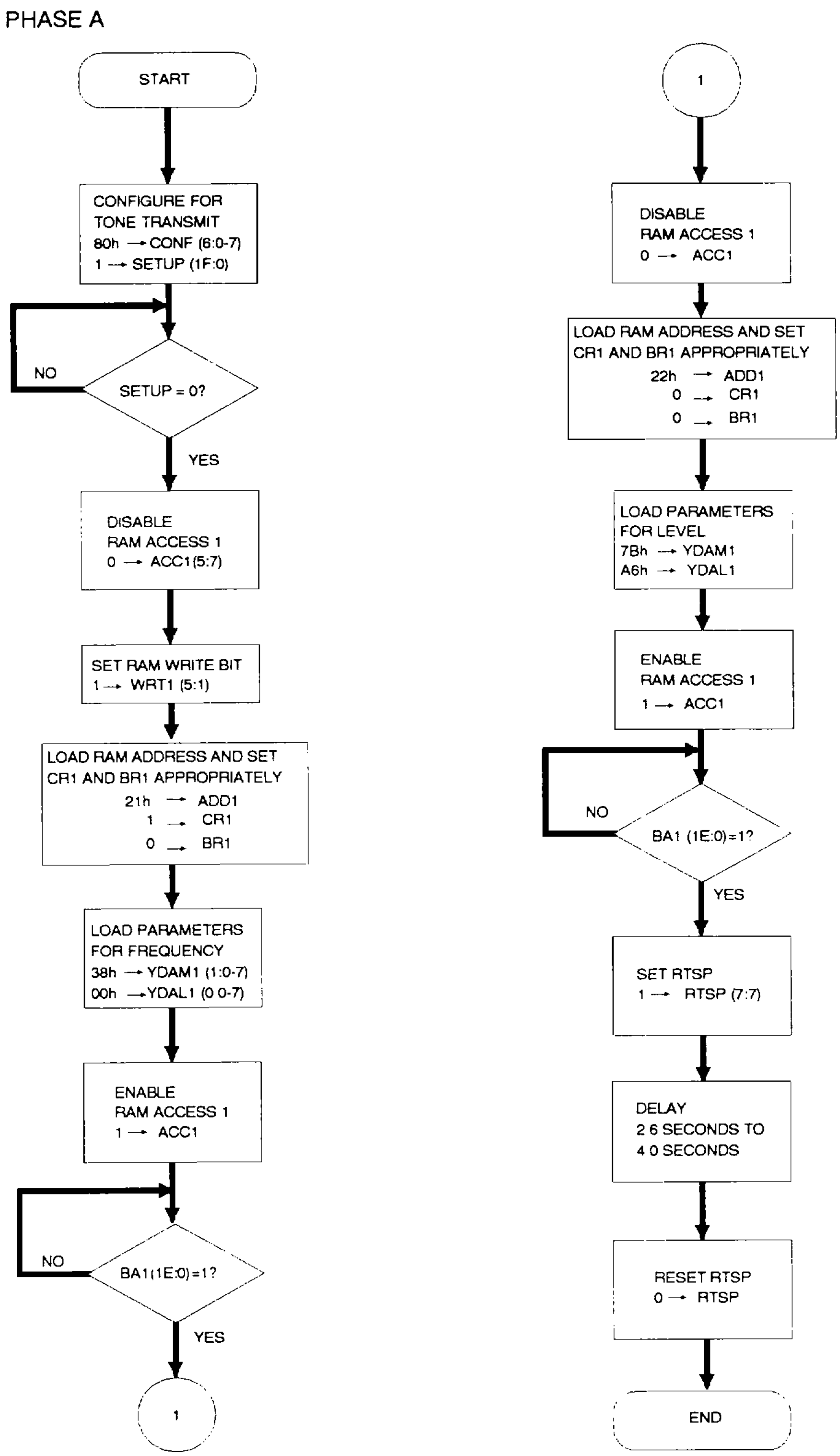


Figure 9-5. Transmit Called Tone (CED) (2100 Hz)

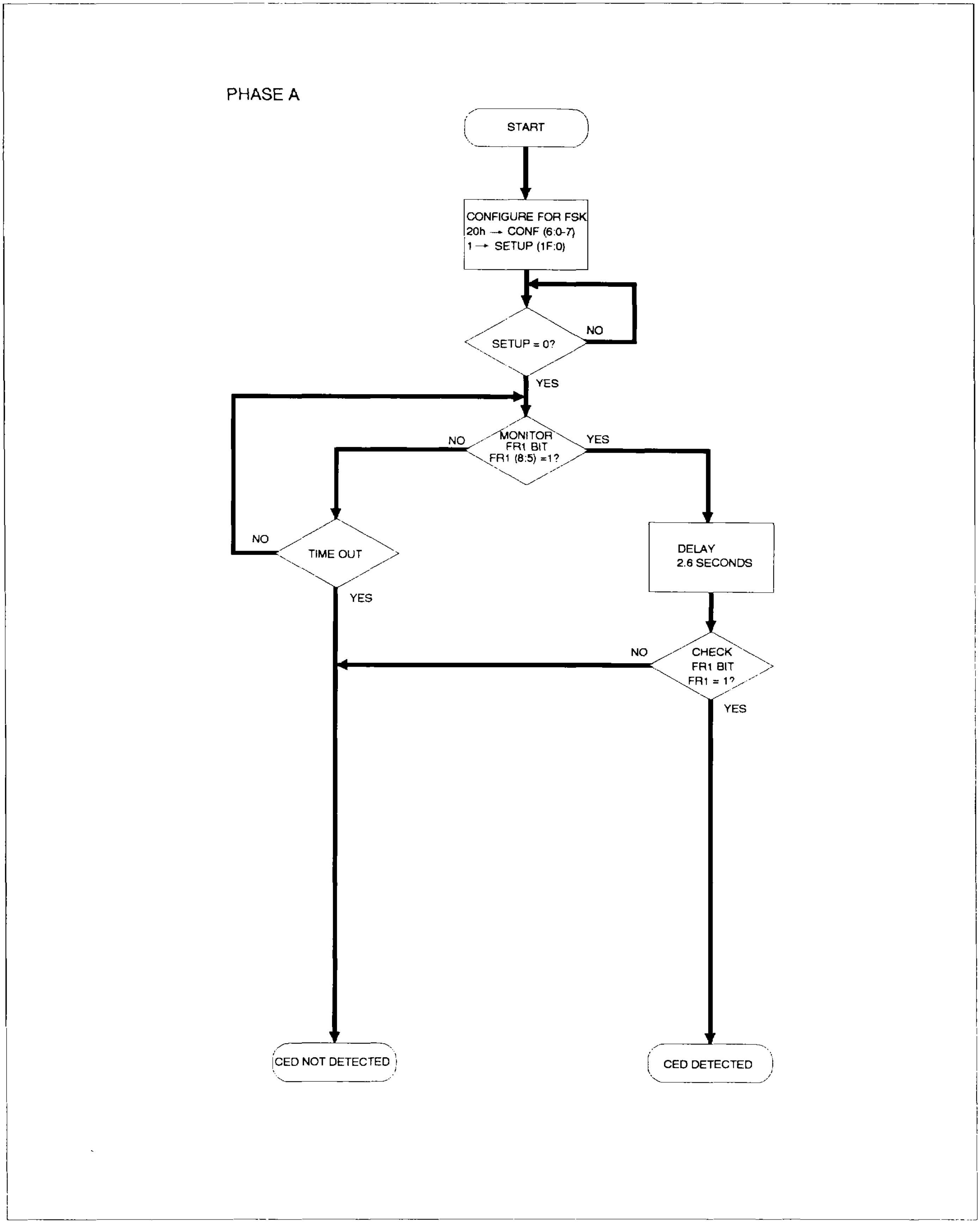


Figure 9-6. Detecting CED Tone (2100 Hz)

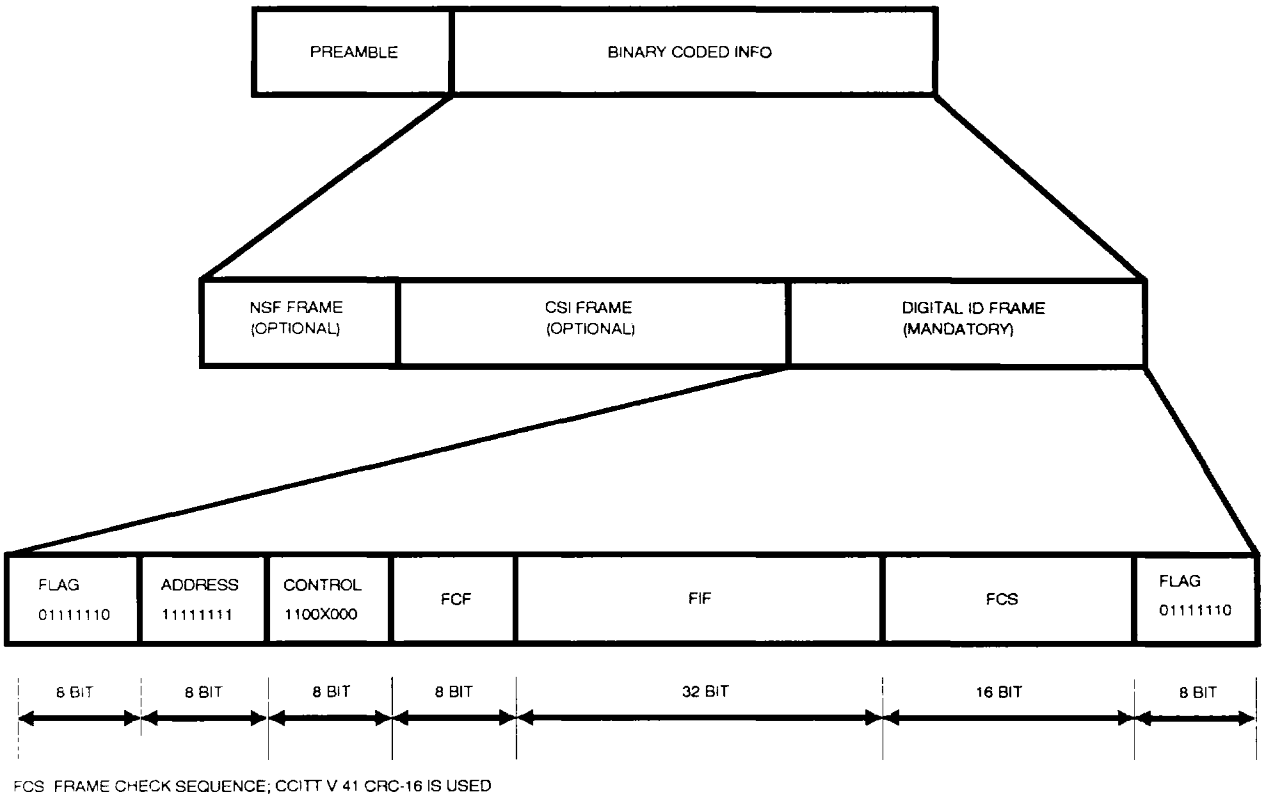


Figure 9-7. HDLC Frame Structure

sponds with a Digital Command Signal (DCS) which informs the called unit which options are chosen to complete this facsimile call.

After the DCS is transmitted, both the calling unit and the called unit set up for the high speed configuration that was chosen and transmitted via the DCS. A Training Check (TCF) is transmitted by the calling unit to verify training and give an indication of channel acceptability for the selected data rate. The TCF consists of a series of zeros for 1.5 seconds ±10%. Since the called unit knows it will be receiving 1.5 seconds of zeros, the host can make a decision whether the line is good enough at the chosen data rate or fallback to a slower speed.

After completing the TCF, the calling unit and the called unit re-configures for FSK, HDLC format. The called unit then transmits either a Confirmation to Receive (CFR) or a Failure To Train (FTT). The CFR is a response informing the calling unit of a successful pre-message procedure completion. A FTT informs the calling unit that the training signal was rejected and requests re-training. If a FTT is received by the calling unit, the fax protocol jumps back to the transition of DCS and continues until finally a CFR is received or the calling unit host decides to terminate the call.

The fallback criterion based upon the modem performance information during TCF reception, for example, may consist of monitoring the number of bit errors or EQM number (see Table 4-1 for RAM access codes and Section 4.2 for scaling information). Refer to the EQM and BER vs. S/N charts in Figure 13-1 for a guideline on EQM numbers. The EQM numbers shown in the charts are the decimal equivalent to the 16-bit hexadecimal numbers divided by 256.

During TCF, EQMs that represent acceptable BERs can be used to determine whether or not to fallback. If a fallback is necessary, EQM can be used to choose the appropriate fallback mode for a desired BER.

9.1.3 Phase C

Phase C occurs after both facsimile machines have set up for the high speed configuration that was decided upon in phase B. The T.30 Error Correction Mode is addressed in a following section. This high speed message information is usually compressed data using a Modified Huffman (MH) or Modified Read (MR) algorithm. The host processor must perform the MH or MR compression before loading the data into the modem. On the receive end, the host processor must perform the MH or MR decompression.

The start of phase C is denoted by an End Of Line (EOL) 8-bit code. The data follows this first EOL character until the end of the line. Another EOL character is transmitted to indicate a new line. A minimum transmission time of a total coded scan line is measured from the beginning of the EOL to the beginning of the following EOL. If the transmitted data requires less time than the minimum transmission time, fill bits must be transmitted. Six consecutive EOL characters constitute a Return To Control (RTC) command meaning end of document transmission. Figure 9-8 illustrates the phase C format.

9.1.4 Phase D

The post-message phase D procedure uses FSK and HDLC format. The calling station will typically send an End Of Message (EOM) signal. This FCF command (EOM) informs the called station that this is the end of the page and return to Phase B. A Multi-Page Signaling (MPS) or End Of Procedure (EOP) signal may be sent instead of EOM. The MPS signal informs the called unit that there are more pages in this facsimile transmission. EOP signals the end of the facsimile transmission. Procedure Interrupt-EOM (PRI-EOM), Procedure Interrupt-MPS (PRI-MPS), and Procedure Interrupt-EOP (PRI-EOP) indicate the same as EOM, MPS, and EOP, respectively, with the additional optional capability of requesting operator intervention. If operator intervention is required, further facsimile procedures commence at the beginning of phase B.

The called station might respond to an EOM, MPS, or EOP signal with a Message Confirmation (MCF) command. This FCF command indicates to the calling unit that the complete message was received. One of the following FCF commands may be sent instead of the MCF: Re-Train Positive (RTP), Re-Train Negative (RTN), Procedure Interrupt Positive (PIP), or Procedure Interrupt Negative (PIN). RTP indicates that a complete message has been received and that additional messages may follow after retransmission of TCF and CFR. RTN indicates that the previous message has not been satisfactorily received, however, further receptions may be possible provided there is a retransmission of TCF and CFR. PIP and PIN indicate that the previous message was received satisfactorily or not satisfactorily, respectively, and operator intervention is required for further transmissions.

9.1.5 Phase E

Call Release, or phase E, occurs after the last post-message signal of the procedure or under certain conditions such as a time-out, procedural interrupt, or a Disconnect (DCN) command.

The DCN command indicates the initiation of phase E. This command requires no response.

9.1.6 Flowcharts

Figures 9-9 through 9-15 illustrate how to implement certain phase B procedures. The examples show how the modem can be set up using the internal HDLC framing capabilities.

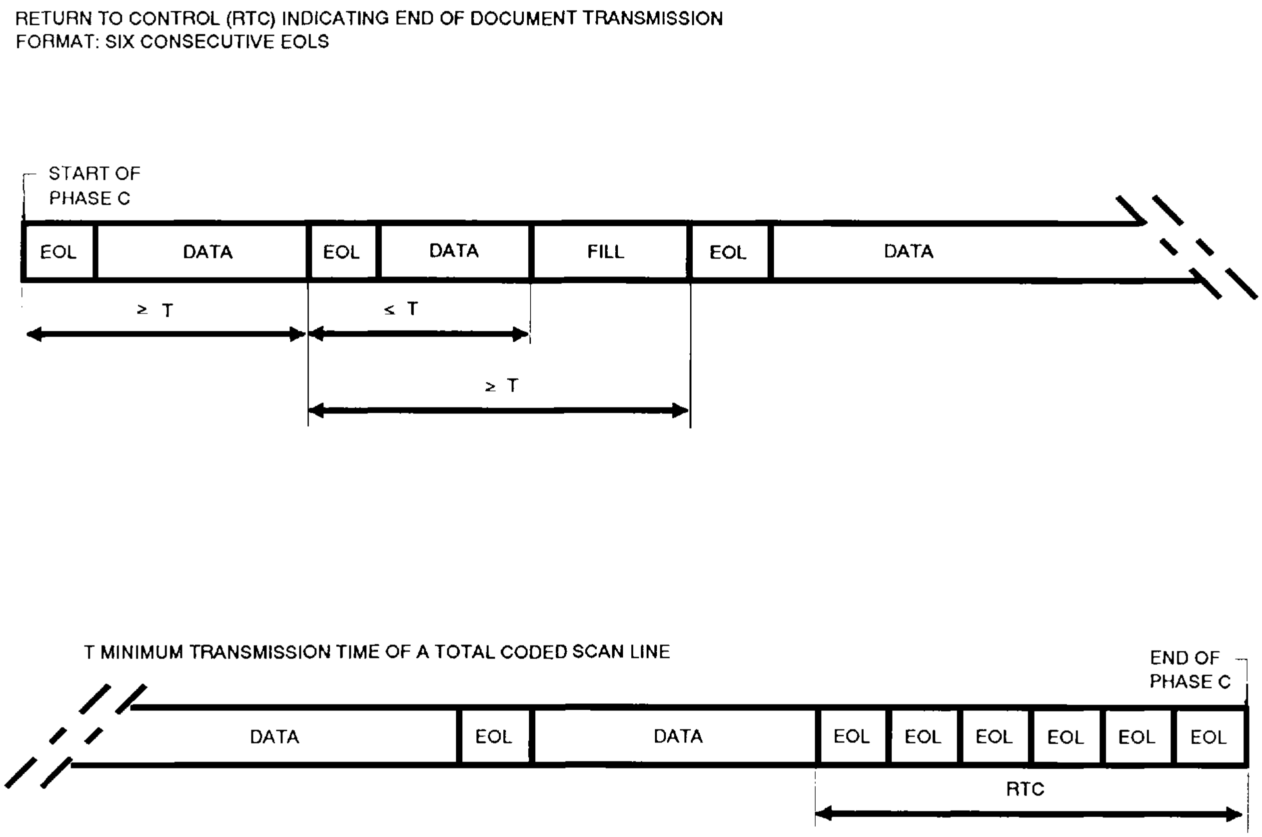


Figure 9-8. Phase C Format

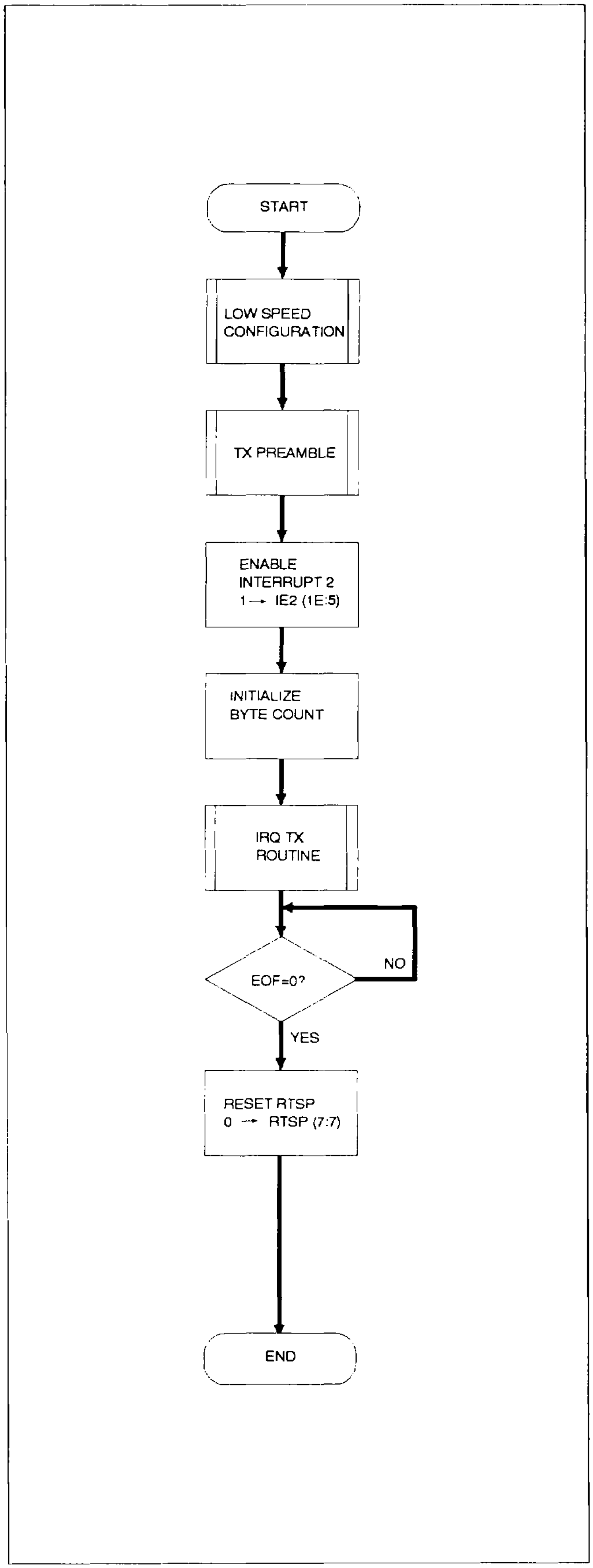


Figure 9-9. Transmit FSK/HDLC Signals

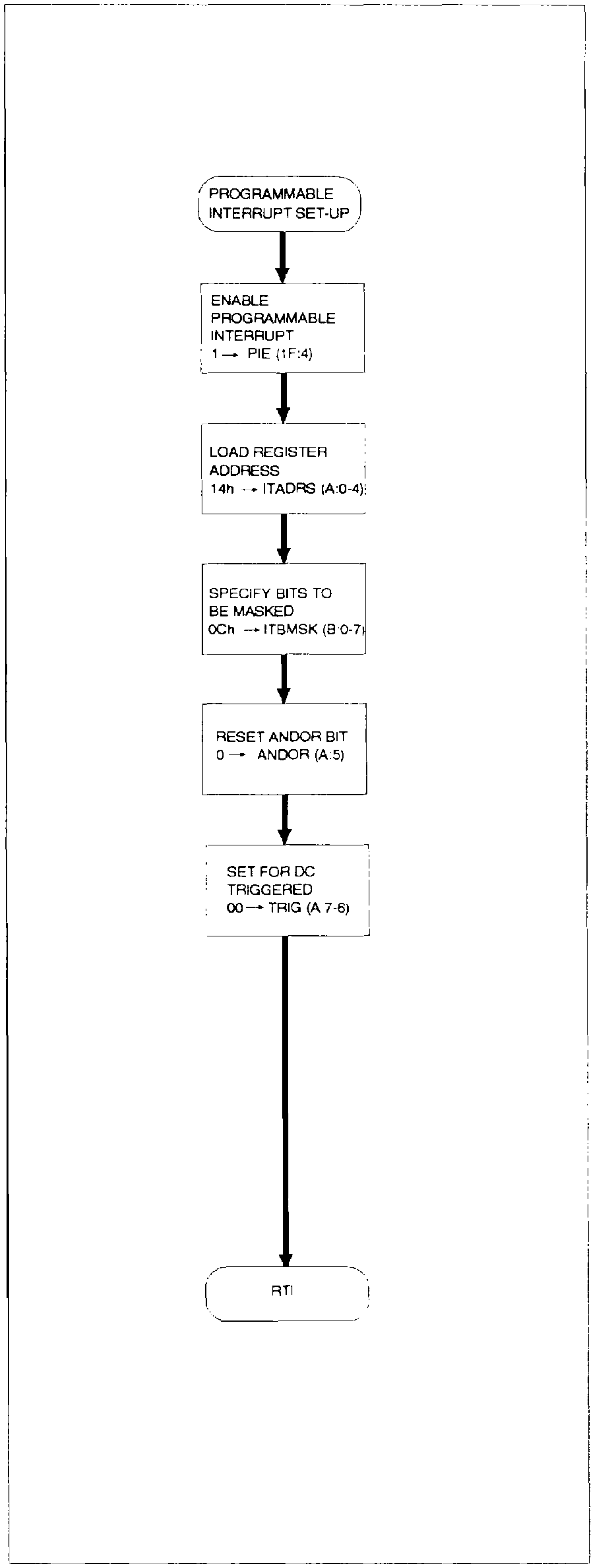


Figure 9-10. Programmable Interrupt Setup Subroutine

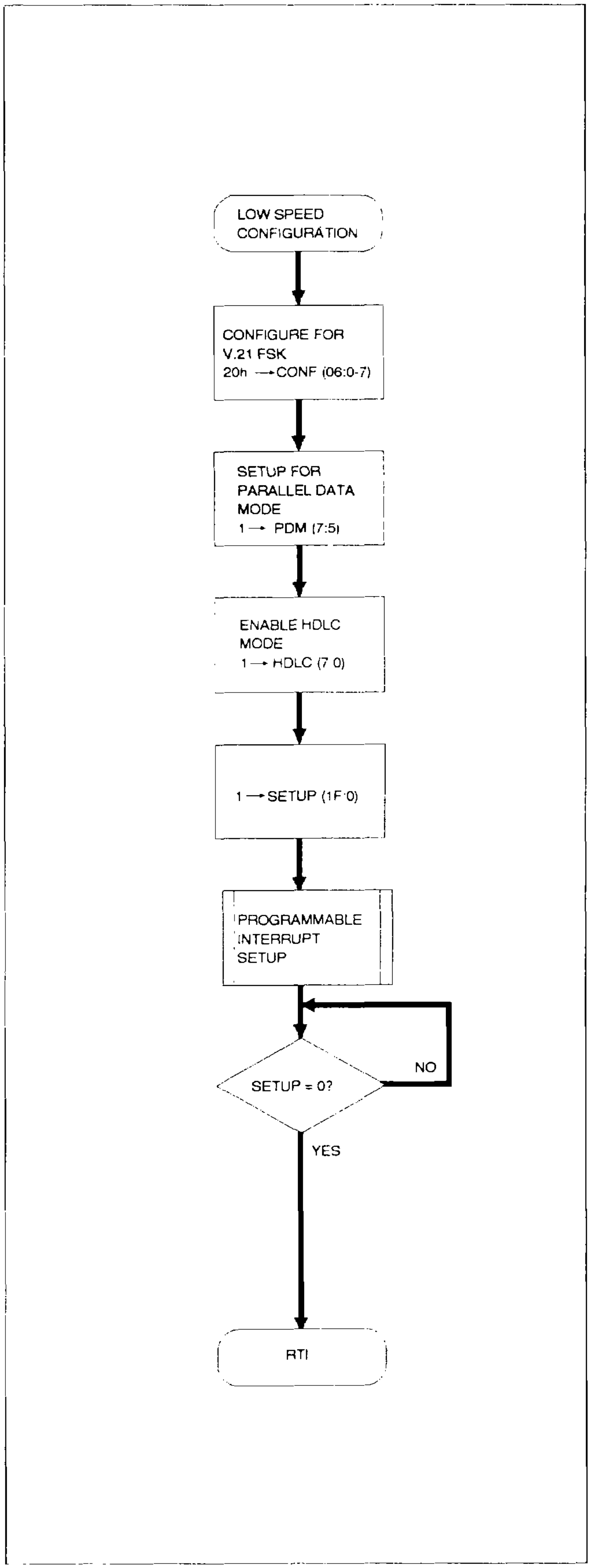


Figure 9-11. Low Speed Configuration Subroutine

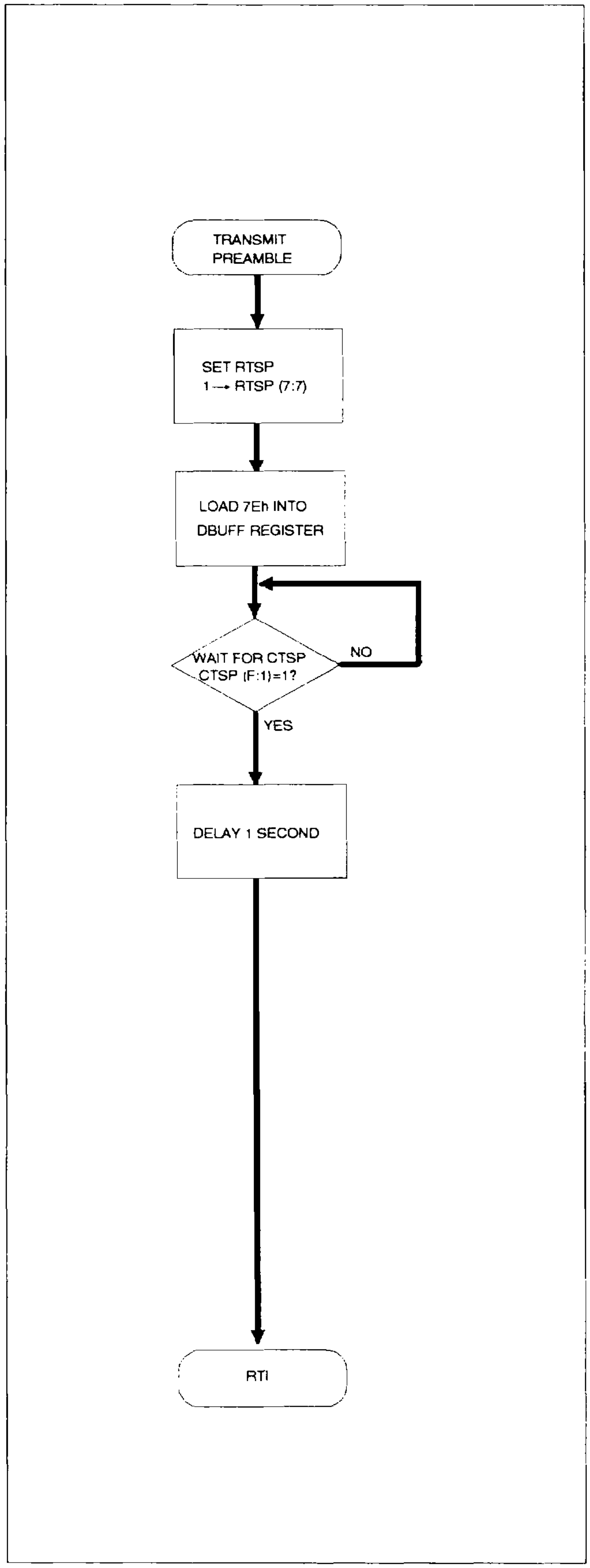


Figure 9-12. Transmit Preamble Subroutine

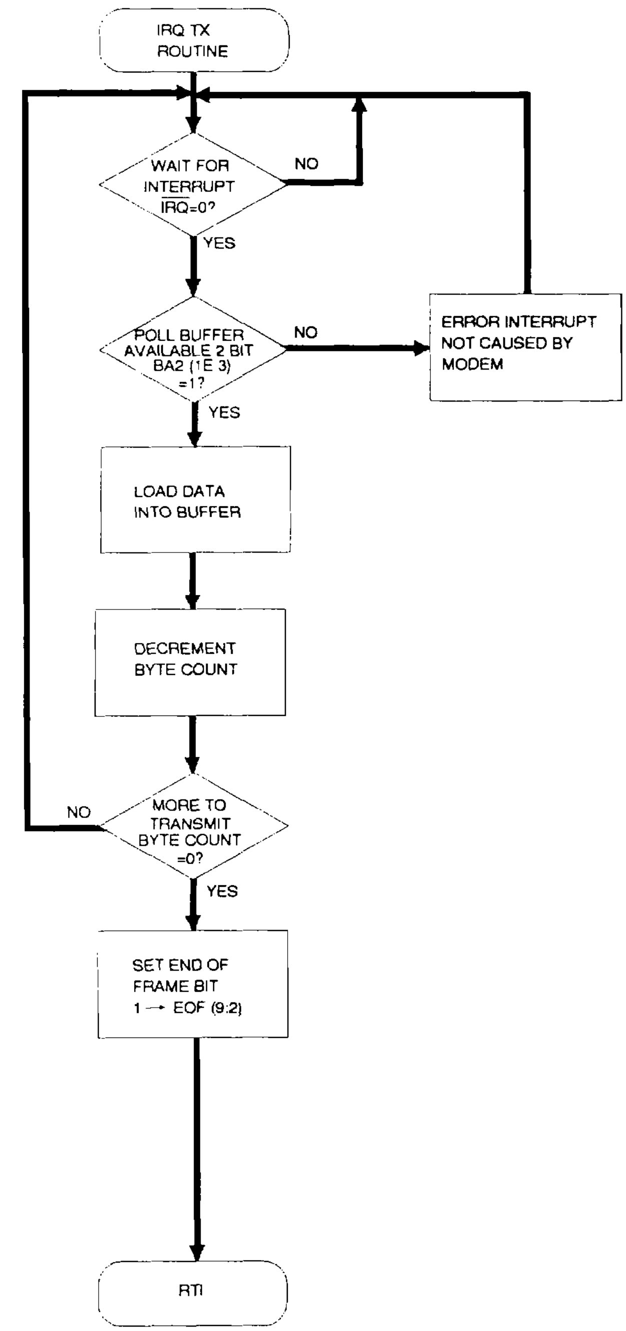


Figure 9-13. LS Interrupt-Driven Transmit Subroutine

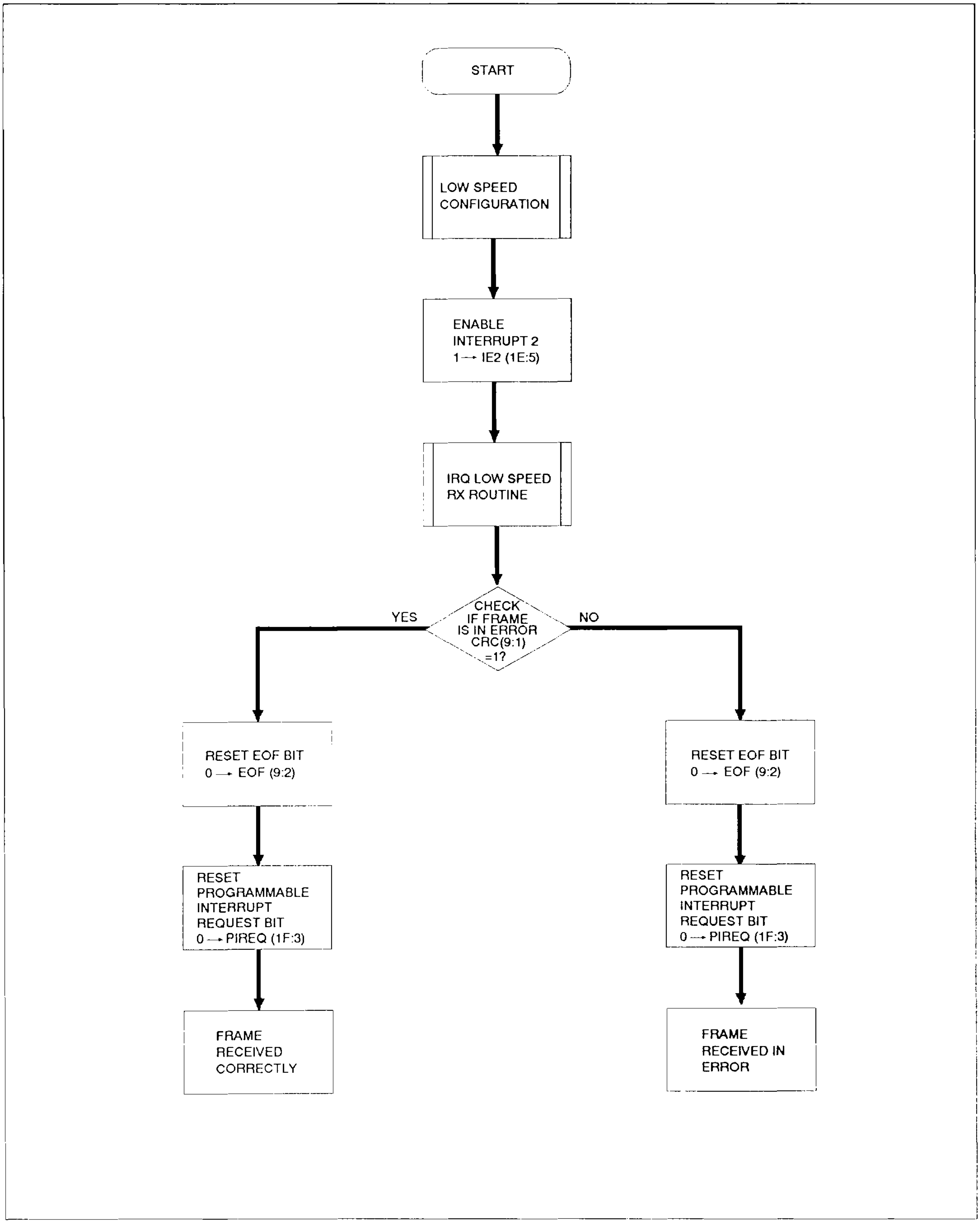


Figure 9-14. Receive FSK/HDLC Signals

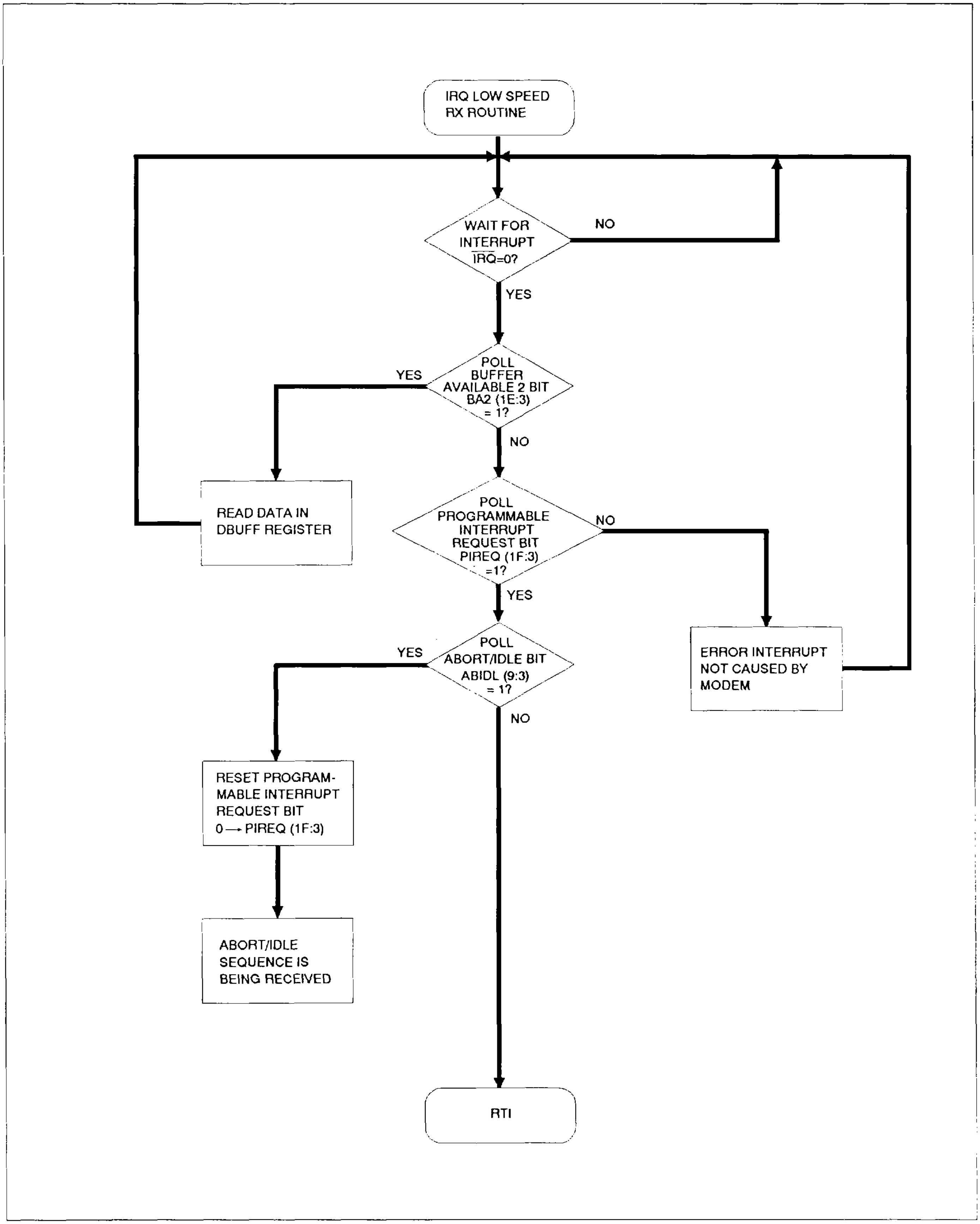


Figure 9-15. LS Interrupt-Driven Receive Subroutine

Figure 9-9 describes how to transmit FSK/HDLC signals such as DIS, DCS, DTC, CFR, FTT, etc. Three subroutines are called out: the low speed configuration, the transmit preamble, and interrupt-driven transmit routine. A Programmable Interrupt set-up is required in the receiver to determine if it is the end of the frame and if the frame was received correctly. Figure 9-10 describes how to set this up. The Low Speed Configuration subroutine is shown on Figure 9-11. Since the HDLC function is being used, the parallel data mode is enabled. The Transmit Preamble routine is shown on Figure 9-12. When the modem is configured in HDLC mode by setting RTSP, the modem will automatically transmit flags. The Interrupt-Driven Transmit routine is illustrated in Figure 9-13. The hardware IRQ pin must be monitored for interrupts. The IRQ pin will become active (go low) when the modem is ready for a byte of data. This data should be loaded into the Data Buffer Register, DBUFF. When the IRQ returns low, the modem is ready for the next byte of data.

Figure 9-14 describes how to receive FSK/HDLC signals. The Interrupt-Driven Low Speed Receive routine is shown on Figure 9-15. After IRQ is low, the Buffer Available 2 (BA2) bit is polled to determine if the next byte must be read by the host. If BA2 is a 0, the Programmable Interrupt Request (PIREQ) bit is polled to determine if one of the programmable interrupt bits caused the interrupt. If Abort/Idle (ABIDL) is a 1, then an abort or idle sequence is being received. If ABIDL is a 0, then a Return from Subroutine is executed and the End of Frame bit is checked to see if it is the end of the frame. The Cyclic Redundancy Check (CRC) bit is looked at to determine if the current frame was received correctly.

Figure 9-16 shows how to re-configure the modem to a high speed configuration. This procedure will be used again when entering phase C. Figure 9-17 describes how to transmit the TCF or one second of zeros.

Figure 9-18 describes the High Speed Message Transmission. This procedure is similar to the Low Speed Message Transmission. The High Speed Configuration is located at Figure 9-16. The High Speed Interrupt-Driven Transmit routine is in Figure 9-19. This is also similar to the low speed procedure.

The High Speed Message Reception procedure is illustrated in Figure 9-20. The High Speed Interrupt-Driven Receive subroutine is in Figure 9-21. Included in the High Speed Message Reception procedure is an optional Ensure Valid Train subroutine (Figure 9-22). This procedure is recommended to ensure that a valid training sequence is accomplished when noise is above the RLSD turn-on threshold.

9.2 T.30 ERROR CORRECTION MODE

9.2.1 General

The revised T.30 contains an Error Correction Mode (ECM) option. The ECM allows the phase C portion of the facsimile transmission to be encoded in a HDLC framing format using a specified number of bits in the information field. The transmitted high speed message is broken up into a number of frames identified by frame numbers. If an error is detected during reception of the message, the called station records the frame number. After all the frames in the message has been received, the called station transmits the frame numbers that were received in error. The calling station then re-transmits only those frames in error. This continues until the entire message is received error free or the calling station decides not to transmit any more frames.

The error detection is performed by comparing the CRC or FCS. Using ECM, the data rate can be as fast as 9600 bps, therefore, the host microprocessor cannot keep up implementing HDLC without the use of a serial I/O device. The modem provides HDLC features at speeds up to 9600 bps.

9.2.2 ECM Frame Structure

In Error Correction Mode, one frame of facsimile data consists of 256 or 64 octets of data. Each page may contain 1 to 256 frames. Also, 1 to 256 pages may be transmitted. The ECM frame structure is illustrated in Figure 9-23. Following the high speed training sequence, the flag, address field, and control field is transmitted. In ECM, Flag=7E, Address=FF, and Control=B0. The Facsimile Control Field for the Facsimile Coded Data block (FCD) is 60. The frame number follows the FCF for FCD, followed by the facsimile data. Pad bits such as EOL, Tag, and Align bits follow the facsimile data. Finally, the FCS check and the ending flag is transmitted.

After 256 frames, a Return Control for Partial page (RCP) block is transmitted three times. The RCP block consists of the same Flag, Address Field, and Control field followed by the FCF for RCP. The FCS immediately follows with the ending flag. After the third RCP, a maximum of 50 ms of flags are transmitted.

An ECM message protocol example is shown in Figure 9-24. The bold arrows are high speed transmissions and the other arrows are FSK transmissions. The example is self-explanatory. If more information is needed, refer to the T.30 ECM specification.

In this paragraph the Q refers to the NULL, EOP, MPS, or EOM Facsimile Control Field commands. The Partial Page Signals (PPS-Q) and Partial Page Request (PPR) frame structures are shown in Figure 9-25. The PPS-Q frame begins with the same Flag, Address field, and Control field. Two FCF commands follow. The first FCF transmitted is to indicate PPS. The second FCF is either NULL, EOP, MPS, or EOM. The page count followed by the block count, followed by the total number of frames in the block are

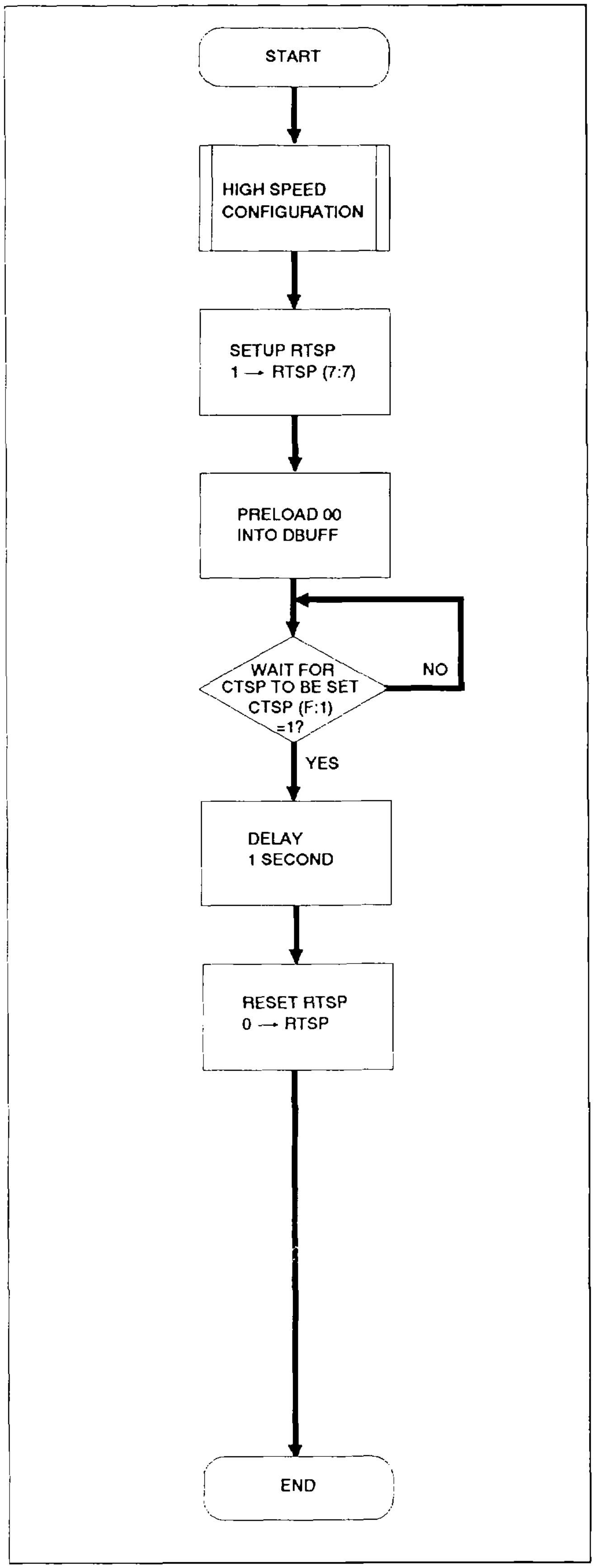


Figure 9-16. Transmitting TCF

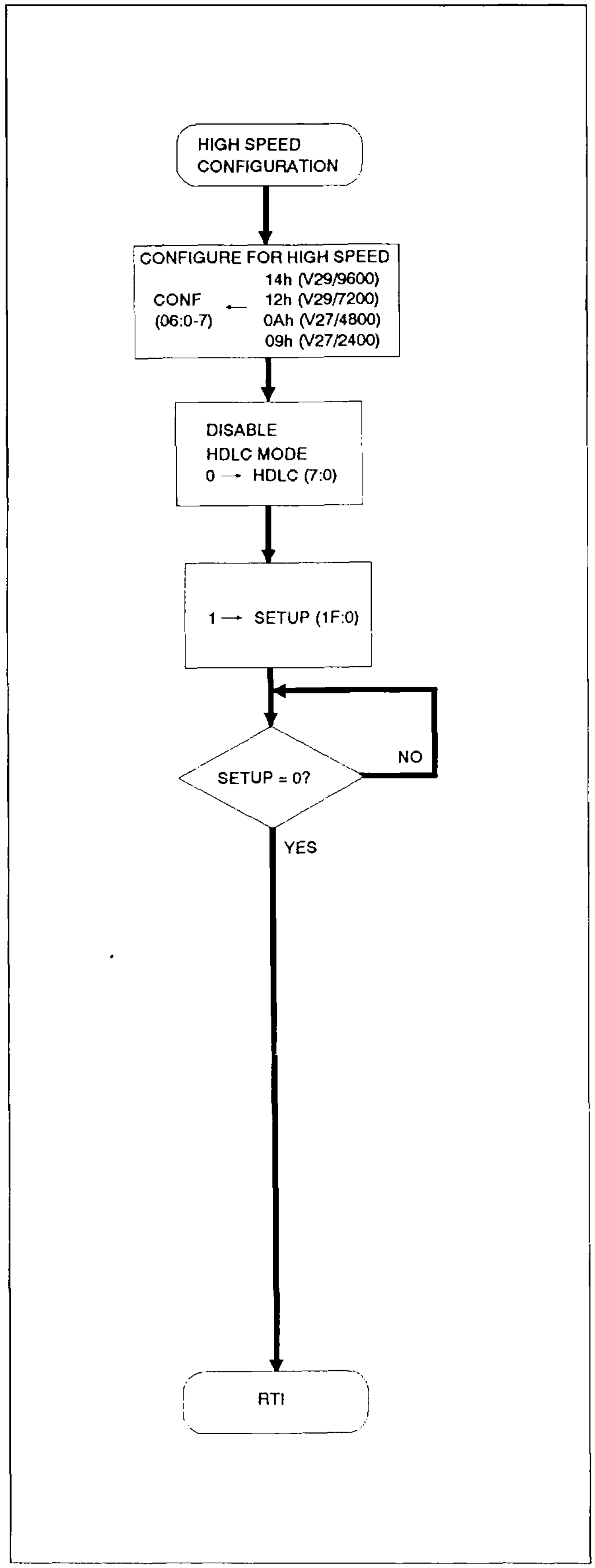


Figure 9-17. HS Configuration Setup Subroutine

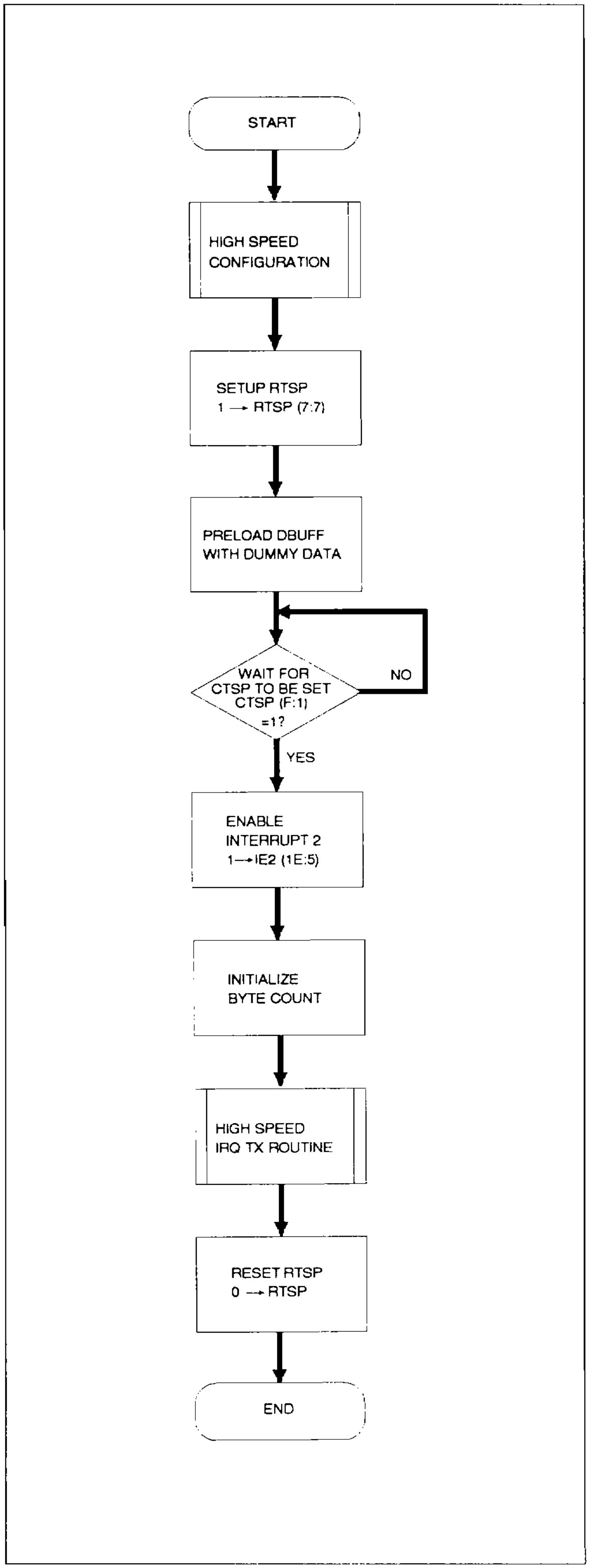


Figure 9-18. High Speed Message Transmission

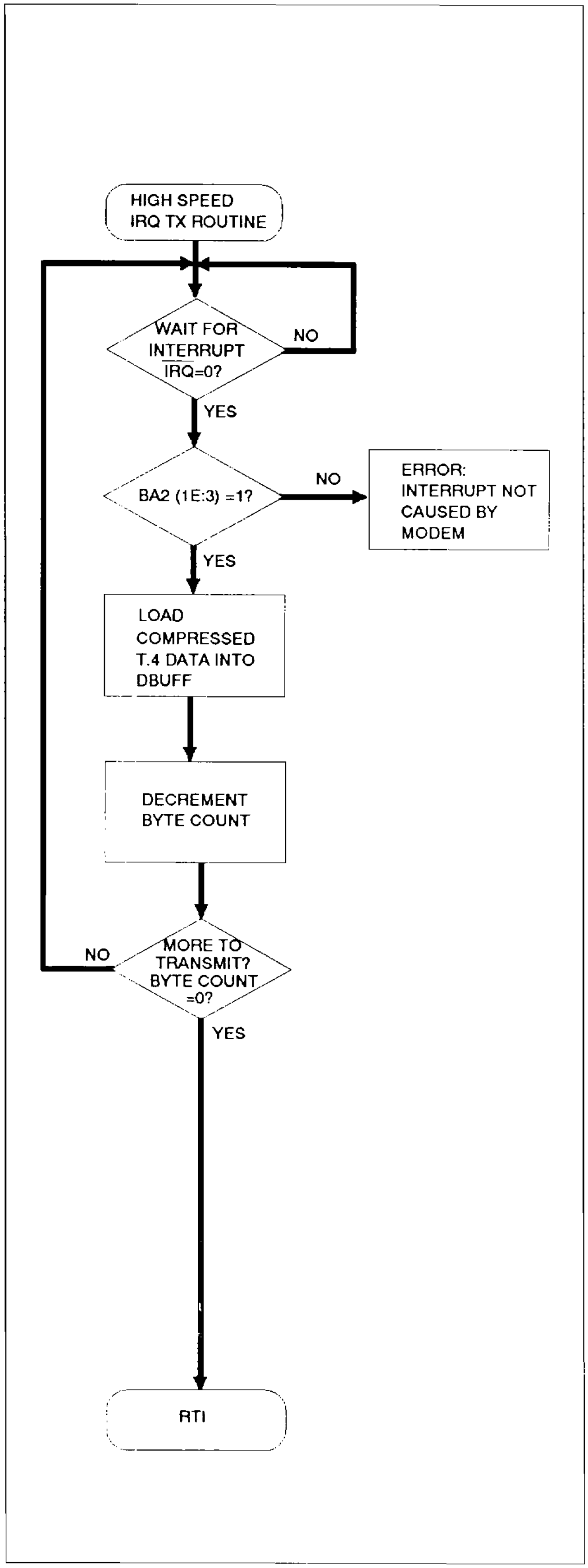


Figure 9-19. HS Interrupt-Driven Transmit Subroutine

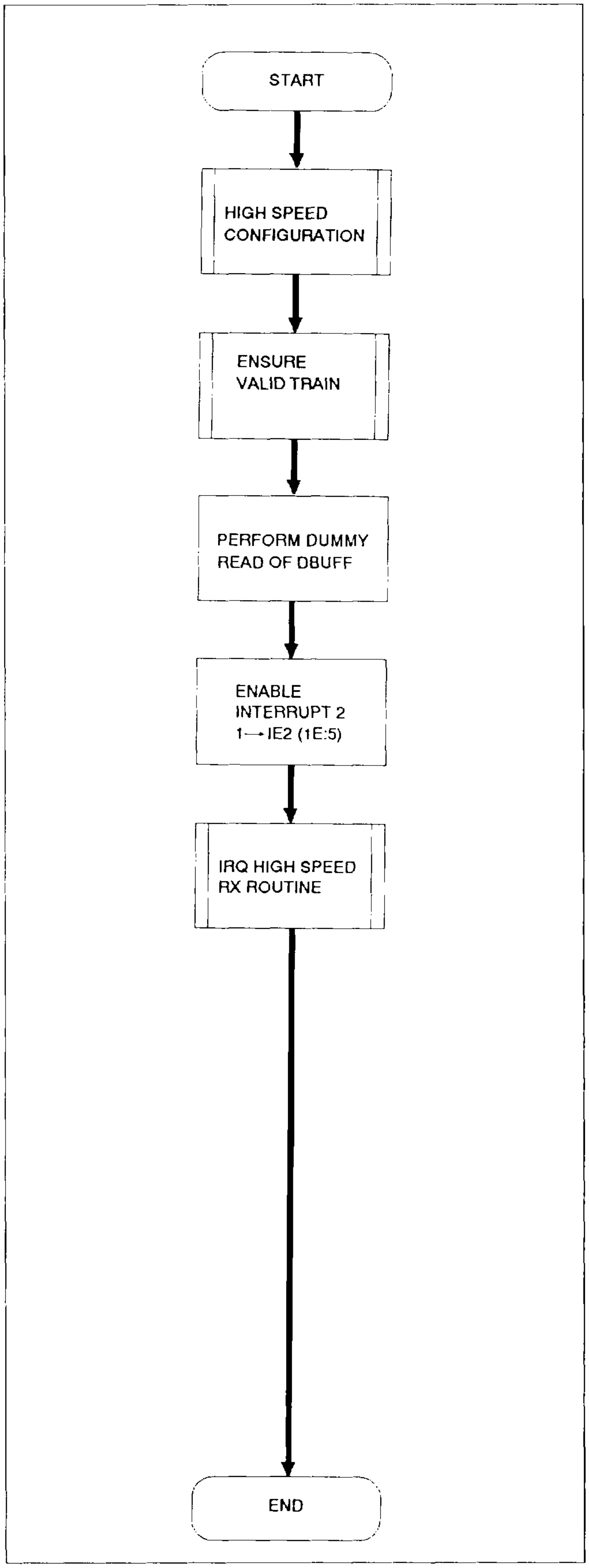


Figure 9-20. High Speed Reception Setup

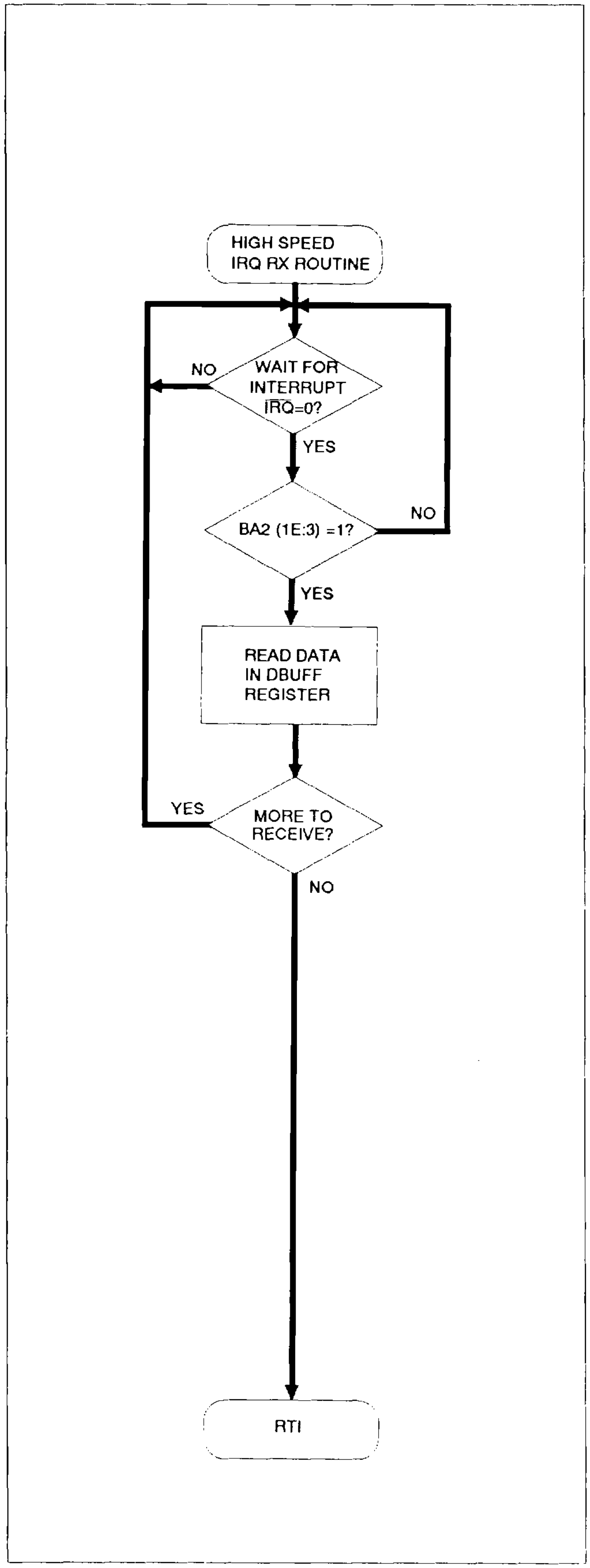


Figure 9-21. HS Interrupt-Driven Receive Subroutine

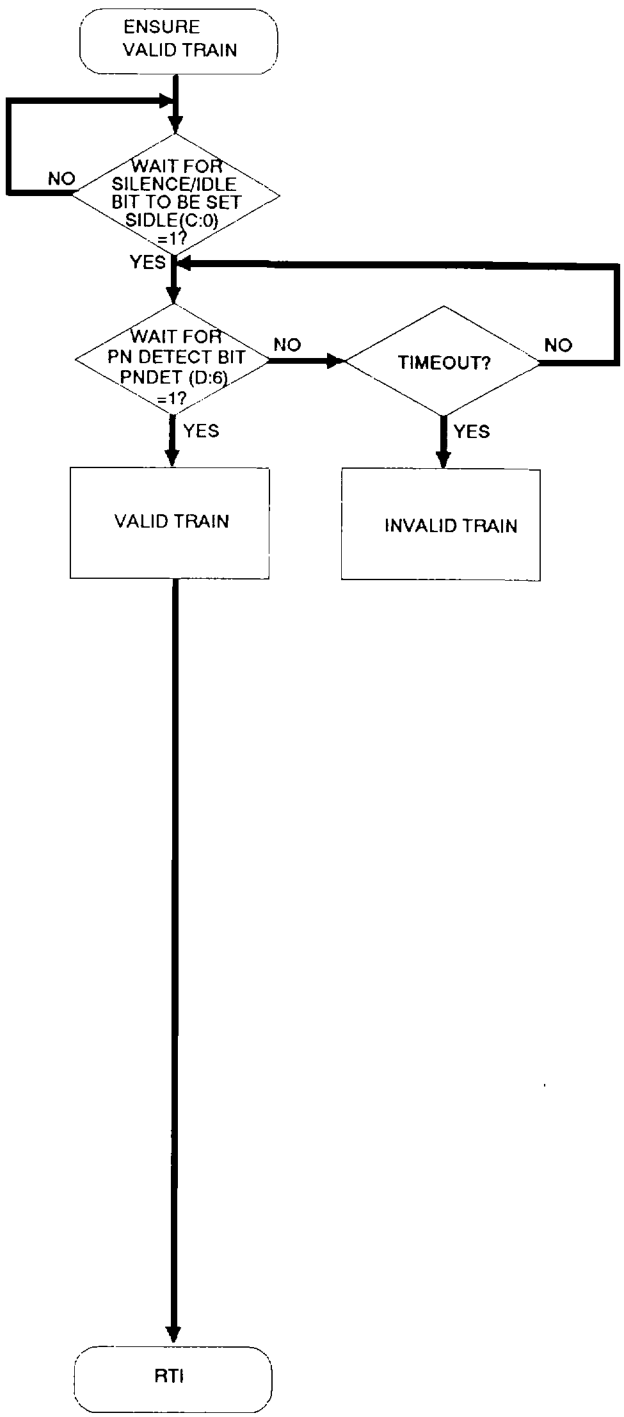


Figure 9-22. Valid Training Sequence Check Subroutine

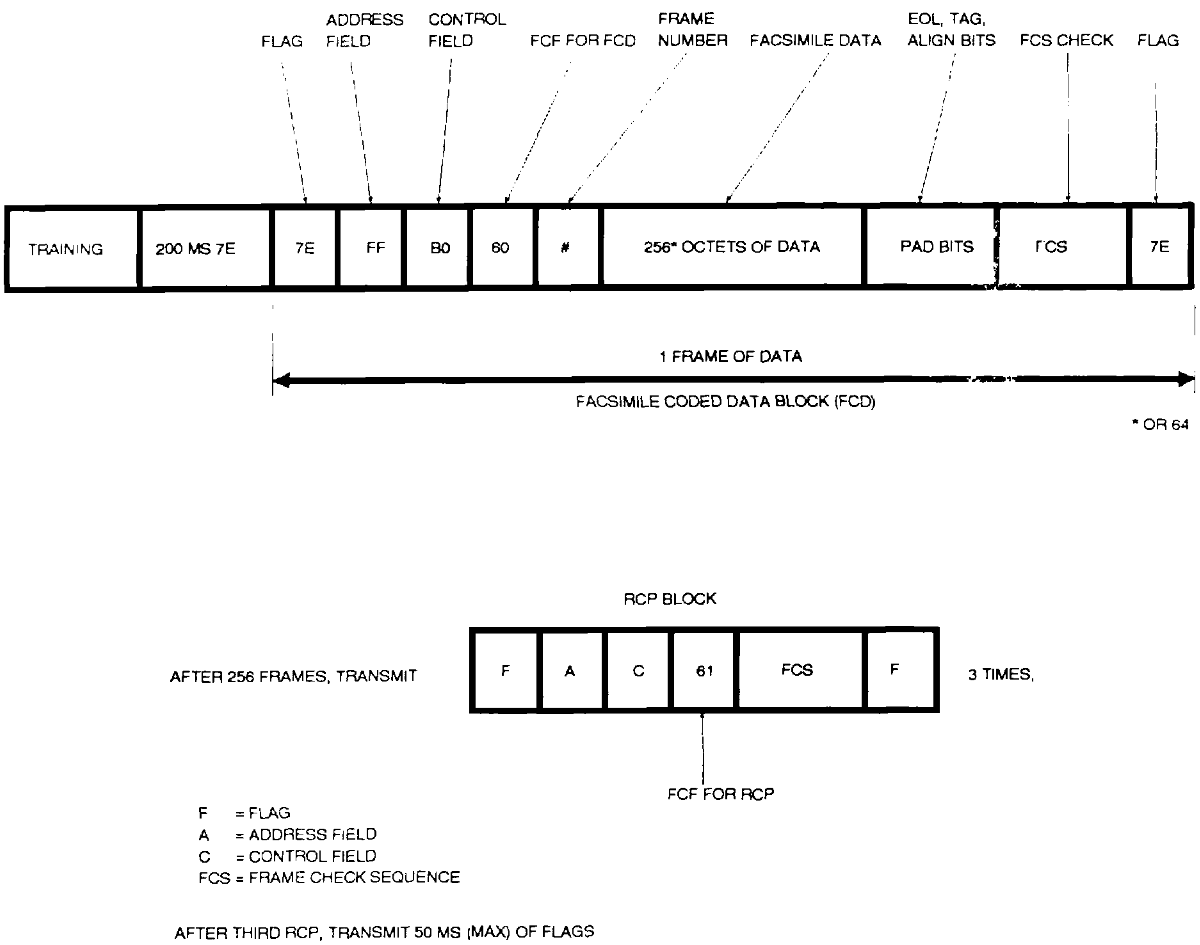


Figure 9-23. ECM Frame Structure

→ MESSAGE, PAGE 0, BLOCK 0
→ PPS-NULL (TO INDICATE MORE BLOCKS FOR THIS PAGE WILL BE TRANSMITTED)
← PPR (TO IDENTIFY FRAMES RECEIVED WITH ERRORS)
→ RETRANSMIT MESSAGE FRAMES IN ERROR, PAGE 0, BLOCK 0
→ PPS-NULL
← MCF (TO INDICATE NO ERRORS, AND READY TO RECEIVE)
→ MESSAGE, PAGE 0, BLOCK 1
→ PPS-MPS (TO INDICATE END OF CURRENT PAGE, MORE PAGES TO TRANSMIT)
← PPR (TO IDENTIFY FRAMES IN ERROR)
→ RETRANSMIT MESSAGE FRAMES IN ERROR, PAGE 0, BLOCK 1
→ PPS-MPS
← RNR (INDICATES RECEIVER NOT READY)
→ RR (REQUEST RECEIVER STATUS)
← RNR (RX STILL NOT READY)
→ RR
← MCF (INDICATES NO ERRORS IN LAST MESSAGE, RX READY)
→ MESSAGE, PAGE 1, BLOCK 0
→ PPS-EOP (INDICATES END OF PROCEDURE, I.E. NO MORE PAGES TO TRANSMIT)
← PPR (INDICATES FRAME ERRORS)

•
•
•

→ RETRANSMIT MESSAGE FRAMES IN ERROR, PAGE 1, BLOCK 0
→ PPS-EOP
← PPR, 4TH REQUEST FOR RETRANSMISSION OF FRAMES IN ERROR FOR PAGE 1, BLOCK 0

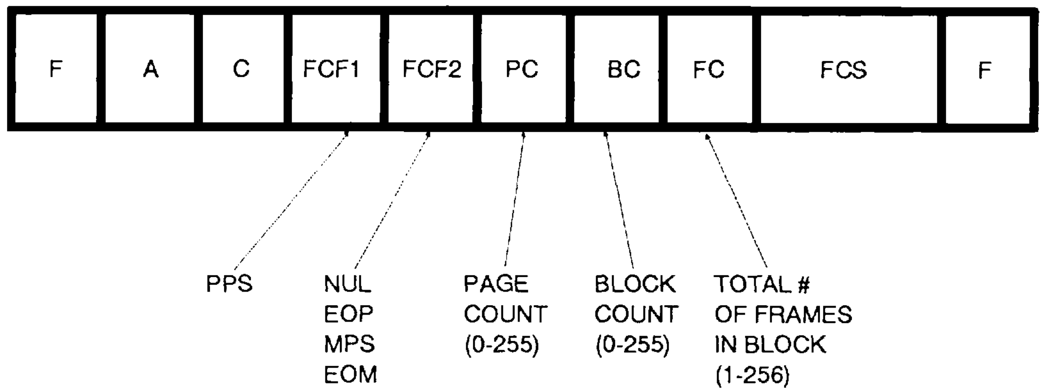
AFTER 4TH REQUEST FOR RETRANSMISSION OF ERRORED FRAMES ON THE SAME BLOCK, THE TRANSMITTER MAY RESPOND WITH:

→ EOR-EOP (INDICATES END OF RETRANSMISSION (I.E. TX WILL NOT CORRECT ANY MORE ERRORS FOR PAGE 1, BLOCK 0
← ERR (RX RESPONSE TO EOR-EOP)
→ DCN (TX DISCONNECTS)

********* OR ************

→ CTC-EOP (INDICATES TX WILL CONTINUE TO CORRECT PAGE 1, BLOCK 0 ERRORS)
← CTR (RESPONSE TO CTC-EOP)
→ RETRANSMIT MESSAGE FRAMES IN ERROR, PAGE 1, BLOCK 0
→ PPS-EOP
← MCF (INDICATES RETRANMISSION RECEIVED WITHOUT ERRORS)
→ DCN (DISCONNECT)

Figure 9-24. ECM Message Protocol Example



FSK 300 BPS

F = FLAG
A = ADDRESS FIELD
C = CONTROL FIELD
FCS = FRAME CHECK SEQUENCE

PPR FRAME STRUCTURE

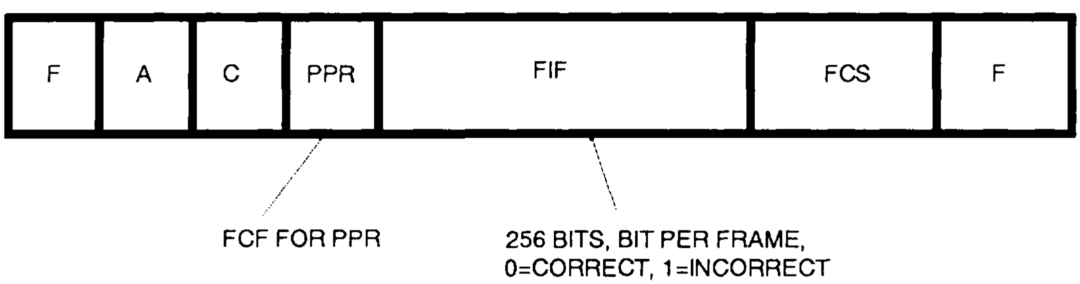


Figure 9-25. PPS and PPR Frame Structure

transmitted next. The FCS and ending flag are finally transmitted.

The PPR frame structure also begins with the same Flag, Address, and Control field. The FCF for PPR is the next octet. The FIF consists of 256 or 64 bits depending on how many frames were transmitted. The contents of FIF is either a 0 or a 1. The bit number corresponds to the frame number and a 0 indicates the frames was received correctly and a 1 indicates an incorrect frame was received.

9.3 SIGNAL RECOGNITION ALGORITHM

A method of determining whether a high speed message or FSK handshaking is being received by the modem is necessary when implementing the T.30 recommendation. When the calling unit transmitter and called unit receiver configure for V.29 or V.27 ter, sometimes the high speed message may not be received (typically due to a noisy line). In this case, the calling unit transmitter will try to send the message up to three times before re-negotiating in FSK signalling. The called unit receiver must, therefore, be able to distinguish between a high speed message and FSK handshaking.

Two algorithms are provided to perform this signal recognition. The first one can be used with all the 9600 bps MONOFAX modems. A flowchart for this method is shown in Figure 9-26.

A simpler alternative signal recognition algorithm can be used with the later 9600 bps MONOFAX modems (R96MFX: R6628-13 and above; R96EFX: R6631-13 and above; R96DFX: R6633-12 and above; and all R96VFX). A flowchart for this alternative algorithm is shown in Figure 9-27. This algorithm uses the PNSUC bit (08:3) which is not available in the DSP interface memory of the earlier modems.

The tone detector coefficients to detect 1650 Hz in either of these algorithms are listed in Table 9-1.

In the R96VFX, a simple signal recognition algorithm which uses the FSK7E bit is shown in Figure 9-28.

Table 9-1. FR3 Coefficients for 1650 Hz Detection

Coefficient Name	RAM Access Code (Hex)*	Coefficient Value (Hex)
α_0	31	05F5
α_1	32	FAC3
α_2	33	05E3
α'_0	34	01F3
α'_1	35	0000
α'_2	36	0000
β_1	B2	3EAE
β_2	B3	C0C3
β'_1	B5	3D05
β'_2	B6	C093
α''	B4	0088
β''	B1	7FBC

* BRx = 0, CRx = 1, and IOx = 0.

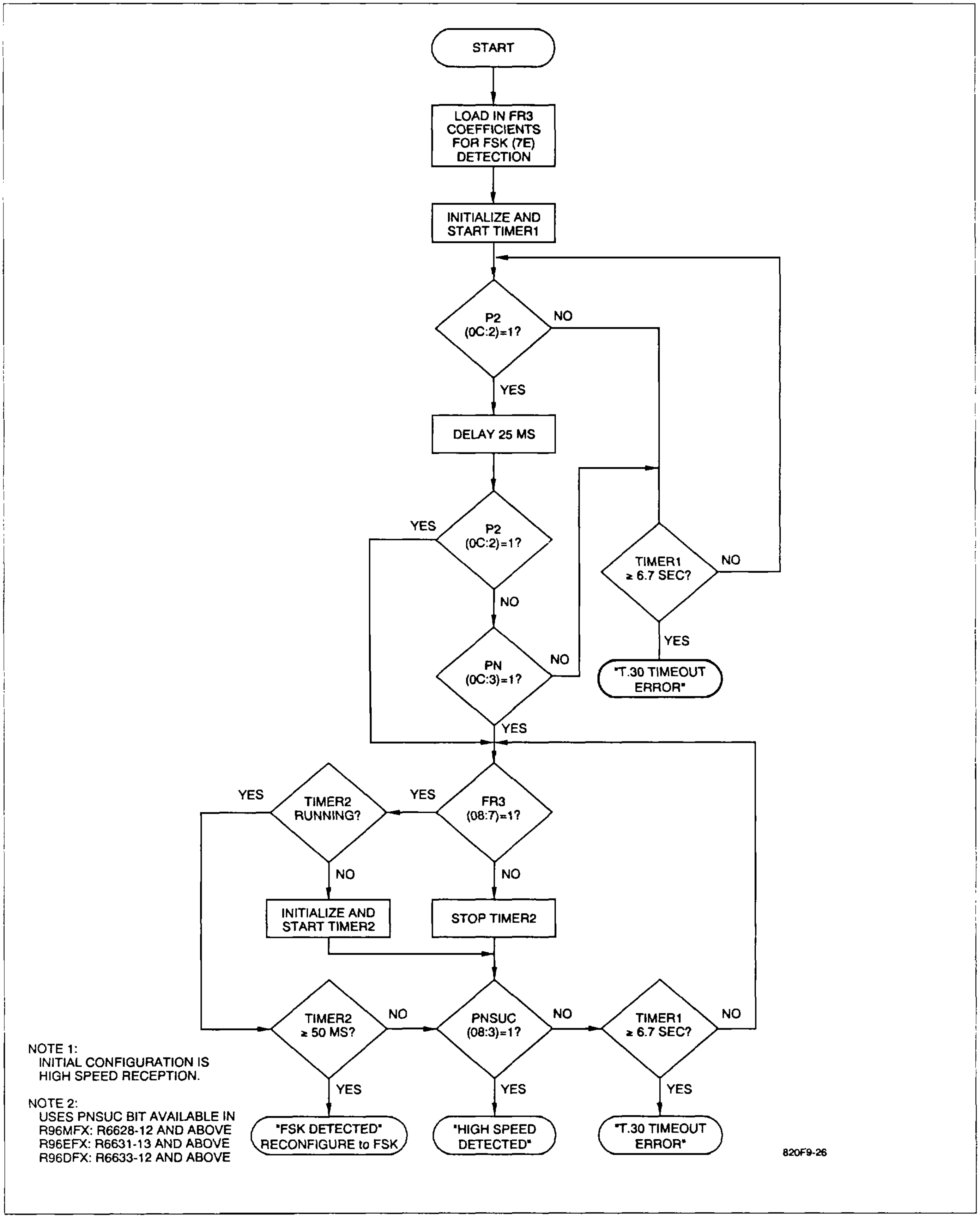


Figure 9-26. Signal Recognition Algorithm

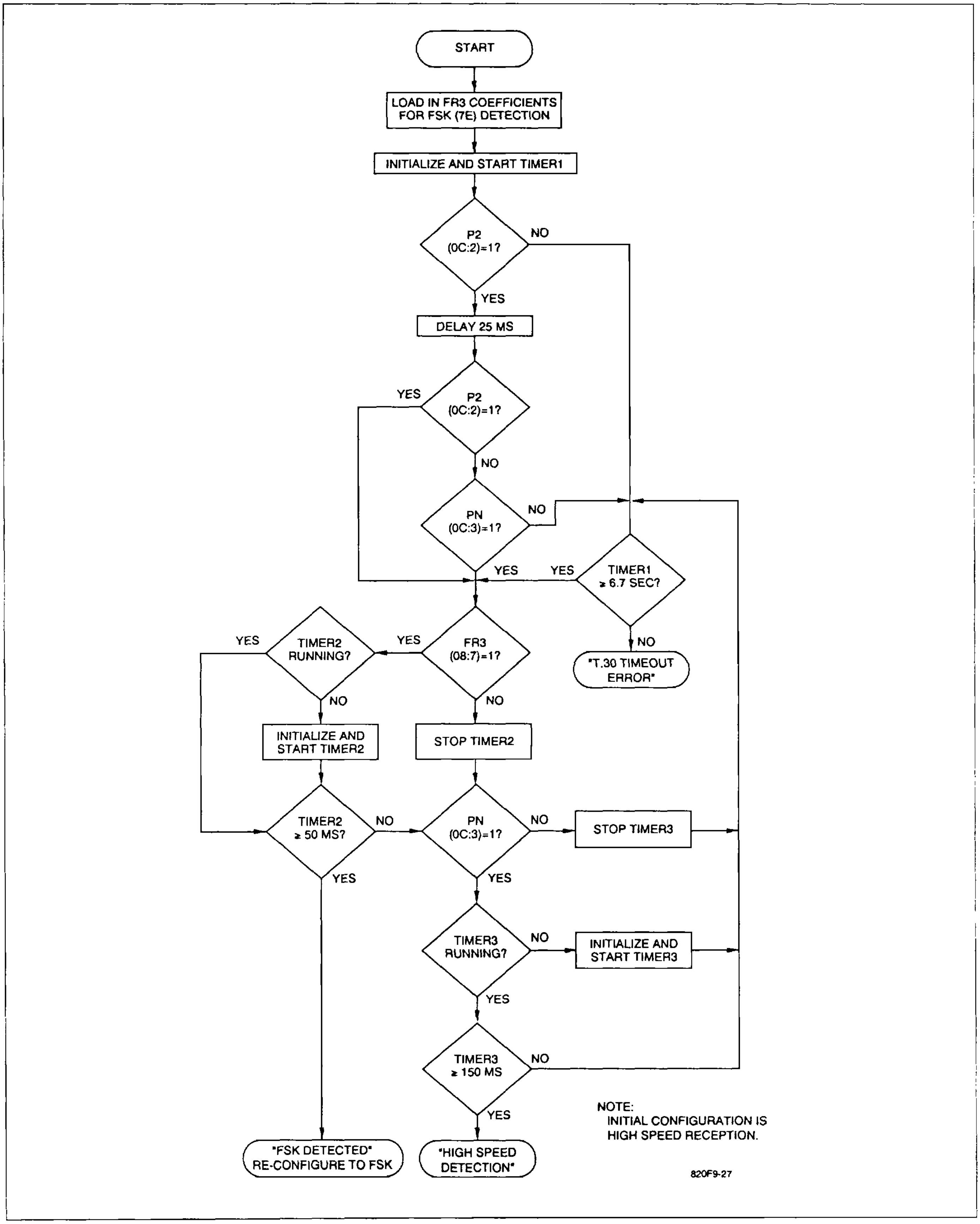


Figure 9-27. Alternative FSK/High Speed Detection Algorithm

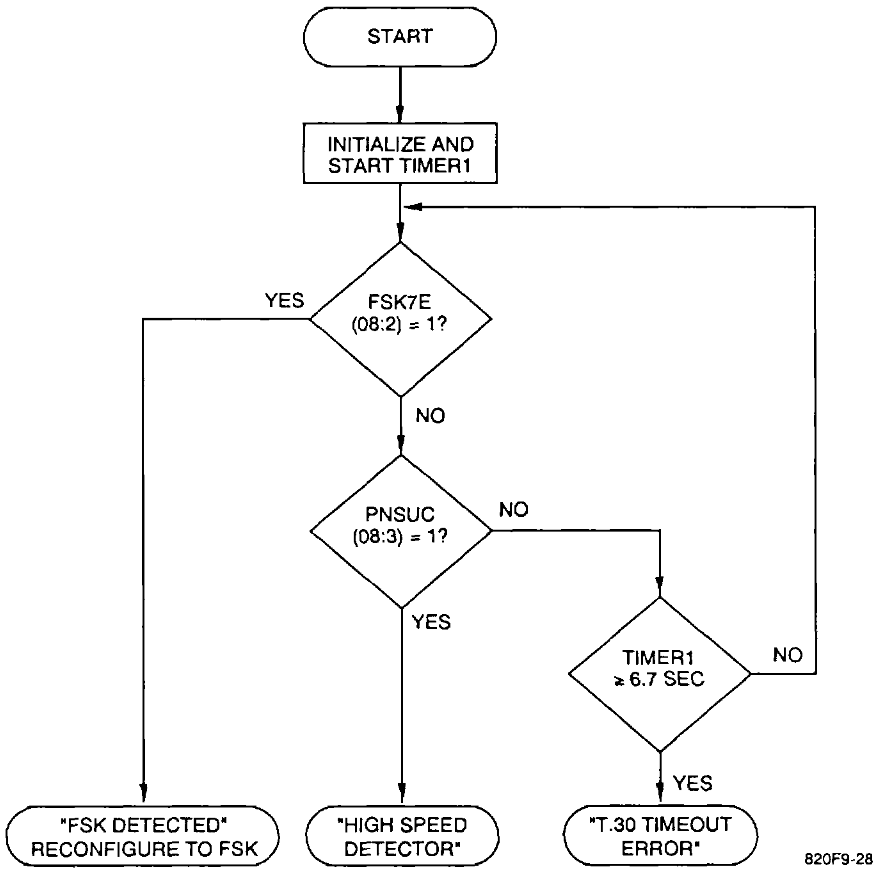


Figure 9-28. FSK Signal Recognition Algorithm using FSK7E

10 ADPCM CODEC

The host selects two, three, or four bits per sample enhanced ADPCM speech compression and decompression by configuring the modem to the appropriate configuration (CONF bits = 9xh) and enabling the coder (bit CDEN) and/or decoder (bit DCDEN). The host enables decoder silence interpolation (bit SDCDE) only if coder silence detection/deletion (bit SCDE) was previously enabled during coding. The default programmable sample rate is 8k Hz. RAM Access 2 must be disabled when either the coder or decoder is enabled. The programmable interrupt operates continuously at the sample rate.

The codec input, codec output, and modem state are dependent upon RTS/RTSP and control bits DCDEN and CDEN as shown in Table 10-1. RAM Access 1 in Table 10-1 refers to RAM Access 1 option for host provided 16-bit speech sample coder input, and refers to RAM Access 1 option for receiving decoder 9-bit serial and 16-bit parallel output (see Sections 10.3.1 and 10.3.2). An x denotes L for least significant byte or M for most significant byte.

10.1 ADPCM CODEC RECEIVER

As shown in Figure 10-1, the modem's integrated analog device filters, amplifies, and samples the analog signal. The filtering includes sin(x)/x attenuation correction. The ADC speech samples are scaled (see Section 10.3.4) and sent to the coder. Alternatively, the host may provide the ADC speech samples (see Section 10.3.1). If enabled, silence detection/deletion provides additional compression (see Section 10.3.5). With 2, 3, or 4 bits per sample compression at the 8k Hz default programmable sample rate, the 16-bit coder output words are provided at 16k, 24k, or 32k bps (1k, 1.5k, or 2k 16-bit words per second), respectively.

The host supplies the decoder with the 16-bit coded words. The speech samples are reconstructed and white noise is inserted if silence interpolation is enabled (see Section 10.3.5). The programmable white noise level may be set to zero for absolute silence insertion. Each reconstructed speech sample is scaled (see Section 10.3.4) then written to RAM for host access (see Section 10.3.2).

The host may enable the three tone detectors/12th order filter (bits TDTEN and 12TH), DTMF receiver (bit DTMFE), and FSK Flag Pattern detector (bit FSKFLS) to operate concurrently with the ADPCM codec receiver to facilitate signaling and FAX recognition. The DTMF receiver and FSK flag pattern detector have been preprogrammed for 9.6k, 8k, 7k, or 6k Hz sample rates. The tone detector filter coefficients must be reprogrammed from their default 9.6k Hz sample rate to match the ADPCM default (8k Hz) or selected sample rate. The host selects a 9.6k, 8k, 7k, or 6k Hz sample rate by using RAM access prior to selecting a 9xh configuration (see parameter 49 in Section 4.2). A sample rate other than 9.6k, 8k, 7k, or 6k Hz may be used (see parameters 43 and 44 in Section 4.2).

Since the ADPCM codec receiver, DTMF receiver, FSK flag pattern detector, and tone detectors may operate concurrently, their status bits or copies of their status bits are located in a single register so that the programmable interrupt may be used to monitor all concurrent features. Register 1A:0-7 contains ADPCM status bits as well as a tone detector status bit, copies of DTMF receiver status bits, and a copy of the FSK flag pattern detector status bit (Figure 3-1d).

10.2 ADPCM CODEC TRANSMITTER

As shown in Figure 10-2, the host provides 16-bit ADC speech samples to the coder input (see Section 10.3.1). The ADC speech samples are scaled and sent to the coder. If enabled, silence detection/deletion provides additional compression (see Section 10.3.5). With 2, 3, or 4 bits per sample compression at the 8k Hz default programmable sample rate, the 16-bit coder output words are provided at 16k, 24k, or 32k bps (1k, 1.5k, or 2k 16-bit words per second), respectively.

The host supplies the decoder with the 16-bit coded words. The speech samples are reconstructed and white noise is inserted if silence interpolation is enabled (see Section 10.3.5). The programmable white noise level may be set to zero for absolute silence insertion. Each reconstructed speech sample is scaled (see Section 10.3.4),

Table 10-1. Codec I/O and Modem State Selection

DCDEN	CDEN	RTS/RTSP	Decoder Input	Decoder Output	Coder Input	Coder Output	Modem State
0	0	Don't care	—	—	—	—	Receiver
0	1	Don't care	—	—	RXA or RAM Access 1	VBUF1x or VBUF2x	Receiver
1	0	OFF	VBUF1x	RAM Access 1	—	—	Receiver
1	0	ON	VBUF1x	TXA and RAM Access 1	—	—	Transmitter
1	1	OFF	VBUF1x	RAM Access 1	RXA	VBUF2x	Receiver
1	1	ON	VBUF1x	TXA	RAM Access 1	VBUF2x	Transmitter

Note: x = L or M

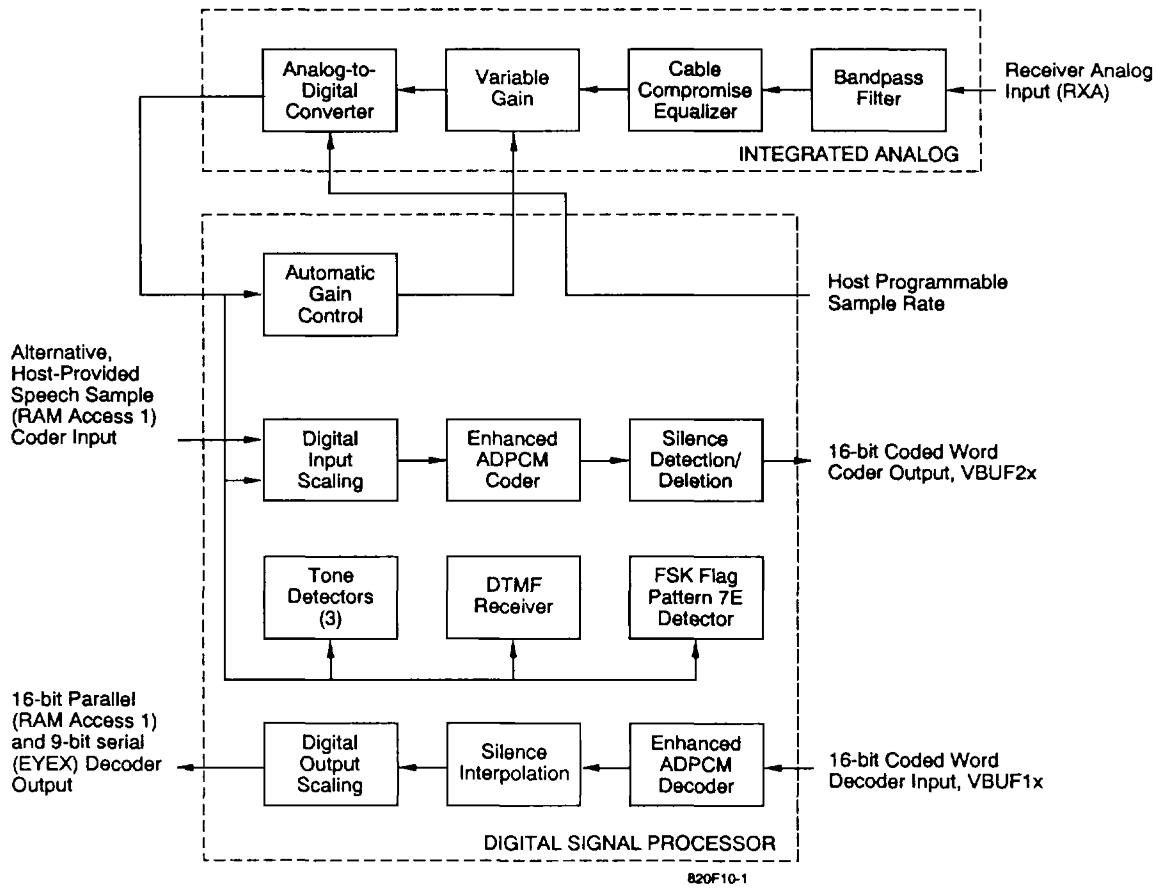


Figure 10-1. ADPCM Codec Receiver

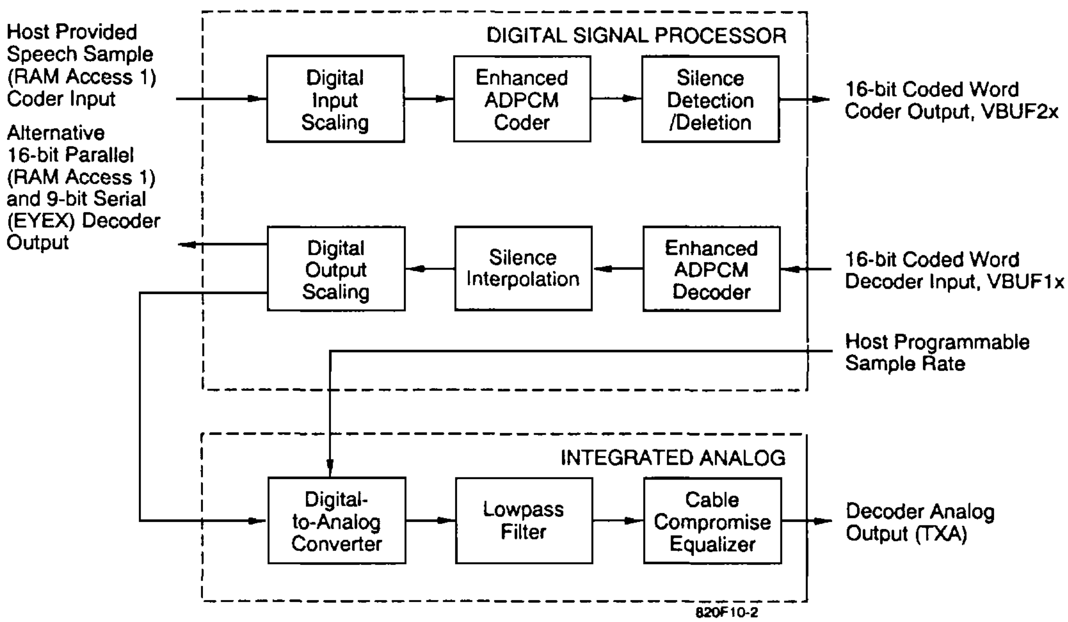


Figure 10-2. ADPCM Codec Transmitter

stored in RAM for host access (see Section 10.3.2), and sent to the integrated analog device's digital-to-analog converter. The integrated analog device filters the reconstructed speech while correcting for sin(x)/x attenuation.

10.3 ADPCM CODEC PROGRAMMING GUIDE

10.3.1 Host Provided ADC Speech Samples

The host may provide speech samples to the coder input through RAM Access 1. Before enabling the coder, the host must set the modem's internal ADC Speech Sample Scaling Parameter equal to zero, set the Host ADC Speech Sample Scaling Parameter equal to a host selected value, and set the Host ADC Speech Sample equal to the first coder input speech sample (see parameters 46, 47, and 48 in Section 4.2). The host writes a coder input speech sample to RAM every sample time when BA1 is set by the modem. The host writing to YDAL1 resets BA1. The host may choose to be interrupted whenever BA1 sets (bit IE1). The modem and host ADC Speech Sample Scaling Parameters must be restored either through RAM Access or reconfiguration after writing the last coder input speech sample, reading the last coder output 16-bit word, and disabling the coder.

The host may not provide coder input speech samples and receive 16-bit parallel and/or 9-bit serial decoder output (see Section 10.3.2) simultaneously since both operations require RAM Access 1.

10.3.2 Decoder 16-bit Parallel and 9-bit Serial Output

Using RAM Access 1, the host may read the 16-bit Reconstructed Speech Samples every sample time (see parameter 45 in Section 4.2). These samples may be directed under host control to an external host microprocessor-compatible 8- to 16-bit DAC for immediate playback, or stored (8 most significant bits) for later playback using the modem's voice mode transmitter (see Section 3.2.3). The modem sets BA1 informing the host that the next sample is available. The host may choose to be interrupted when BA1 sets (bit IE1). After reading the sample, the host must reset BA1 by reading YDAL1.

The serial eye pattern X output (EYEX in Table 2-5) provides a serial bit stream consisting of 9-bit words shifted sign bit first out of the modem with the sign bit repeated (Figure 2-6). Using RAM Access 1 to read the 16-bit Reconstructed Speech Samples (see parameter 45 in Section 4.2), the most significant byte of the reconstructed speech sample may be directed to EYEX. The host may first convert EYEX from serial-to-parallel form by a serial-to-parallel converter before converting EYEX to analog form by a digital-to-analog converter. The serial eye pattern strobe, EYESYNC, is used to load the digital-to-analog converter. EYESYNC has a frequency equal to the sample rate, and the serial eye pattern clock, EYECLK, has a frequency of 24*(sample rate). EYECLK* is a clock derived from EYESYNC and EYECLK for shifting EYEX data into a serial to parallel converter or the serial input of a digital-to-analog converter. Figure 2-6 shows the timing of EYECLK, EYESYNC, EYECLK*, and EYEX. The example circuit in Figure 2-7 shows a serial-to-parallel converter and a digital-to-analog converter interface circuit.

The host may not provide ADC speech samples to the coder (see Section 10.3.1) and receive 16-bit parallel and/or 9-bit serial decoder output simultaneously since both operations require RAM Access 1.

10.3.3 Coder AGC Slew Rate and Maximum Gain

The slew rate parameter controls how rapidly the Automatic Gain Control (AGC) will track amplitude changes in the received signal. The quality of ADPCM compressed speech is affected by the slew rate. The default codec receiver slew rate is loaded by the modem every sample time. The host may prevent the modem from loading the slew rate (bit FRZSL), then load its own slew rate using RAM access (see parameter 6 in Section 4.2). When the FSK Flag Pattern detector or DTMF receiver is enabled, the modem alters the slew rate in response to the received signal energy if bit FRZSL is reset. If the FRZSL bit is set, then the performance of the FSK Flag Pattern detector and the DTMF receiver are dependent upon the host selected slew rate.

When the host sets bit FRZSL, the voice mode receiver operates as described in Section 3.2.3. Note that the DTMF receiver, FSK Flag Pattern detector, and tone detectors may operate concurrently.

Using RAM access, the host may specify the maximum gain (0 to 50 dB) applied to the coder input signal (see parameter 55 in Section 4.2). Allowing high gain may degrade signal quality by increasing the noise level.

10.3.4 Codec Input and Output Digital Scaling

Before being compressed by the ADPCM coder, the coder input is digitally scaled using a RAM parameter (see parameter 46 in Section 4.2). The default value is 1/3 (2AABh). Increasing the value of this parameter provides positive gain to the reconstructed speech signal at the decoder output.

After being decompressed by the ADPCM decoder, the decoder output (reconstructed speech) is digitally scaled prior to transmission using a RAM parameter (see parameter 11 in Section 4.2). The default value is 1 (7FFFh). Decreasing the value of this parameter attentuates the reconstructed speech signal.

Parameter Selection Guidelines

The default codec parameters have been selected to offer the highest speech quality for 4, 3, and 2 bits per sample ADPCM compression with sample rates in the range of 6k to 9.6 k Hz for data rates of 12k to 38.4k bps. Lower data rates are possible using the coder silence detection/deletion option. The modem system designer may program parameter values to achieve a desired speech quality required for each specific application. The parameter values selected for 12k bps may not provide the optimum speech quality at 38.4k bps or other data rates between 12k and 38k bps.

The following is a recommended interactive method for parameter selection(see Figure 10-3). Note that the recommended method to select coder silence detection/deletion and decoder silence interpolation parameters is given in Section 10.3.5.

1. Select 4, 3, or 2 bits per sample ADPCM compression and a sample rate. The specific application will dictate a higher data rate for best speech quality or a lower data rate for minimum storage requirements. The data rate need not be constant. Under host control, it may start at a higher rate and decrease as the available memory is reduced.
2. Compress and playback a message repeatedly as necessary.
   a. If the background noise level is too high, reduce the AGC coder input gain, dBTHR (parameter 55 in Section 4.2).
   b. If the message tends to increase in volume where the beginning of the message may be distorted, then set bit FRZSL and increase the slew rate (parameter 6 in Section 4.2).
   c. If the playback level is too low, increase the coder digital input scaling parameter, ADCS (parameter 46 in Section 4.2). The maximum AGC coder input gain may also be increased if the background noise level is low.
   d. If the playback level is too high, decrease the decoder transmit output level (parameter 10 in Section 4.2).

10.3.5 Codec Silence Detection/Deletion and Interpolation

Silence deletion reduces the bit rate necessary to digitally record speech via ADPCM compression. "Background noise deletion" is more accurate than "silence deletion", however, the term "silence" is used with the understanding that it represents "background noise."

Because speech quality is highly subjective, the silence detection/deletion feature is host programmable. Through RAM access, the parameters determining how much silence is detected/deleted may be changed.

Upon ADPCM decoding, white noise at a host definable level is inserted for the duration of the silence interval previously detected and deleted by the ADPCM coder.

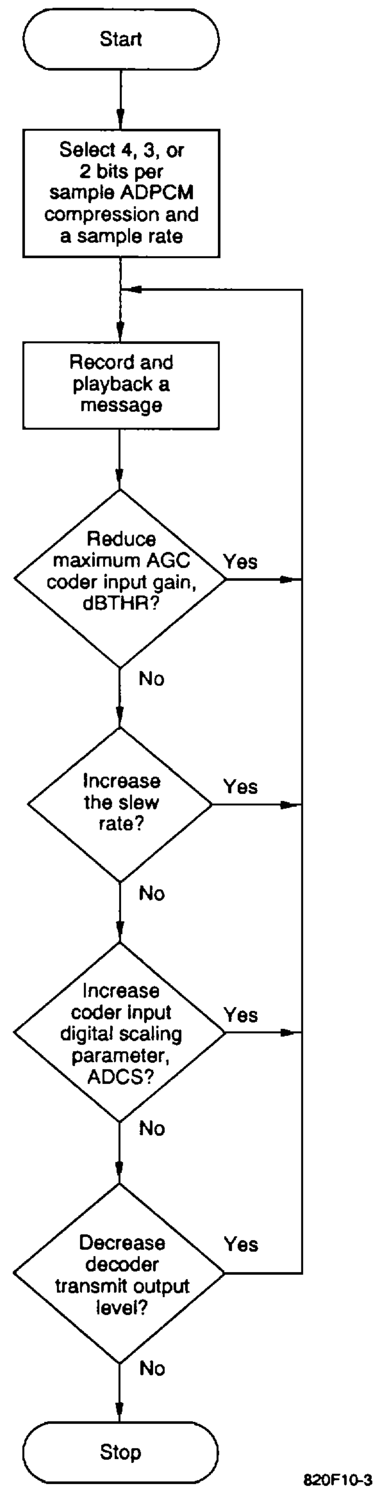


Figure 10-3. Codec Parameter Selection

Coder Silence Detection/Deletion

Prior to silence detection, the coder passes the coded output, 16 bits at a time, to the host (Figure 10-4a). Once silence is detected, a maximum of 32,768 sample periods may pass before any more data is given to the host. Once this maximum time interval is reached or speech is detected, a 16-bit code word is passed to the host. The next 16-bit coder output represents the full or partial duration of the detected silence interval.

If speech is detected, the coder resumes its normal operation, otherwise, silence interval measurements continue.

The synchronization between the coder and decoder is shown in Figure 10-4a, first for the silence interval less than 32,768 sample periods, and then for the silence interval greater than 32,768 sample periods.

Decoder Silence Interpolation

Upon recognizing the silence codeword in the decoder input file, the decoder silence interpolation routine halts the ADPCM decompression. White noise is inserted and transmitted at a default level of -36 ± 1 dB for the duration of the silence interval. The modem scales the output of the noise generator by a random noise parameter, RANOISE (see parameter 50 in Section 4.2). It has been observed that inserting low level white noise (not absolute silence) during playback of silence intervals improves perceived speech quality.

Parameter Selection Guidelines

The silence detection/deletion and interpolation parameters have been selected to provide significant silence deletion. The following guidelines will help to achieve more/less silence deletion.

Four parameters are used to detect speech and silence: MTHRESH, MADAPT, SILSPE, and SPESIL. They are presented below and in greater detail in Section 4.2 (see parameters 51, 52, 53, and 54).

If silence deletion is to be used on prerecorded speech files, the parameters may be changed for each file to achieve maximum speech quality and compression.

The following is a suggested interactive method for selecting parameter values (see Figure 10-5):

1. To perceive the amount of silence being deleted, raise the inserted noise level by increasing RANOISE. Once all other parameter values are selected, reduce RANOISE to an acceptable level.
2. Record and playback the desired file using the parameter default values (except RANOISE).
3. If speech is deleted, do the following:
   a. If the beginning of words are deleted, lower SPESIL so that the silence-to-speech transition is detected earlier.
   b. If the end of words are deleted, lower SILSPE so that the speech-to-silence transition is detected later.
   c. If lowering SILSPE and SPESIL in (a) and (b) above have minimal effects, lower MADAPT.
   d. Keep MADAPT as high as possible. MADAPT is too high if speech is being deleted at any point during playback.
4. If not enough silence is deleted, raise MTHRESH until some speech is deleted, and repeat at step 3.

10.4 ADPCM CODEC APPLICATION GUIDE

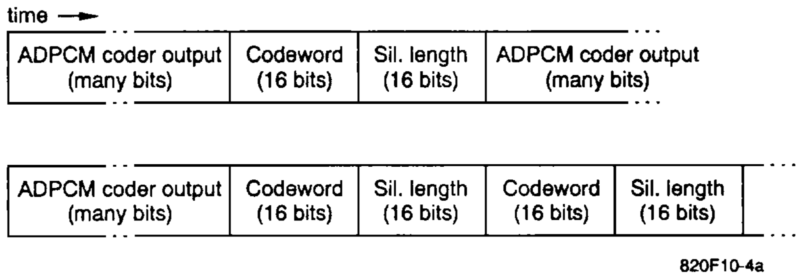
10.4.1 Codec Operation

After configuring to ADPCM and waiting for the SETUP bit to reset, the host should perform a RAM access 1 read operation of any RAM address. Waiting for the BA1 bit to set will preclude the modem from overwriting host changes to ADPCM control bits in register 0E:0-7 with default values (see Table 3-1d).

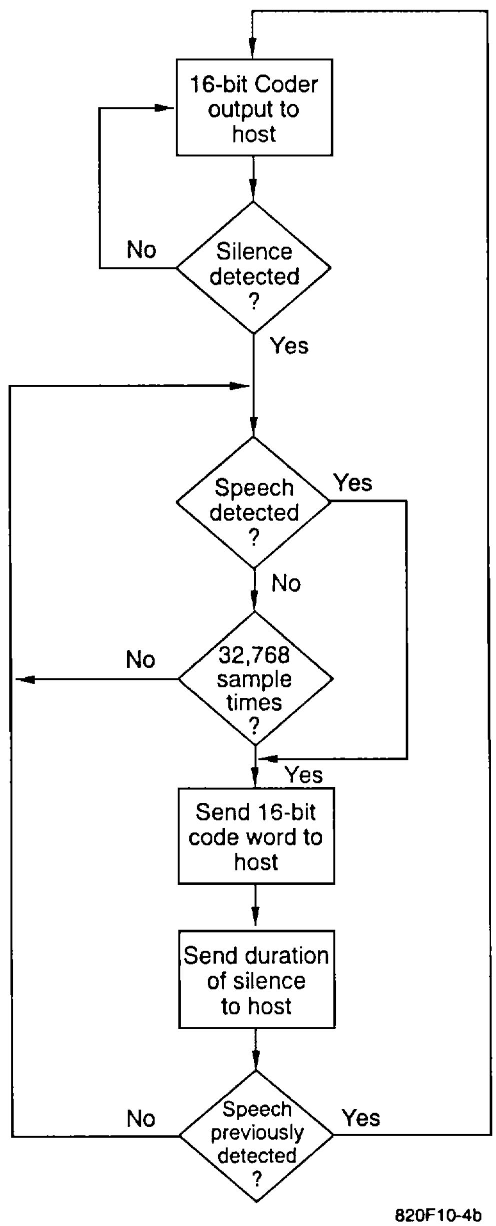
The coder writes 16-bit coded words to output register VBUF2x and sets status bit CDBA. If the decoder is disabled, the coder also writes to output register VBUF1x and sets status bit BA2. When the host reads VBUF1L, the modem resets BA2. CDBA must be reset by the host. The host must verify that the CDBA bit is reset before proceeding. The programmable interrupt may be enabled (bit PIE) to interrupt the host whenever CDBA sets to indicate that VBUF2x is full. The host may also be interrupted when BA2 sets (bit IE2) to indicate that VBUF1x is full. The host should disable the coder immediately after reading the last coded word from VBUF1x/VBUF2x.

The host supplies the decoder with the 16-bit coder output words by writing to VBUF1x when BA2 and DCDBA are set by the decoder. The first 16-bit decoder input must be written to VBUF1x and DCDBA reset before the decoder is enabled. When the host writes to VBUF1x, the modem resets BA2. DCDBA must be reset by the host. The host must verify that the DCDBA bit is reset before proceeding. The programmable interrupt may interrupt the host whenever DCDBA sets or the host may be interrupted whenever BA2 sets indicating VBUF1x is empty. After writing the last 16-bit decoder input to VBUF1x and resetting DCDBA, the host waits for BA2 or DCDBA to set then disables the decoder.

Figure 10-6 is a flowchart of the ADPCM coder and Figure 10-7 is a flowchart of the ADPCM decoder. In these flowcharts, only the coder or decoder is enabled, the host does not provide ADC speech samples, the decoder output is sent to TXA, and no interrupts are enabled. Figure 10-8 is a comprehensive flowchart of the ADPCM codec and its concurrent features. In this flowchart, both coder, decoder, and all other features may be enabled, the host may provide ADC speech samples, the host may elect not to send the decoder output to TXA, and the programmable interrupt and BA1 interrupt are used extensively. The use



a. Coder and Decoder Synchronization



b. Coder Silence Detection/Deletion

Figure 10-4. Coder Silence Detection/Deletion

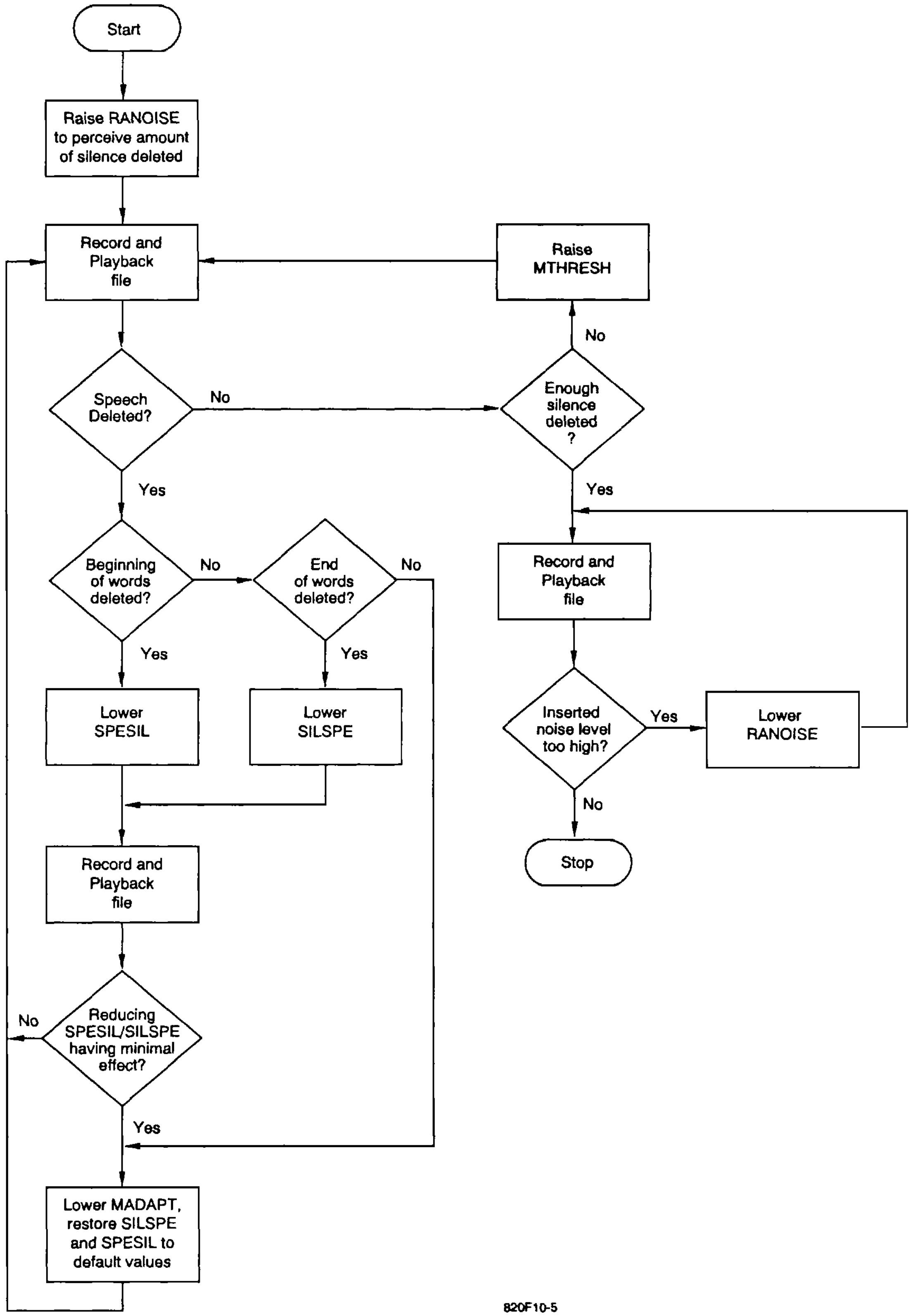


Figure 10-5. Silence Parameter Selection

of interrupts is optional. The host may instead poll each of the status bits.

10.4.2 Prerecorded Speech Signal Level

When using the ADPCM coder to compress prerecorded speech signals, the host should record these signals such that the peak voltage is 2.8 V when measured at the modem's RXA input.

10.4.3 Transmitter AC Coupling

To remove any DC offset that may be present at the transmitter output, an AC coupling capacitor (0.1 µF, 20%, 50V) may be placed in series between the modem TXOUT pin (QUIP pin no. 28 or PLCC pin no. 34) and resistor R7 (34.8 K Ω) shown in Figures 12-1 and 12-2.

10.4.4 Concurrent Features Maximum Sample Rates

Table 10-2 lists the maximum sample rates for selected concurrent features. A feature is enabled if there is a 1 in its column. It is disabled if there is a 0 in its column. The control bits are ordered left to right as they appear in register 0E (see Figure 3-1d). After the host enables the desired features, register 0E will have the value tabulated in the Hex column.

10.4.5 Coder Output Files and Decoder Output Tapes

ADPCM coder output (decoder input) files on disk and taped recordings of decoder decompressed speech signals are available upon request (contact your local Rockwell sales office). These files and tapes include speech samples compressed using 4, 3, and 2 bits per sample with sample rates of 8k, 7k, and 6k Hz for 32k, 28k, 24k, 21k, 18k, 16k, 14k, and 12k bps compressed data. The quality of the decoder reconstructed speech signal when using one of the provided coder output files should be comparable to the quality of the decoder reconstructed speech signals as recorded on the tapes.

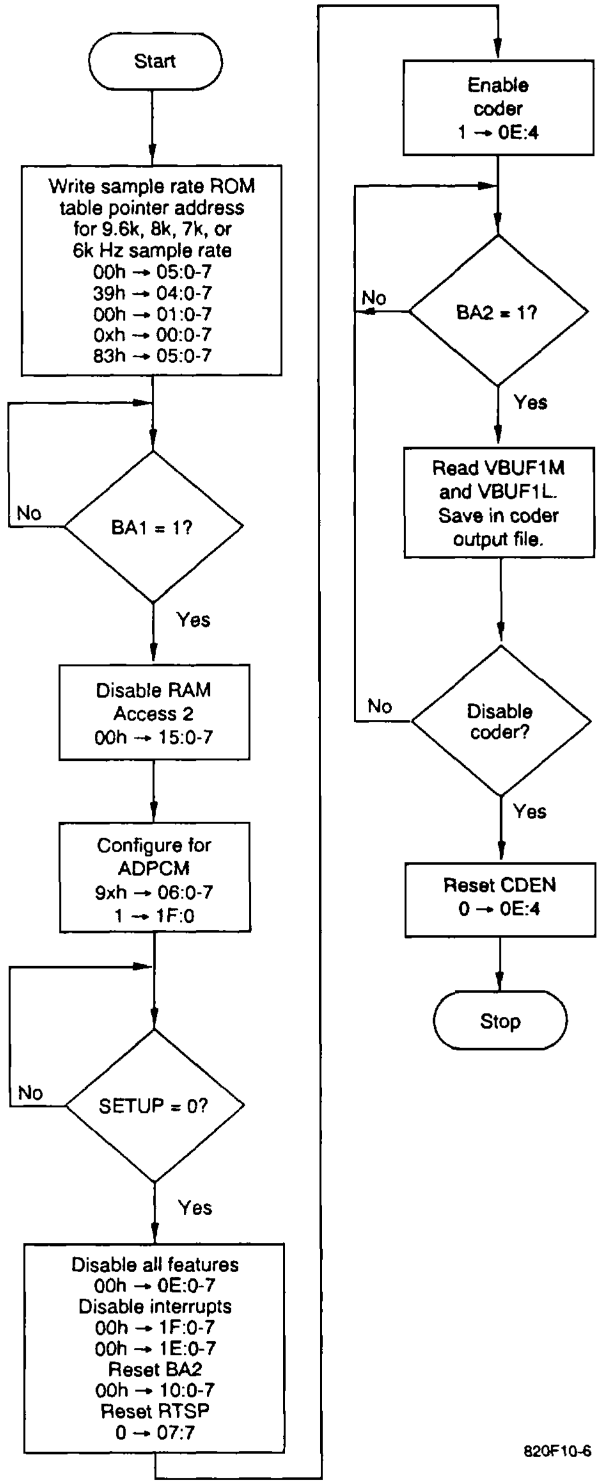


Figure 10-6. ADPCM Coder Operation

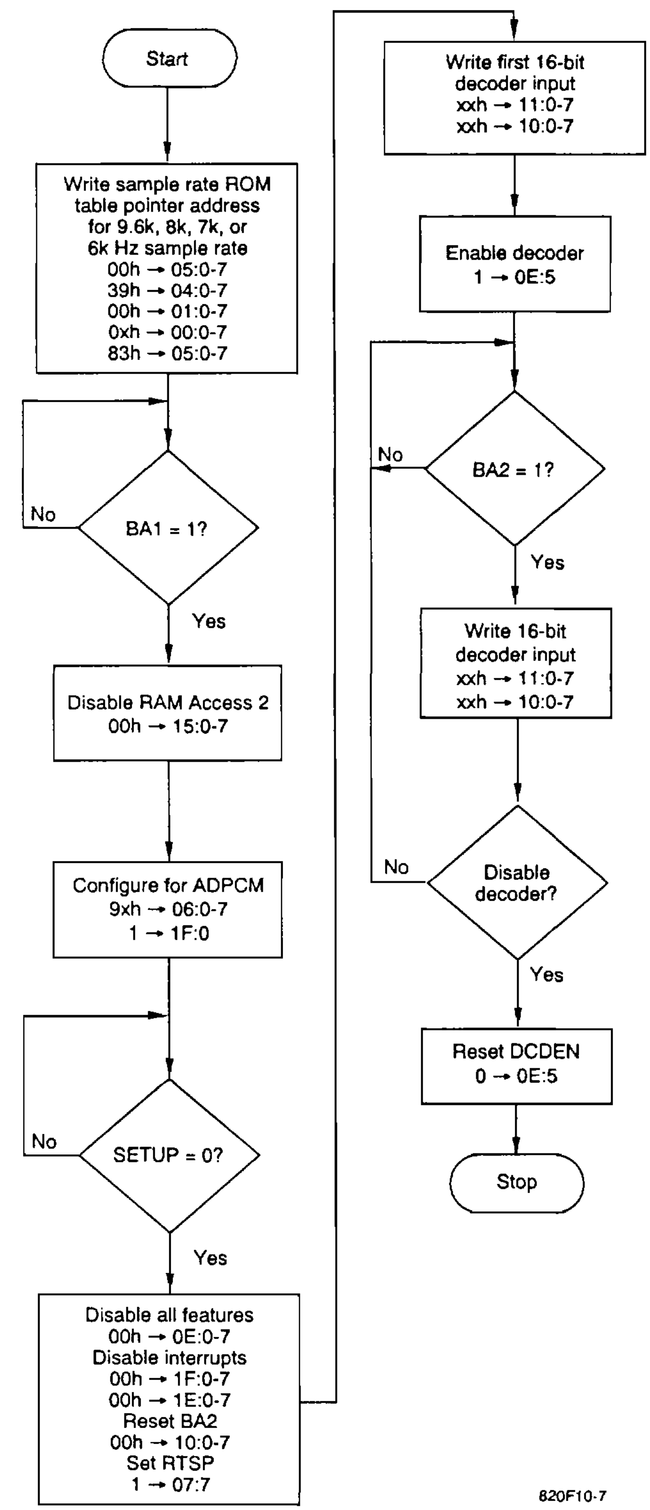


Figure 10-7. ADPCM Decoder Operation

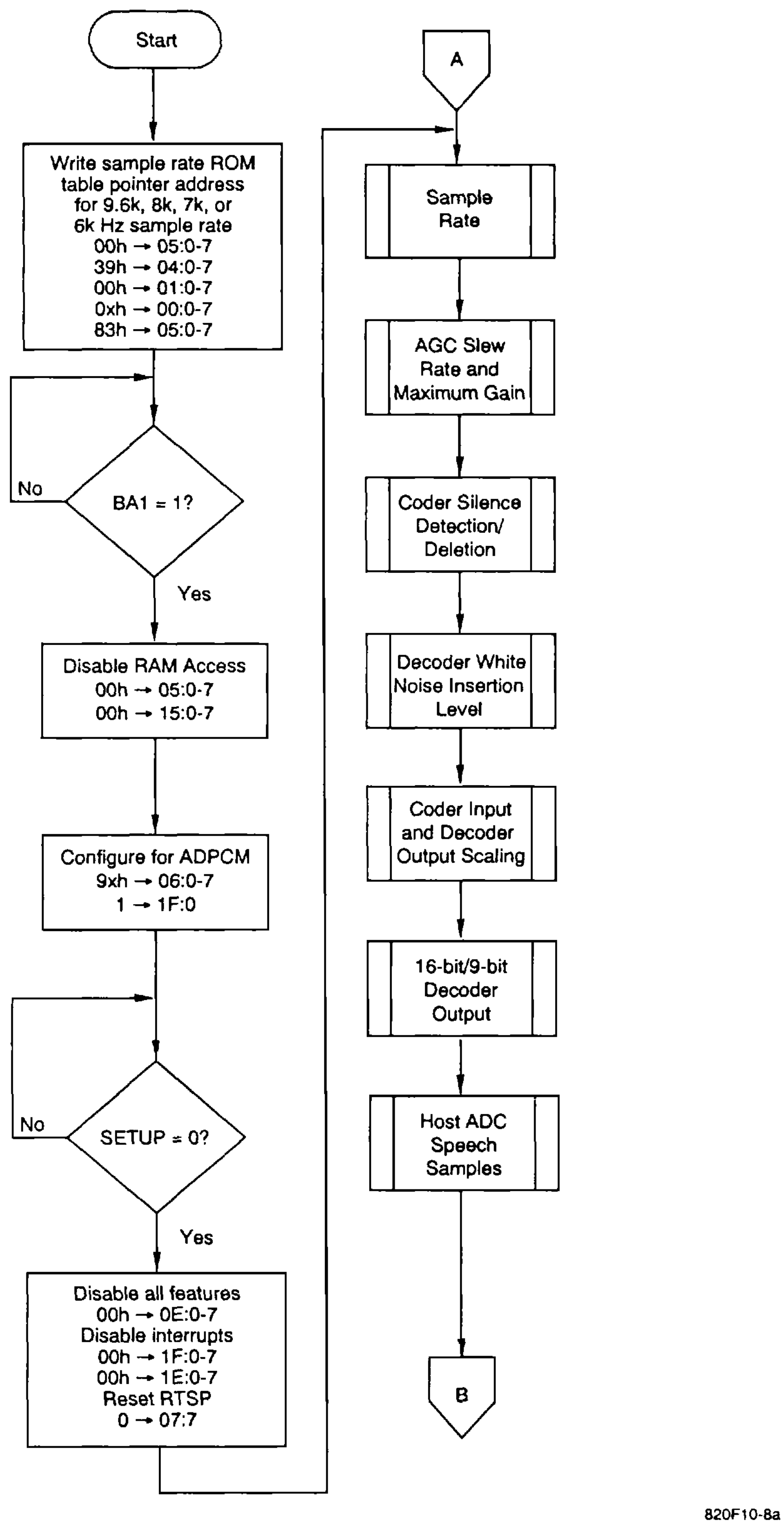


Figure 10-8. ADPCM Codec Operation

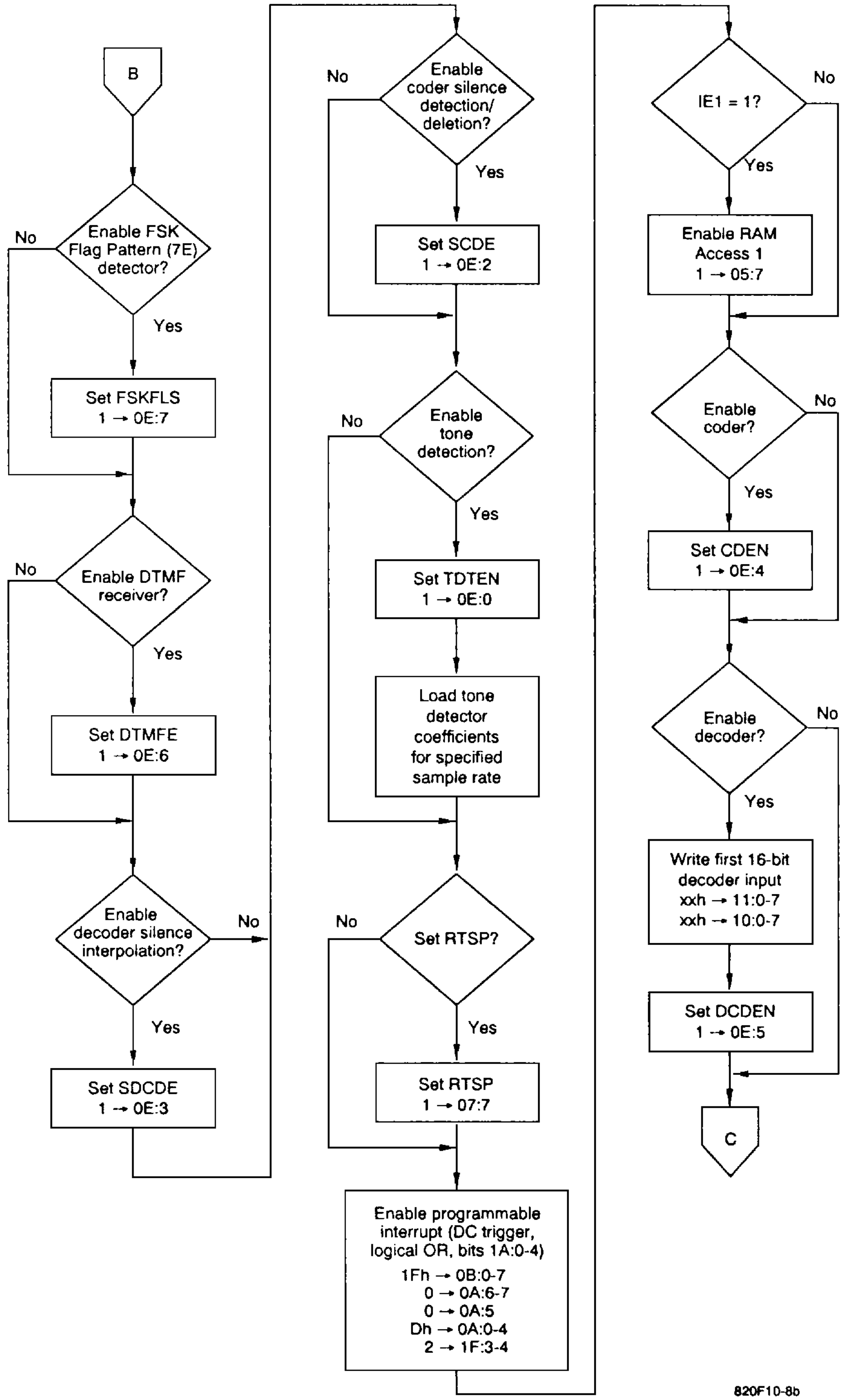


Figure 10-8. ADPCM Codec Operation (Cont'd)

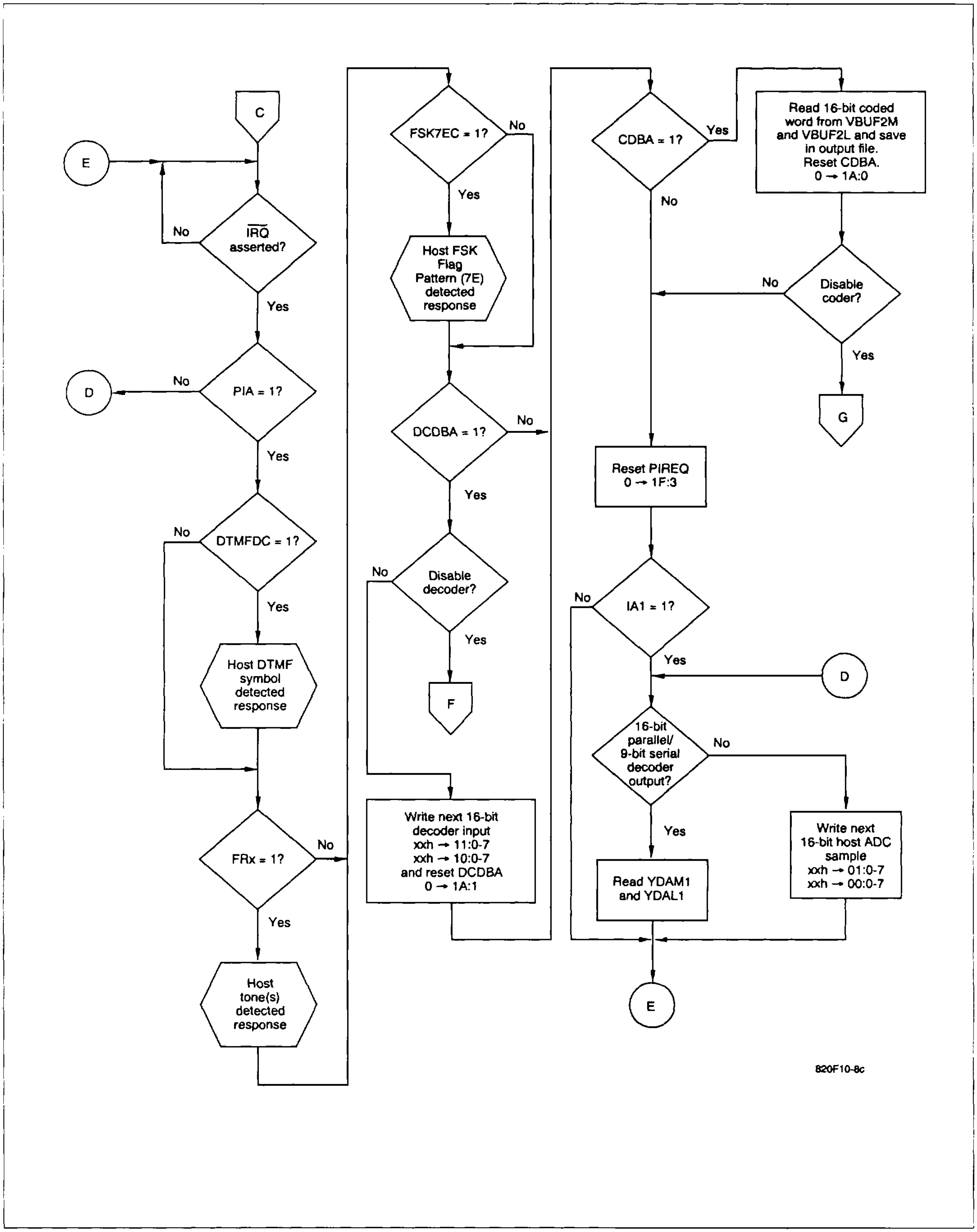


Figure 10-8. ADPCM Codec Operation (Cont'd)

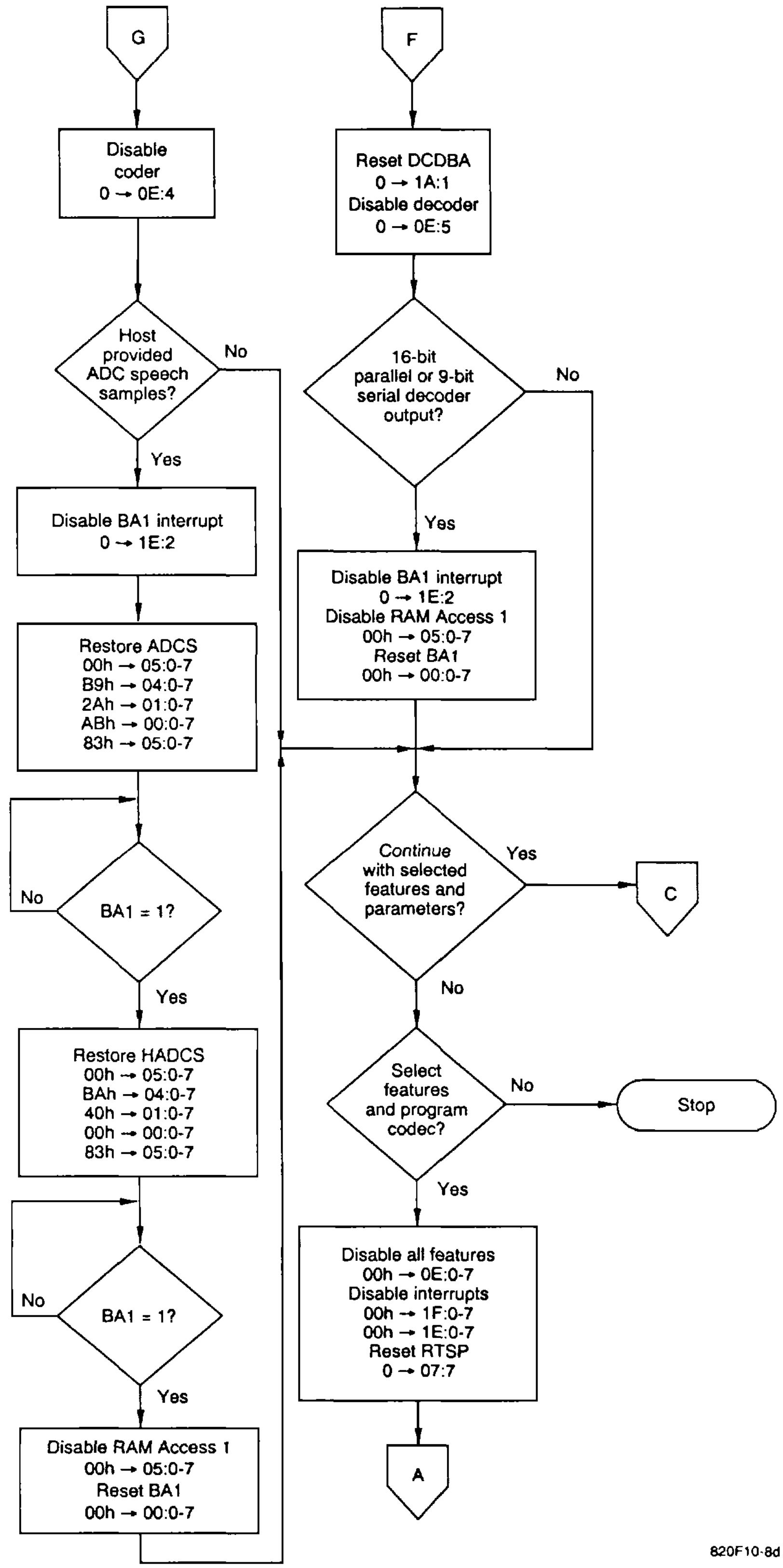


Figure 10-8. ADPCM Codec Operation (Cont'd)

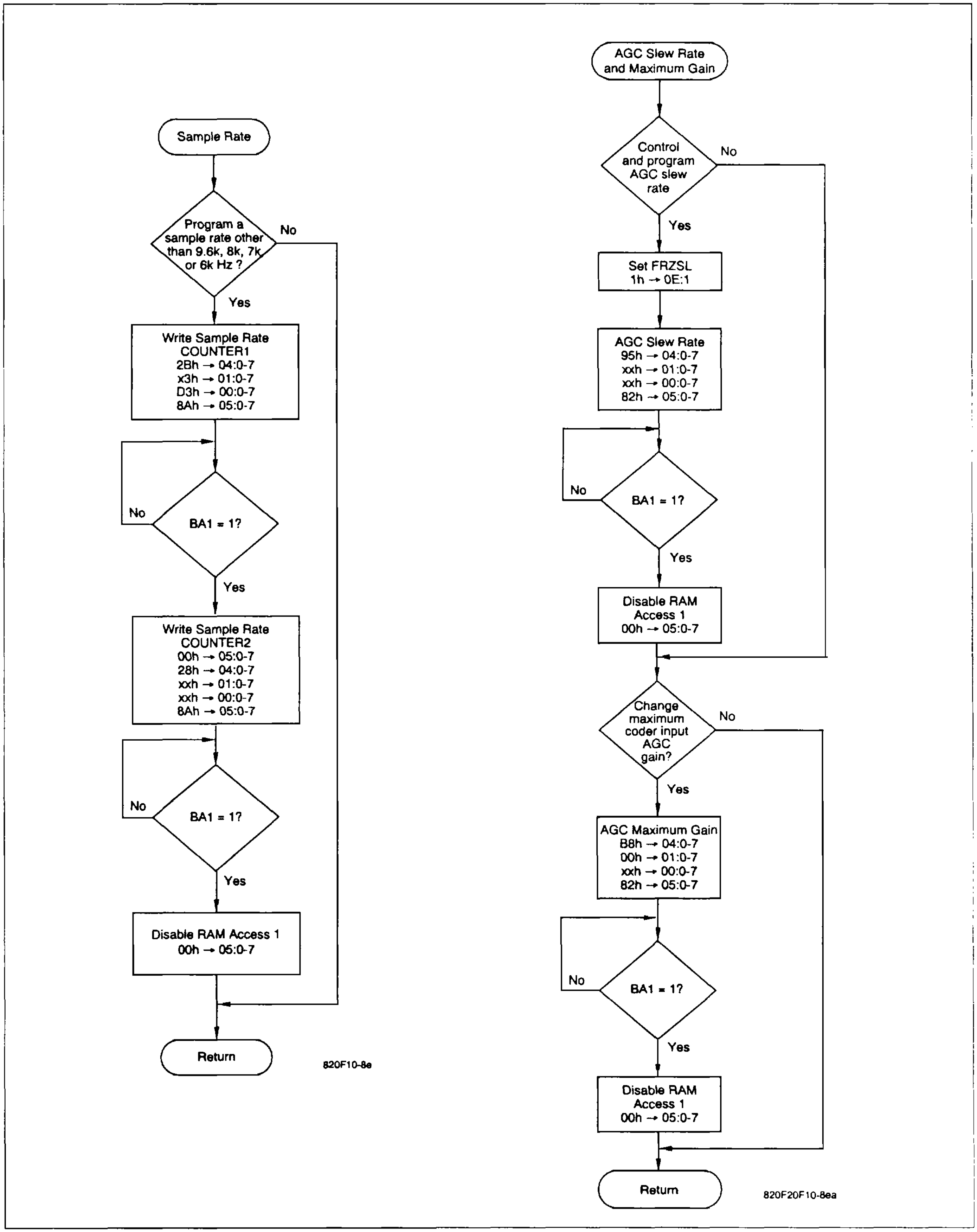


Figure 10-8. ADPCM Codec Operation (Cont'd)

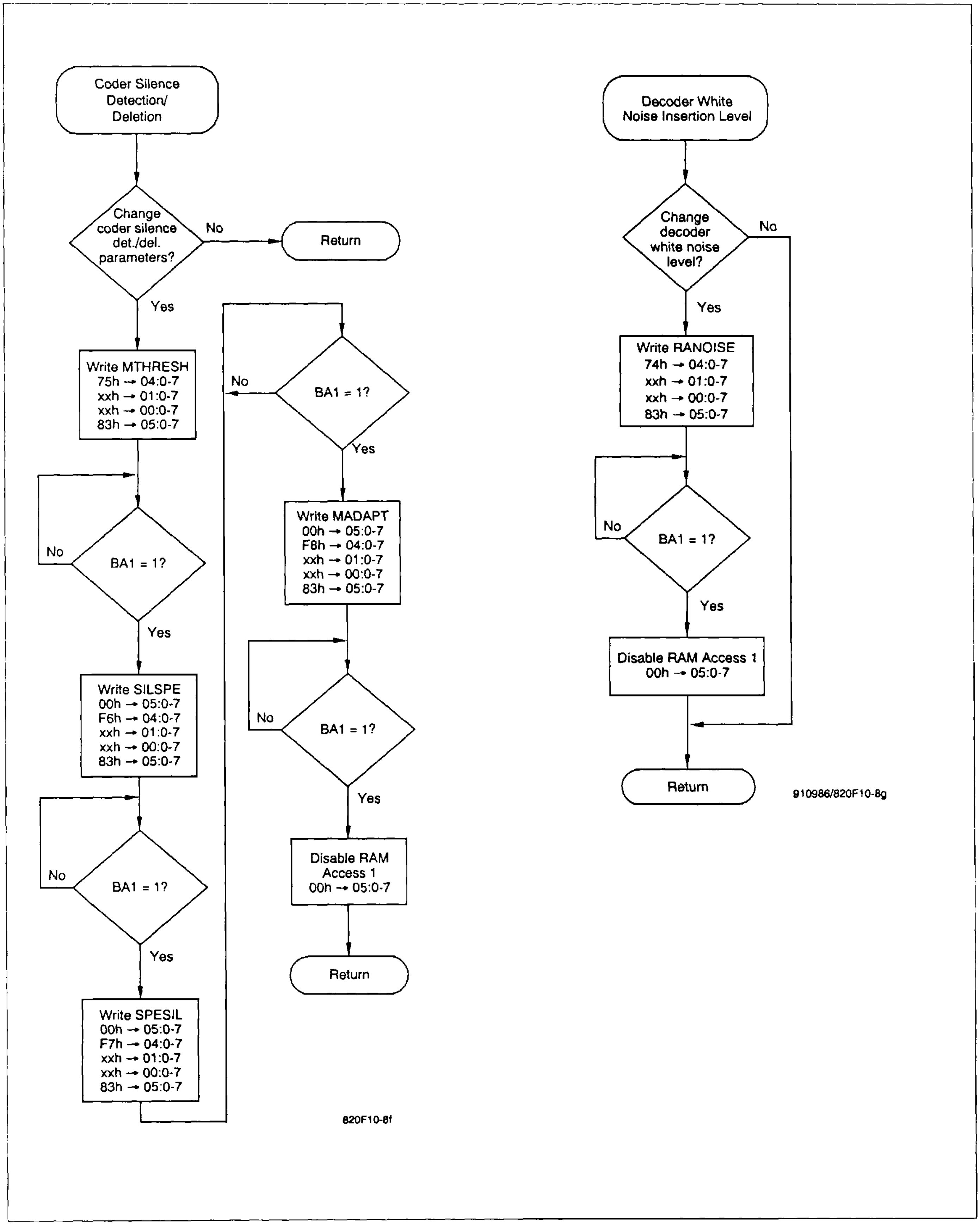


Figure 10-8. ADPCM Codec Operation (Cont'd)

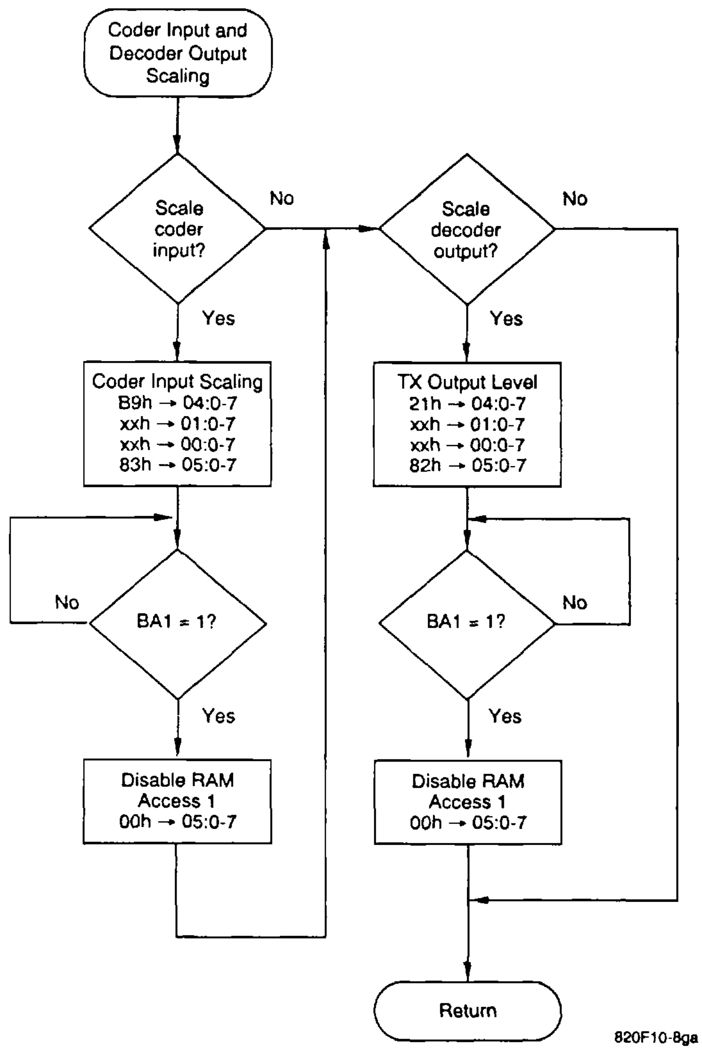


Figure 10-8. ADPCM Codec Operation (Cont'd)

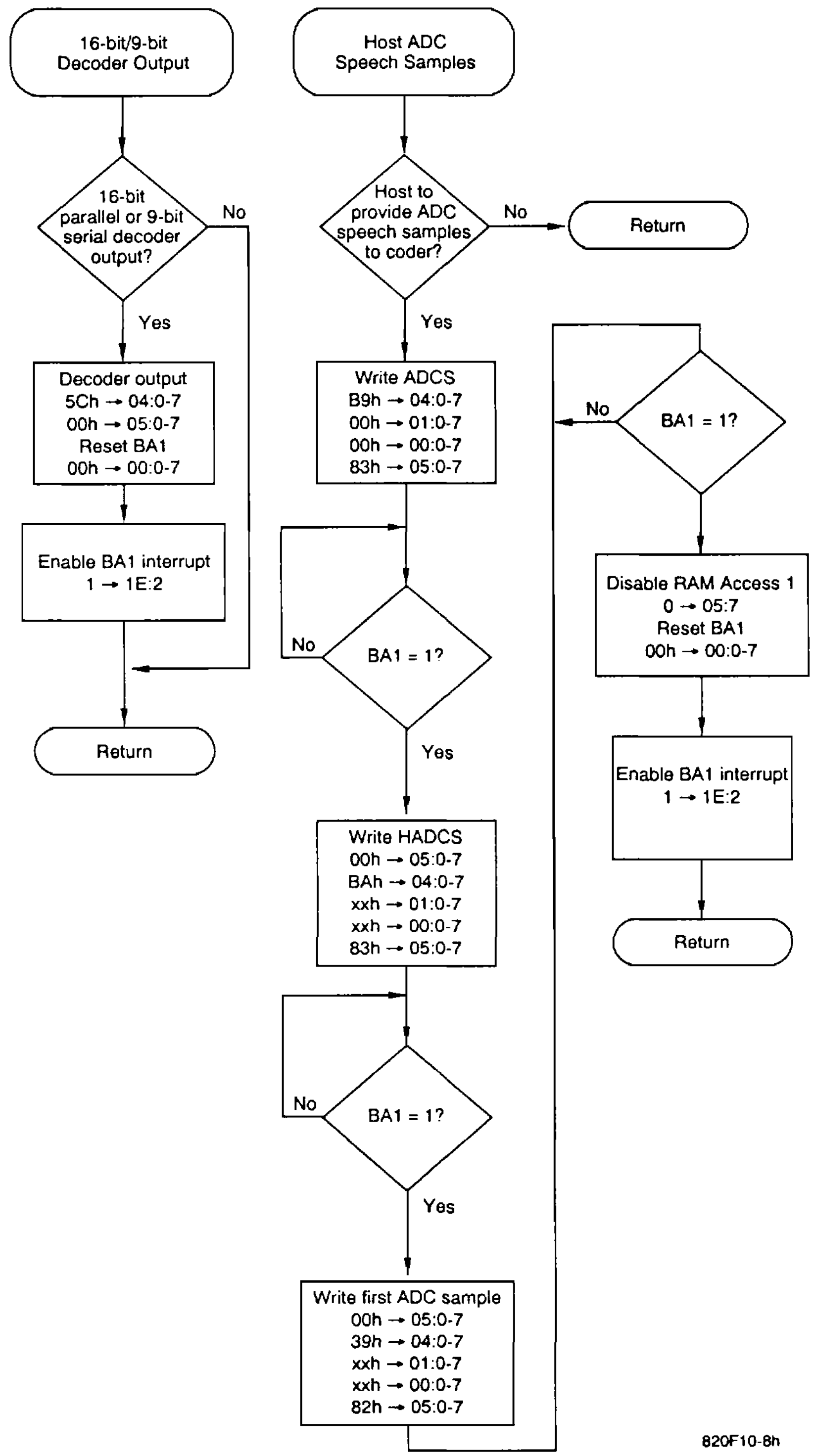


Figure 10-8. ADPCM Codec Operation (Cont'd)

Table 10-2. ADPCM Codec Maximum Sample Rate

FSKFLS	DTMFE	DCDEN	CDEN	SDCDE	SCDE	FRZSL	TDTEN	Hex	MAX F_s (Hz)
0	0	0	0	0	0	0	0	00	9600
0	0	0	0	0	0	0	1	01	9600
0	0	0	0	0	0	1	1	03	9600
0	0	0	1	0	0	0	0	10	9600
0	0	0	1	0	0	0	1	11	9600
0	0	0	1	0	0	1	0	12	9600
0	0	0	1	0	0	1	1	13	9600
0	0	0	1	0	1	0	0	14	9600
0	0	0	1	0	1	0	1	15	9600
0	0	0	1	0	1	1	0	16	9600
0	0	0	1	0	1	1	1	17	9600
0	0	1	0	0	0	0	0	20	9600
0	0	1	0	0	0	0	1	21	9600
0	0	1	0	0	0	1	0	22	9600
0	0	1	0	0	0	1	1	23	9600
0	0	1	0	1	0	0	0	28	9600
0	0	1	0	1	0	0	1	29	9600
0	0	1	0	1	0	1	0	2A	9600
0	0	1	0	1	0	1	1	2B	9600
0	0	1	1	0	0	0	0	30	8000
0	0	1	1	0	0	0	1	31	8000
0	0	1	1	0	0	1	0	32	8000
0	0	1	1	0	0	1	1	33	8000
0	0	1	1	0	1	0	0	34	8000
0	0	1	1	0	1	0	1	35	7000
0	0	1	1	0	1	1	0	36	8000
0	0	1	1	0	1	1	1	37	7000
0	0	1	1	1	0	0	0	38	8000
0	0	1	1	1	0	0	1	39	8000
0	0	1	1	1	0	1	0	3A	8000
0	0	1	1	1	0	1	1	3B	8000
0	0	1	1	1	1	0	0	3C	8000
0	0	1	1	1	1	0	1	3D	7000
0	0	1	1	1	1	1	0	3E	8000
0	0	1	1	1	1	1	1	3F	7000
0	1	0	0	0	0	0	0	40	9600
0	1	0	0	0	0	0	1	41	9600
0	1	0	0	0	0	1	0	42	9600
0	1	0	0	0	0	1	1	43	9600
0	1	0	1	0	0	0	0	50	9600
0	1	0	1	0	0	0	1	51	8000
0	1	0	1	0	0	1	0	52	9600
0	1	0	1	0	0	1	1	53	8000
0	1	0	1	0	1	0	0	54	8000
0	1	0	1	0	1	0	1	55	8000
0	1	0	1	0	1	1	0	56	8000
0	1	0	1	0	1	1	1	57	8000

Table 10-2. ADPCM Codec Maximum Sample Rate (Cont'd)

FSKFLS	DTMFE	DCDEN	CDEN	SDCDE	SCDE	FRZSL	TDTEN	Hex	MAX F_s (Hz)
0	1	1	0	0	0	0	0	60	9600
0	1	1	0	0	0	0	1	61	8000
0	1	1	0	0	0	1	0	62	9600
0	1	1	0	0	0	1	1	63	8000
0	1	1	0	1	0	0	0	68	9600
0	1	1	0	1	0	0	1	69	8000
0	1	1	0	1	0	1	0	6A	9600
0	1	1	0	1	0	1	1	6B	8000
0	1	1	1	0	0	0	0	70	7000
0	1	1	1	0	0	0	1	71	6000
0	1	1	1	0	0	1	0	72	7000
0	1	1	1	0	0	1	1	73	6000
0	1	1	1	0	1	0	0	74	6000
0	1	1	1	0	1	0	1	75	6000
0	1	1	1	0	1	1	0	76	6000
0	1	1	1	0	1	1	1	77	6000
0	1	1	1	1	0	0	0	78	7000
0	1	1	1	1	0	0	1	79	6000
0	1	1	1	1	0	1	0	7A	7000
0	1	1	1	1	0	1	1	7B	6000
0	1	1	1	1	1	0	0	7C	6000
0	1	1	1	1	1	0	1	7D	6000
0	1	1	1	1	1	1	0	7E	6000
0	1	1	1	1	1	1	1	7F	6000
1	0	0	0	0	0	0	0	80	9600
1	0	0	0	0	0	0	1	81	9600
1	0	0	0	0	0	1	0	82	9600
1	0	0	0	0	0	1	1	83	9600
1	0	0	1	0	0	0	0	90	9600
1	0	0	1	0	0	0	1	91	9600
1	0	0	1	0	0	1	0	91	9600
1	0	0	1	0	0	1	1	93	9600
1	0	0	1	0	1	0	0	94	9600
1	0	0	1	0	1	0	1	95	9600
1	0	0	1	0	1	1	0	96	9600
1	0	0	1	0	1	1	1	97	9600
1	0	1	0	0	0	0	0	A0	9600
1	0	1	0	0	0	0	1	A1	9600
1	0	1	0	0	0	1	0	A2	9600
1	0	1	0	0	0	1	1	A3	9600
1	0	1	0	1	0	0	0	A8	9600
1	0	1	0	1	0	0	1	A9	9600
1	0	1	0	1	0	1	0	AA	9600
1	0	1	0	1	0	1	1	AB	9600
1	0	1	1	0	0	0	0	B0	8000
1	0	1	1	0	0	0	1	B1	8000
1	0	1	1	0	0	1	0	B2	8000
1	0	1	1	0	0	1	1	B3	8000
1	0	1	1	0	1	0	0	B4	8000
1	0	1	1	0	1	0	1	B5	7000
1	0	1	1	0	1	1	0	B6	8000
1	0	1	1	0	1	1	1	B7	7000
1	0	1	1	1	0	0	0	B8	8000
1	0	1	1	1	0	0	1	B9	7000
1	0	1	1	1	0	1	0	BA	8000
1	0	1	1	1	0	1	1	BB	7000
1	0	1	1	1	1	0	0	BC	8000
1	0	1	1	1	1	0	1	BD	7000
1	0	1	1	1	1	1	0	BE	8000
1	0	1	1	1	1	1	1	BF	7000

Table 10-2. ADPCM Codec Maximum Sample Rate (Cont'd)

FSKFLS	DTMFE	DCDEN	CDEN	SDCDE	SCDE	FRZSL	TDTEN	Hex	MAX F_S (Hz)
1	1	0	0	0	0	0	0	C0	9600
1	1	0	0	0	0	0	1	C1	9600
1	1	0	0	0	0	1	0	C2	9600
1	1	0	0	0	0	1	1	C3	9600
1	1	0	1	0	0	0	0	D0	9600
1	1	0	1	0	0	0	1	D1	8000
1	1	0	1	0	0	1	0	D2	9600
1	1	0	1	0	0	1	1	D3	8000
1	1	0	1	0	1	0	0	D4	8000
1	1	0	1	0	1	0	1	D5	8000
1	1	0	1	0	1	1	0	D6	8000
1	1	0	1	0	1	1	1	D7	8000
1	1	1	0	0	0	0	0	E0	9600
1	1	1	0	0	0	0	1	E1	8000
1	1	1	0	0	0	1	0	E2	9600
1	1	1	0	0	0	1	1	E3	8000
1	1	1	0	1	0	0	0	E8	8000
1	1	1	0	1	0	0	1	E9	8000
1	1	1	0	1	0	1	0	EA	8000
1	1	1	0	1	0	1	1	EB	8000
1	1	1	1	0	0	0	0	F0	7000
1	1	1	1	0	0	0	1	F1	6000
1	1	1	1	0	0	1	0	F2	7000
1	1	1	1	0	0	1	1	F3	6000
1	1	1	1	0	1	0	0	F4	6000
1	1	1	1	0	1	0	1	F5	6000
1	1	1	1	0	1	1	0	F6	6000
1	1	1	1	0	1	1	1	F7	6000
1	1	1	1	1	0	0	0	F8	6000
1	1	1	1	1	0	0	1	F9	6000
1	1	1	1	1	0	1	0	FA	6000
1	1	1	1	1	0	1	1	FB	6000
1	1	1	1	1	1	0	0	FC	6000
1	1	1	1	1	1	0	1	FD	6000
1	1	1	1	1	1	1	0	FE	6000
1	1	1	1	1	1	1	1	FF	6000

11 PROGRAMMABLE DIGITAL EQUALIZER (PDE)

11.1 PDE DESCRIPTION

A programmable digital equalizer is provided in the R96VFX high speed receiver path as shown in Figure 11-1.

The programmable digital equalizer consists of four cascaded biquads. This is similar to the tone detectors when cascaded by enabling bit 12TH. The programmable digital equalizer is enabled by setting bit PDEQZ. The block is shown in Figure 11-2.

The programmable digital equalizer defaults to a Japanese two link delay equalizer, with 1.1 dB gain at 2700 Hz. The frequency response curves are shown in Figure 11-3.

11.2 PDE COEFFICIENTS

The equation to calculate the hex coefficients is:

$$\text{Coefficient}_{16} = \text{Coefficient} * 32768$$

The format is 16 bits, signed, twos complement. The coefficient range is from -1 (8000h) to +1 minus 1 least significant bit (7FFFh).

The poles and zeros are shown in Table 11-1.

The programmable digital equalizer RAM access codes are shown in Table 11-2.

Note that these parameters need to be changed only once. They are not written by the modem at any time other than power-on.

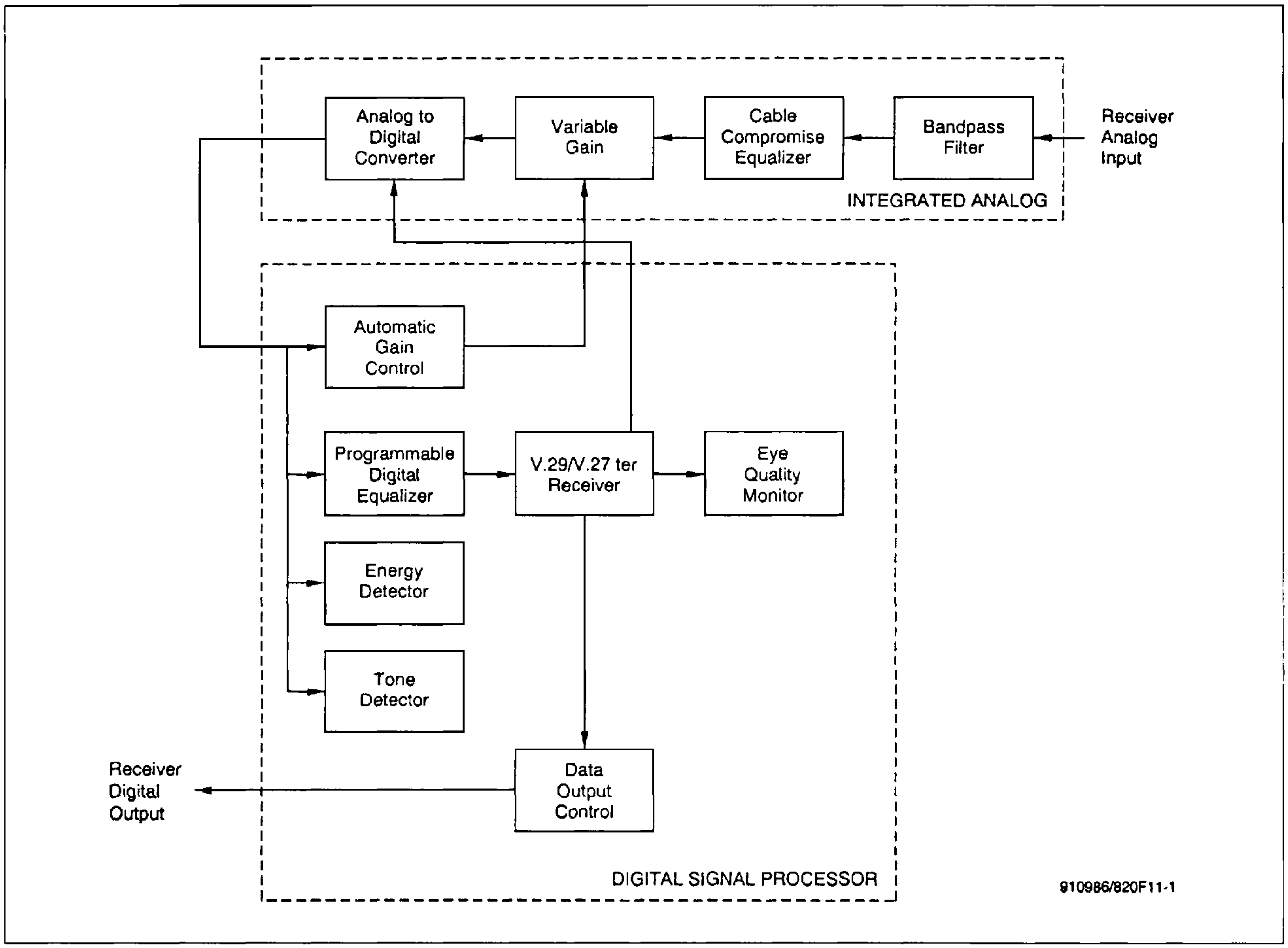


Figure 11-1. High Speed Receiver with PDE

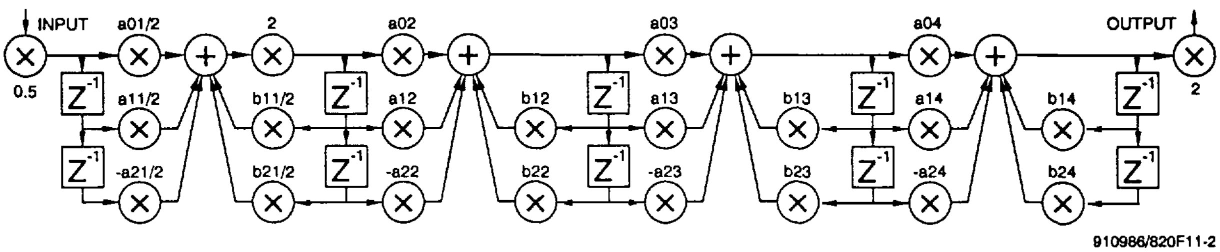


Figure 11-2. PDE Block Diagram

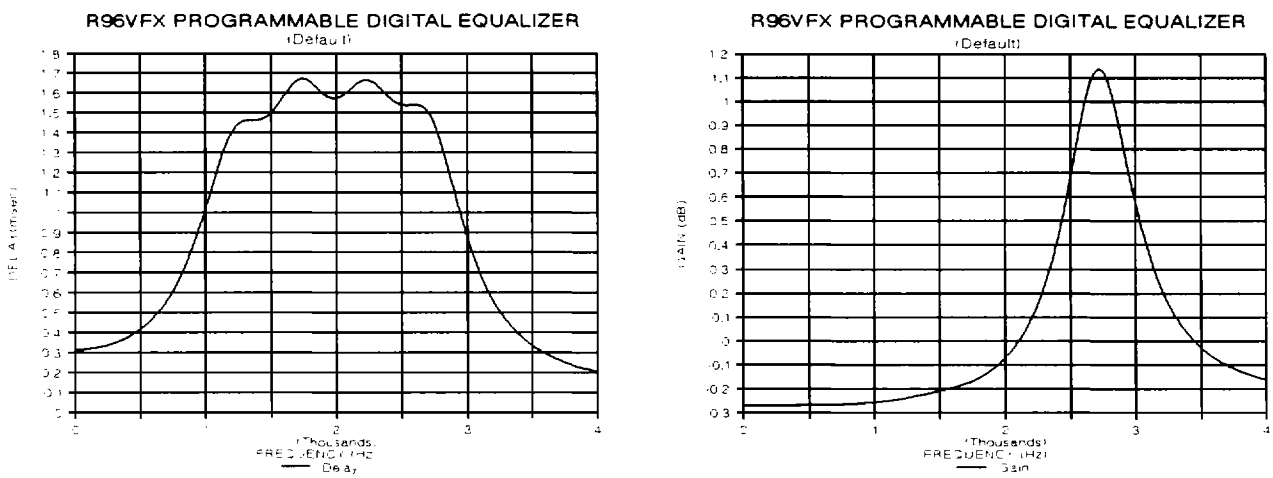


Figure 11-3. PDE Response

Table 11-1. PDE Poles and Zeros

Section Number	Poles	Zeros
1	0.794 @ 1215 Hz	1.26 @ 1215 Hz
2	0.798 @ 1728 Hz	1.25 @ 1728 Hz
3	0.793 @ 2241 Hz	1.26 @ 2241 Hz
4	0.830 @ 2713 Hz	1.27 @ 2713 Hz

Table 11-2. PDE RAM Access Codes

Name	BRx	CRx	IOx	ADDx	Read Reg. No.	Default Value (Hex)	Default Value (Dec)
a01/2	0	0	0	EC	0, 1	285C	0.31531771
a02	0	0	0	EE	0, 1	516C	0.63611724
a03	0	0	0	F0	0, 1	50A5	0.63002045
a04	0	0	0	F2	0, 1	4FB4	0.62269083
a11/2	0	1	0	6C	2, 3	B8D1	-0.55611875
a21/2	0	1	0	6D	2, 3	C000	-0.50000000
a12	0	1	0	6E	2, 3	A8FF	-0.67972752
a22	0	1	0	6F	2, 3	8000	-1.00000000
a13	0	1	0	70	2, 3	EAD7	-0.16531356
a23	0	1	0	71	2, 3	8000	-1.00000000
a14	0	1	0	72	2, 3	291D	0.32118352
a24	0	1	0	73	2, 3	8000	-1.00000000
b11/2	0	1	0	EE	0, 1	472F	0.55611875
b21/2	0	1	0	EF	0, 1	D7A4	-0.31531771
b12	0	1	0	F0	0, 1	5701	0.67972752
b22	0	1	0	F1	0, 1	AE94	-0.63611724
b13	0	1	0	F2	0, 1	1529	0.16531356
b23	0	1	0	F3	0, 1	AF5B	-0.63002045
b14	0	1	0	F4	0, 1	D4EA	-0.33660000
b24	0	1	0	F5	0, 1	AA61	-0.66890000

12 MODEM INTERFACE CIRCUIT

12.1 CIRCUIT AND COMPONENTS

The modem is supplied as a 68-pin PLCC or 64-pin QUIP device to be designed into OEM circuit boards. The recommended modem interface circuit (Figures 12-1 and 12-2) and parts (Table 12-1) illustrate the connections and components required to connect the modem to the OEM electronics.

Crystal/Oscillator Specifications

Tables 12-2 through 12-4 specify parameters for crystals or oscillators identified in these schematics.

AUXI Input Not Used

If the AUXI input is not used, resistors R10 and R16 can be eliminated and AUXI must be connected to AGND2.

CABLE1 and CABLE2 Isolation

When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3K ohm series resistor should be used on each input (CABLE1 and CABLE2) for isolation.

Transmit Level and Receive Threshold Trimmers

Resistors R7 and R17 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more than 99.8% of the units.

Table 12-1. Typical Modem Interface Parts List

Component Designation	Component Value	Manufacturer's Part Number	Suggested Manufacturer
C11, C13	1000 pF ±5%, 50V		
C7, C8, C9, C12, C14	0.1 μF ±20%, 50V		
C4, C6	0.33 μF ±20%, 50V		
C10	1.0 μF ±20%, 50V		
C5	10.0 μF ±10%, 25V	ECEBEF100	Panasonic
C2	18 pF ±5%, 50V		
C3	39 pF ±5%, 50V		
R4	3 Ω ± 5%, 1/4W		
R12	255 Ω ±1%, 1/4W		
R10, R16	1 KΩ±5%, 1/4W		
R6	3 KΩ ±5%, 1/4W		
R18, R19	10 KΩ ±1%, 1/4W		
R7	34.8 KΩ ±1%, 1/4W		
R17	46.4 KΩ ±1%, 1/4W		R–Ohm
R11	36.5 KΩ ±1%, 1/4W		R-Ohm
R14, R15	86.6 KΩ ±1%, 1/4W		
R5	2.7 MΩ ± 5%, 1/4W		
CR1	–5.1V ± 1%, regulator	1N4625D	Motorola
Y1 (except R96VFX)	24.00014 MHz	See Table 11-2	
Y1 (R96VFX)	26.39998 MHz	See Table 11-3	
Y2 (R96MFX and R96EFX)	24.00014 MHz	TC0-706AB*	Toyocom

* TC0-706AB is the only square wave generator recommended (see Table 12-4). A sine wave oscillator may alternatively be used (see Note 3 in Figures 12-1 and 12-2).

Table 12-2. 24.00014 MHz Crystal Specifications

Characteristic	Value
Nominal Frequency @ 25°C	24.00014 MHz
Frequency Tolerance @ 25°C	± 0.0015% (15 ppm)
Operating Temperature	0°C to 60°C
Storage Temperature	–55°C to 85°C
Temperature Stability (T_A = 0°C to 60°C)	± 0.003% (30 ppm)
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF max.
Load Capacitance	18 ± 0.2 pF
Drive Level (Test at 20 nW)	2.5 mW max.
Aging, Per Year	0.0005% (5 ppm)
Oscillation Mode	Fundamental
Series Resistance	25 Ω max.
Maximum Frequency Variation with 16.5 pF or 19.5 pF Load Capacitance	± 0.0035% (35 ppm)

Table 12-3. 26.39998 MHz Crystal Specifications

Characteristic	Value
Nominal Frequency @ 25°C	26.39998 MHz
Frequency Tolerance @ 25°C	± 0.0015% (15 ppm)
Operating Temperature	0°C to 60°C
Storage Temperature	–55°C to 85°C
Temperature Stability (T_A = 0°C to 60°C)	± 0.003% (30 ppm)
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF max.
Load Capacitance	18 ± 0.2 pF
Drive Level (Test at 20 nW)	2.5 mW max.
Aging, Per Year	0.0005% (5 ppm)
Oscillation Mode	Fundamental
Series Resistance	25 Ω max.
Maximum Frequency Variation with 16.5 pF or 19.5 pF Load Capacitance	± 0.0035% (35 ppm)

Table 12-4. 24.00014 MHz Oscillator Specifications

Characteristic	Value
Frequency	24.00014 MHz
Frequency Stability	
vs. Temperature	± 5 ppm (0°C - 60°C)
vs. Input Voltage	± 1 ppm (4.75 V - 5.25 V)
vs. Aging	1 ppm/year
Frequency Tolerance	± 2 ppm
Frequency Adjustment by Internal Trimmer	± 5 ppm min.
Operating Temperature	0°C - 60°C
Input Voltage	5.0 V± 0.5% (4.75 V - 5.25 V)
Output	
Symmetry	50% ± 10% (40% - 60%)
Drive	CL = 15 pF
Type	CMOS: Low = 0.5 V, High = Vcc
Package	14-pin DIP

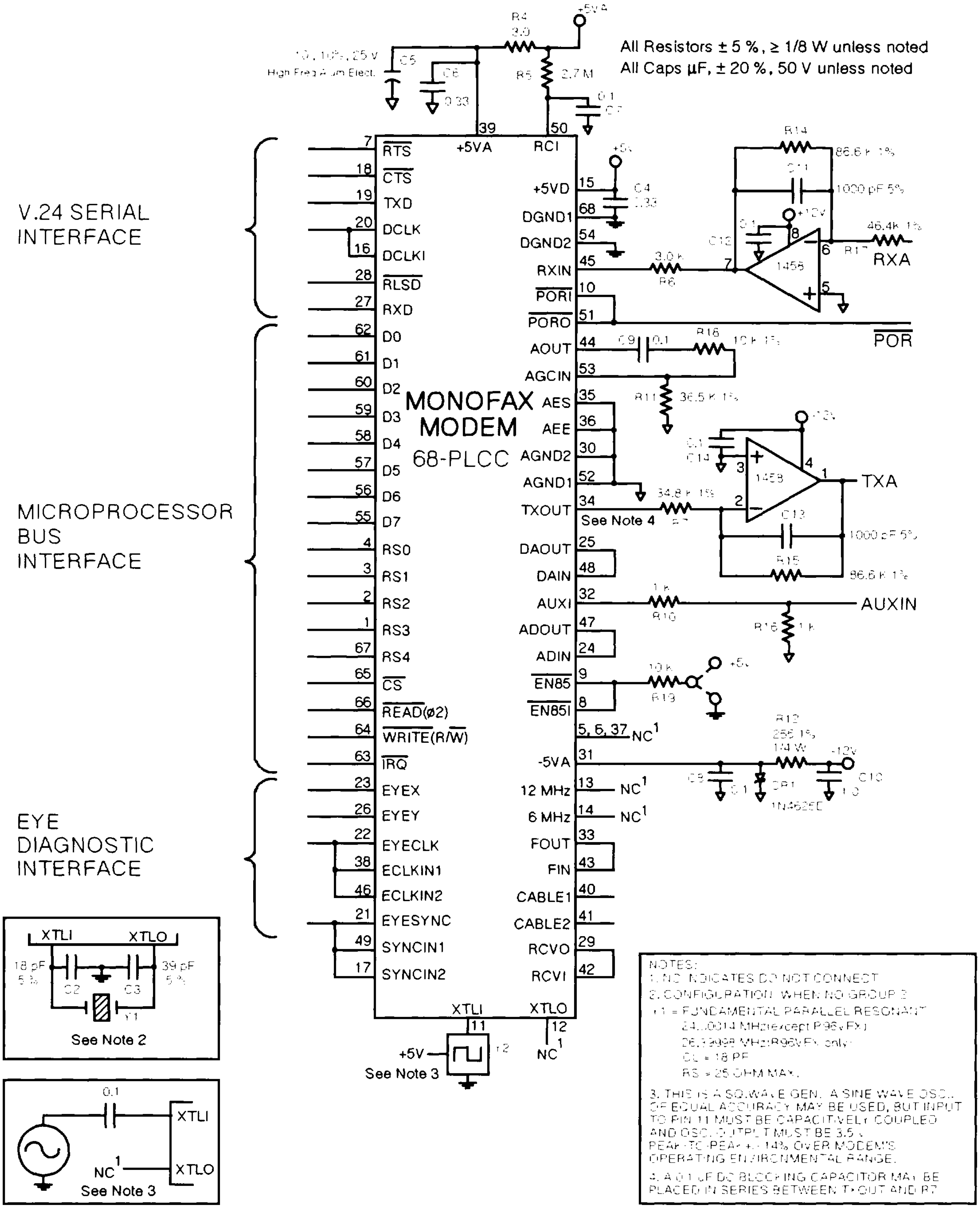


Figure 12-1. Recommended Modem PLCC Interface Circuit

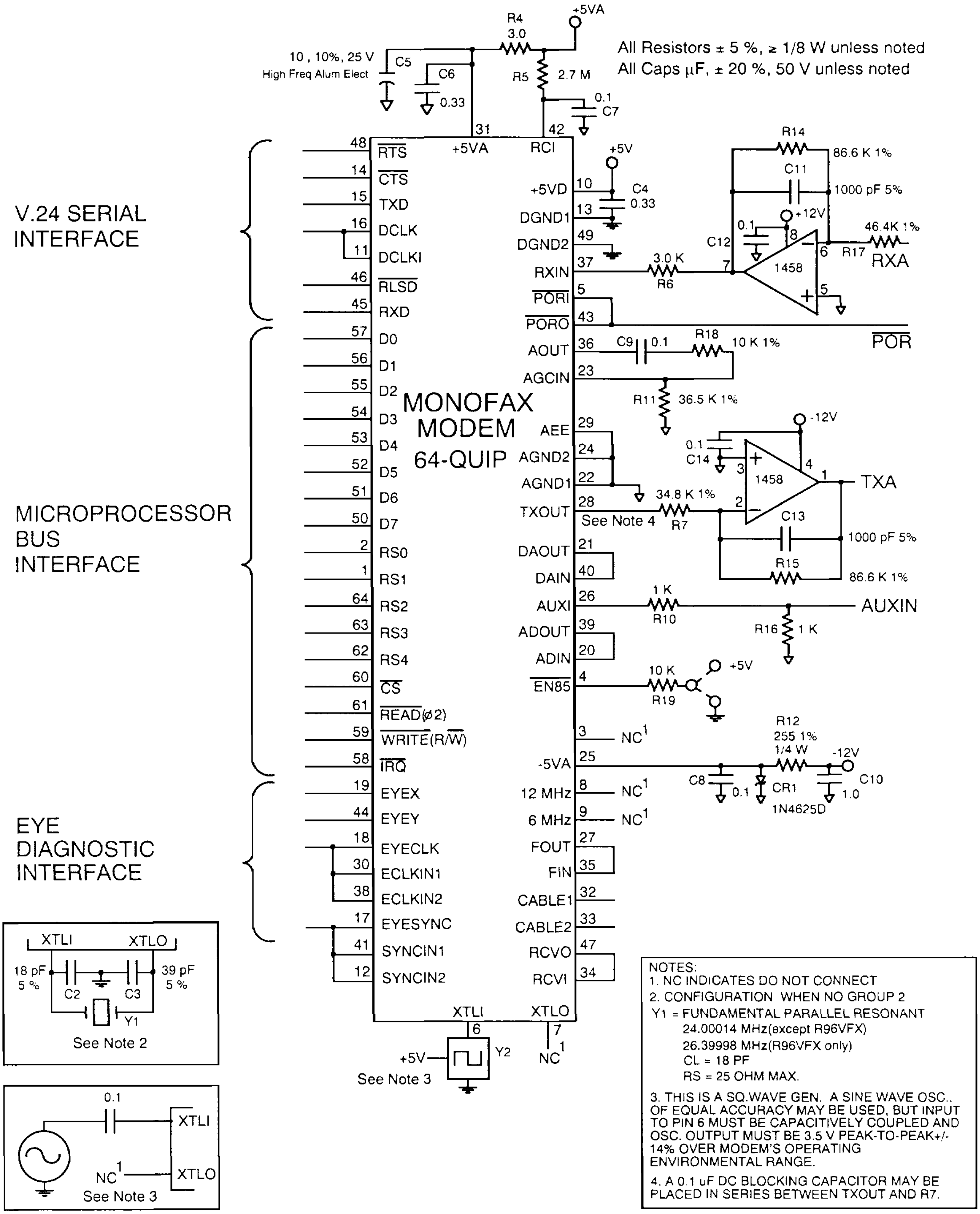


Figure 12-2. Recommended Modem QUIP Interface Circuit

12.2 PC BOARD LAYOUT CONSIDERATIONS

Good engineering practices must be adhered to when designing a printed circuit (PC) board containing a MONOFAX modem. Suppression of noise is essential to the proper operation and performance of the modem itself and for surrounding equipment.

Two aspects of noise in an OEM board design containing a MONOFAX modem must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital (A/D) conversion/digital-to-analog (D/A) conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met to allow use in specific environments.

Proper PC board layout (component placement, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding is required for the board design to achieve desired modem performance and to attain EMI certification.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

General Board Layout Guidelines

The board design should adhere to the following general guidelines. Most of these guidelines are also applicable to minimizing on-board noise EMI generation (see next section).

1. The modem device and all supporting analog circuitry, including the DAA, if required, should be located on the same area of printed circuit board.
2. All power traces should be at least a 0.1 inch width.
3. If the power source is located more than approximately 5 inches from the modem, a decoupling capacitor of 10 μF or greater should be placed in parallel with C4 near the +5VD pin and the DGND2 pin.
4. All circuitry connected to the XTLI and XTLO pins should be kept short to prevent stray capacitance from affecting the oscillator.
5. The AGND1 pin should be tied directly to the AGND2 pin at the modem package. The AGND2 pin should tie directly, by a dedicated path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to the AGND2 pin and to all analog ground points shown in Figures 12-1 and 12-2.
7. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to the DGND2 pin and to all digital ground points shown in Figure 11-1, plus the crystal-can ground.
8. The modem PLCC package should be oriented relative to the two ground planes so that the corner containing pin 9 is toward the digital ground plane and the corner containing pin 43 is toward the analog ground plane. The modem QUIP package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
9. As a general rule, digital signals should be routed on the component side of the PCB while the analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
10. Routing of the modem signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to Tables 12-5 and 12-6 for the noise characteristics of each modem pin.

Electromagnetic Interference (EMI) Considerations

The following guidelines are offered to specifically help minimize EMI generation. Some of these guidelines are redundant or similar to the general guidelines but are mentioned to reinforce their importance.

In order to minimize contribution of MONOFAX modem-based design to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

1. Keep the crystal/oscillator and other related external components as close to the device XTLI and XTLO pins as physically possible.
2. Keep any traces carrying high frequency signals as short as possible.

3. Have a good ground plane. In some cases a multilayer board might be required with full layers for ground and power distribution.
4. Decouple power to ground with decoupling capacitors as close to the device as possible.
5. Eliminate ground loops, which are unexpected current return paths to the power source.
6. Decouple the phone line cables at the telco jacks using series inductors of about 8 μH.
7. Decouple the power cord at the power cord interface with decoupling capacitors.
8. Locate high frequency circuits in a separate area to minimize capacitive coupling to other circuits.
9. Locate cables and connectors to avoid coupling from high frequency circuits.
10. Layout the highest frequency signal traces next to the ground grid.
11. If a multilayer board design is used, the following design rules are recommended:

    A. Make no cuts in the ground or power planes.

    B. The ground plane must cover all traces.

Table 12-4. Modem PLCC Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	High	Low
3	7	5	33	32
4	18	6	40	34
11	19	8	41	
12	20	9	43	
13	27	10	44	
14	28	15	45	
16		29	53	
17		30		
21		31		
22		36		
23		37		
24		39		
25		42		
26		50		
38		51		
46		52		
47		54		
48		63		
49				
55				
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63				
64				

Table 12-5. Modem QUIP Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	High	Low
1	14	3	23	26
2	15	4	27	28
6	16	5	32	
7	45	10	33	
9	46	13	35	
11	48	22	36	
12		24	37	
17		25		
18		29		
19		31		
20		34		
21		42		
30		43		
38		47		
39		49		
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Crystal Oscillator EMI Considerations

A source of EMI radiation in a MONOFAX modem design can be the crystal oscillator circuit which produces fundamental energy at 24.00014 MHz (26.39998 MHz for the R96VFX) and third harmonic energy at 72.00042 MHz (79.19994 MHz for the R96VFX).

The third harmonic energy can easily be reduced by adding some series resistance between the XTLO pin and the load capacitor as illustrated in Figure 12-3. This resistor and the XTLO capacitor create a low pass filter which can attenuate the third harmonic component energy. It is important to note that, although a larger resistor value will further reduce the third harmonic component, it will also attenuate the fundamental frequency and may cause an oscillator circuit start-up problem. A careful selection of this resistor is very important.

12.3 PACKAGE DIMENSIONS

See Figures 12-5 and 12-6.

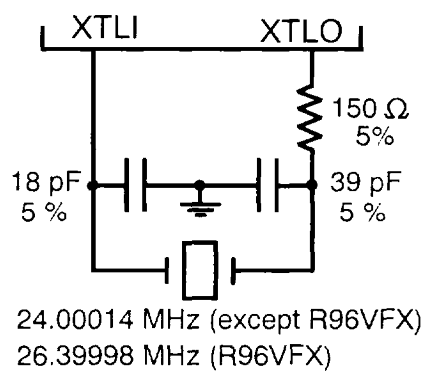
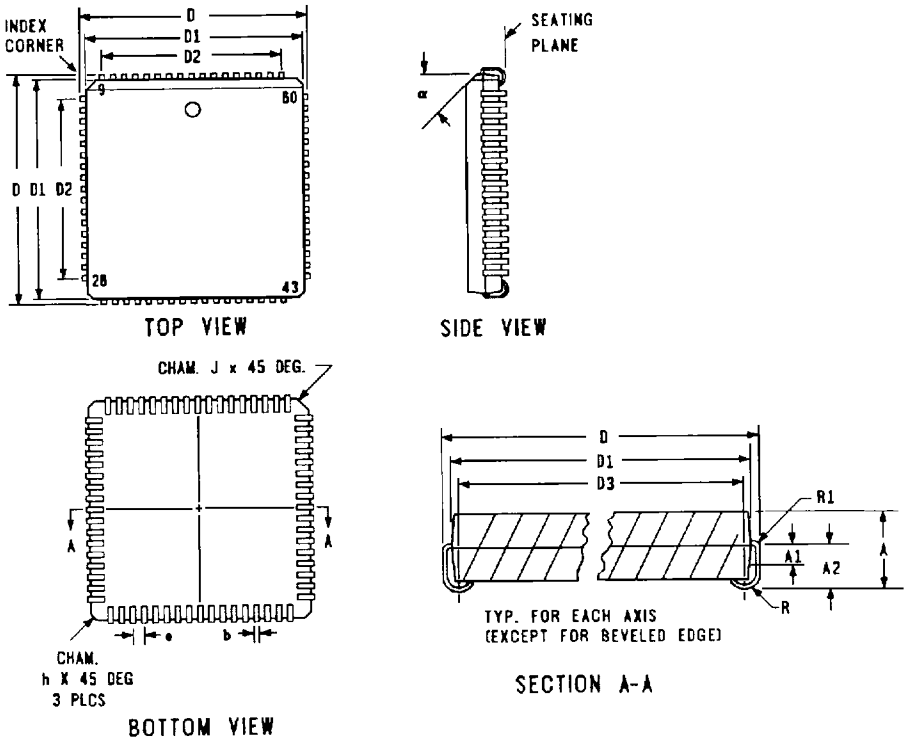
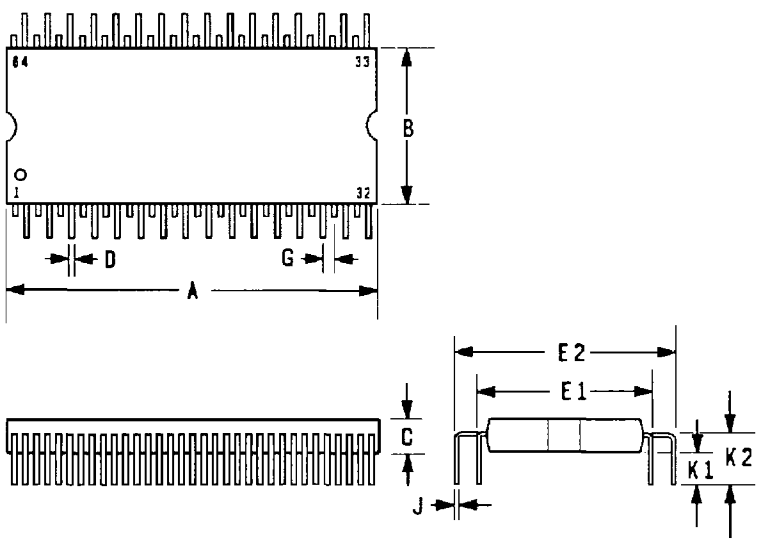


Figure 12-3. Recommended Circuit to Minimize EMI



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		0.018 TYP	
D	25.02	25.27	0.985	0.995
D1	24.00	24.26	0.945	0.955
D2	20.19	20.45	0.795	0.805
D3	23.24	23.50	0.915	0.925
e	1.27 BSC		0.050 BSC	
h	0.254 TYP		0.010 TYP	
J	1.15 TYP		0.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		0.035 TYP	
R1	0.254 TYP		0.010 TYP	
REF: PD68J/GP00-D164				

Figure 12-4. Modem 68-Pin PLCC Dimensions



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	41.10	41.61	1.618	1.638
B	17.02	17.53	0.670	0.690
C	3.56	4.06	0.140	0.160
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	3.25	3.81	0.130	0.150
K2	5.08	5.84	0.200	0.230
REF: PD64Q/GP00-D188				

Figure 12-5. Modem 64-Pin QUIP Dimensions

13 PERFORMANCE

13.1 TYPICAL BIT ERROR RATES

The bit error rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

Typical BER performance is shown in Figure 13-1.

13.2 TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-noise phase jitter at 120 Hz.

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

At 9600 bps (V.29 Short Train), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 5° peak-to-peak phase jitter at 60 Hz.

13.3 DTMF PERFORMANCE

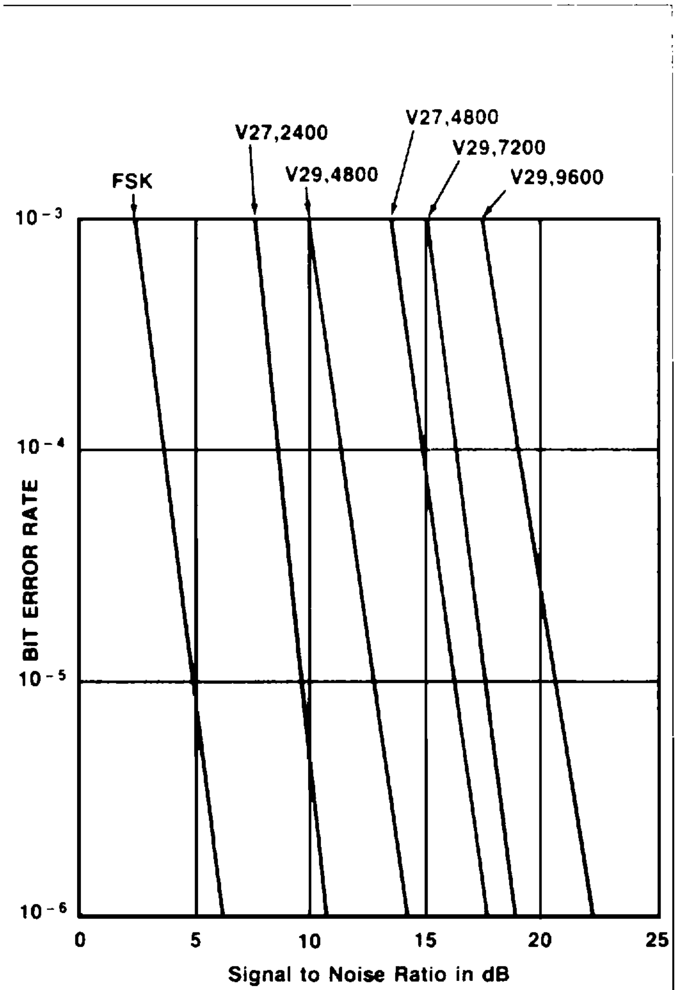
DTMF performance is described in Table 13-1.

Table 13-1. DTMF Receiver Performance Characteristics

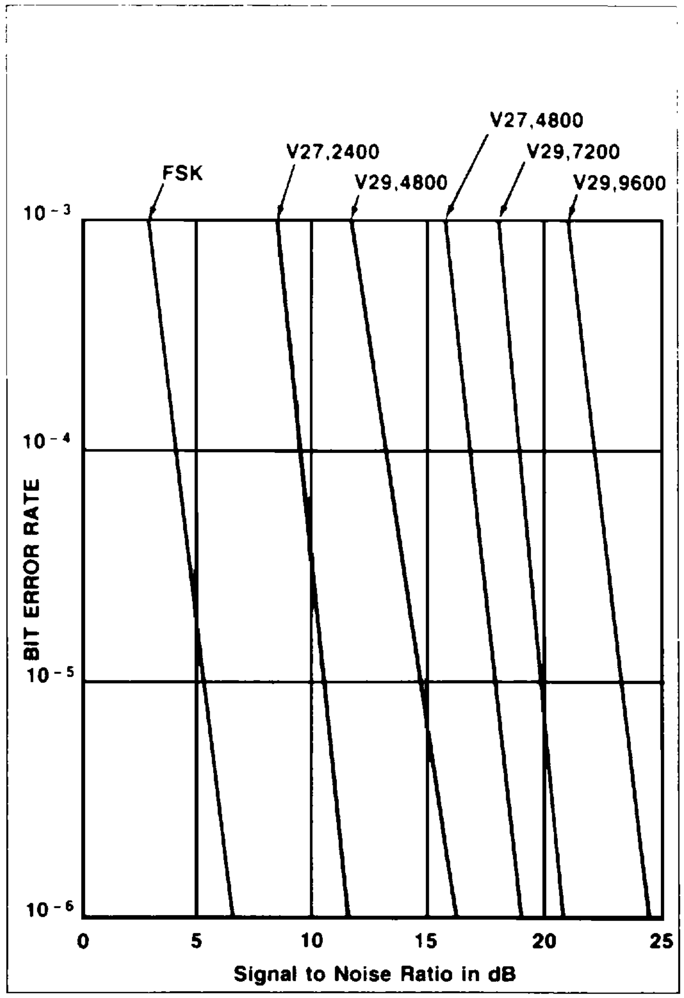
Characteristic	Minimum[12]	Maximum[12]	Units	Programmable?	Notes
Acceptable Twist	–8.2 ±0.2	+4.3 ±0.2	dB	Yes	1, 2, 4, 5, 6, 9
Acceptable Positive Frequency Deviation		+1.5 to +3.2	%	Yes	1, 3, 4, 5, 6, 9
Acceptable Negative Frequency Deviation	–2.1 to –2.8		%	Yes	1, 3, 4, 5, 6, 9
Required On-Time	40.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 9
Required Off-Time	40.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 9
Required Cycle-Time	93.0 ±1.0		ms	Yes	2, 3, 4, 5, 6, 9
Dynamic Range	–43.0	0.0	dBm	Yes	1, 2, 3, 5, 6, 9
Signal-to-Noise Ratio	12.0		dB	No	1, 2, 3, 4, 5, 6, 7, 8, 9
Talk Off	2	3	Hits	Yes	10

Notes:

1. On-time = 50 ms, off-time = 50 ms, and cycle-time = 100 ms.
2. Nominal DTMF frequencies.
3. Both tones of DTMF symbol have equal amplitude, i.e., 0 dB twist.
4. Received signal level = –35.0 dBm.
5. All 16 DTMF symbols transmitted.
6. Error rate of 1/10,000 or less.
7. 3K Hz flat bandwidth limited Gaussian noise.
8. Signal is least amplitude signal of composite DTMF symbol.
9. TAS Telephone Network Simulator Model #112, flat line transmission path.
10. Mitel CM7291 DTMF Receiver Test Cassette.
11. All DTMF receiver parameters are equal to their default values.
12. Values shown are for DTMF Receiver (configuration code 21h).



Typical Bit Error Rate
(Back-to-Back, T Equalizer, Level −20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer Level −20 dBm)

Figure 13-1. Modem Typical Error Rate (BER) Curves