Signetics

FAST 74F1761
DRAM and Interrupt Vector Controller

Preliminary Specification

FAST Products

FEATURES

- **Programmable DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Provides byte selection for 16- and 32-bit buses**
- **Interrupt Priority Encoder included**
- **Interrupt Acknowledge vector generator on-chip**

DESCRIPTION

The Signetics DRAM and Interrupt Vector Controller (DIVC) is a high-performance bipolar device designed to reduce board space and improve performance in microprocessor-based systems. The DIVC's functions include a DRAM signal interface with user programmable timing to match the performance of specific DRAMs used in a system. With a maximum clock frequency of 100MHz, this means a timing resolution of 10ns. The DRAM Controller section also includes automatic refresh arbitration, with the duration and frequency of refresh totally programmable by the user. When used with the 74F1762 Memory Address Controller, the DIVC provides a complete system solution for DRAM and Interrupt Control. For Interrupt Control, the DIVC contains an Interrupt Priority Decoder with latched inputs controlled by the Interrupt Latch Enable (ILE) input. In addition, the DIVC contains an Interrupt Acknowledge Controller which passes a programmable 8-bit vector on the system data bus upon receipt of an interrupt acknowledge. There are 7 interrupt acknowledge vectors; each accessible by placing the priority number of the Interrupt Acknowledge on the A1 – A3 signal inputs while acknowledging an interrupt.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1761	100MHz	200mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V± 10%; T_A = 0°C to 70°C
Plastic DIP	N74F1761N
PLCC 44	N74F1761A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM request input	1.0/1.0	20μA/0.6mA
SIZ0/$\overline{LDS}$, SIZ1, A0/$\overline{UDS}$, A1	Byte Select inputs	1.0/1.0	20μA/0.6mA
A2, A3	Register Select inputs	1.0/1.0	20μA/0.6mA
$\overline{CS}$, $\overline{DS}$	Chip Select, Data Strobe	1.0/1.0	20μA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20μA/0.6mA
$\overline{INTACK}$	Interrupt Acknowledge input	1.0/1.0	20μA/0.6mA
ILE	Interrupt Latch Enable input	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input	1.0/1.0	20μA/0.6mA
$\overline{INTRQ1-7}$	Interrupt Request inputs	1.0/1.0	20μA/0.6mA
$\overline{DTACK}$	Data Transfer Acknowledge output	(OC)/80	24mA
D0 – D7	Data Bus	50/80 (1.0/1.0)	1.0mA/24mA
$\overline{IPL0-2}$	Interrupt Priority outputs	50/80	1.0mA/24mA
$\overline{RAS}$, MUX, $\overline{REFEN}$, $\overline{CAS0-3}$	DRAM Control outputs	1750/100	35mA/60mA

NOTE:
1. One (1.0) FAST Unit Load is defined as 20μA in the High state and 0.6mA in the Low state. O.C. = Open-Collector

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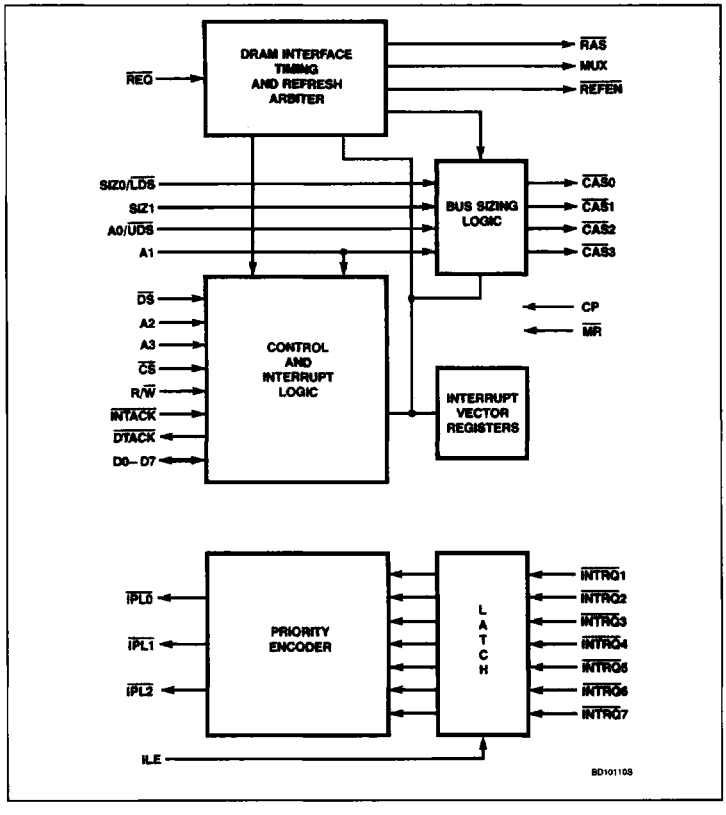
DRAM and Interrupt Vector Controller FAST 74F1761

BLOCK DIAGRAM



PIN CONFIGURATION