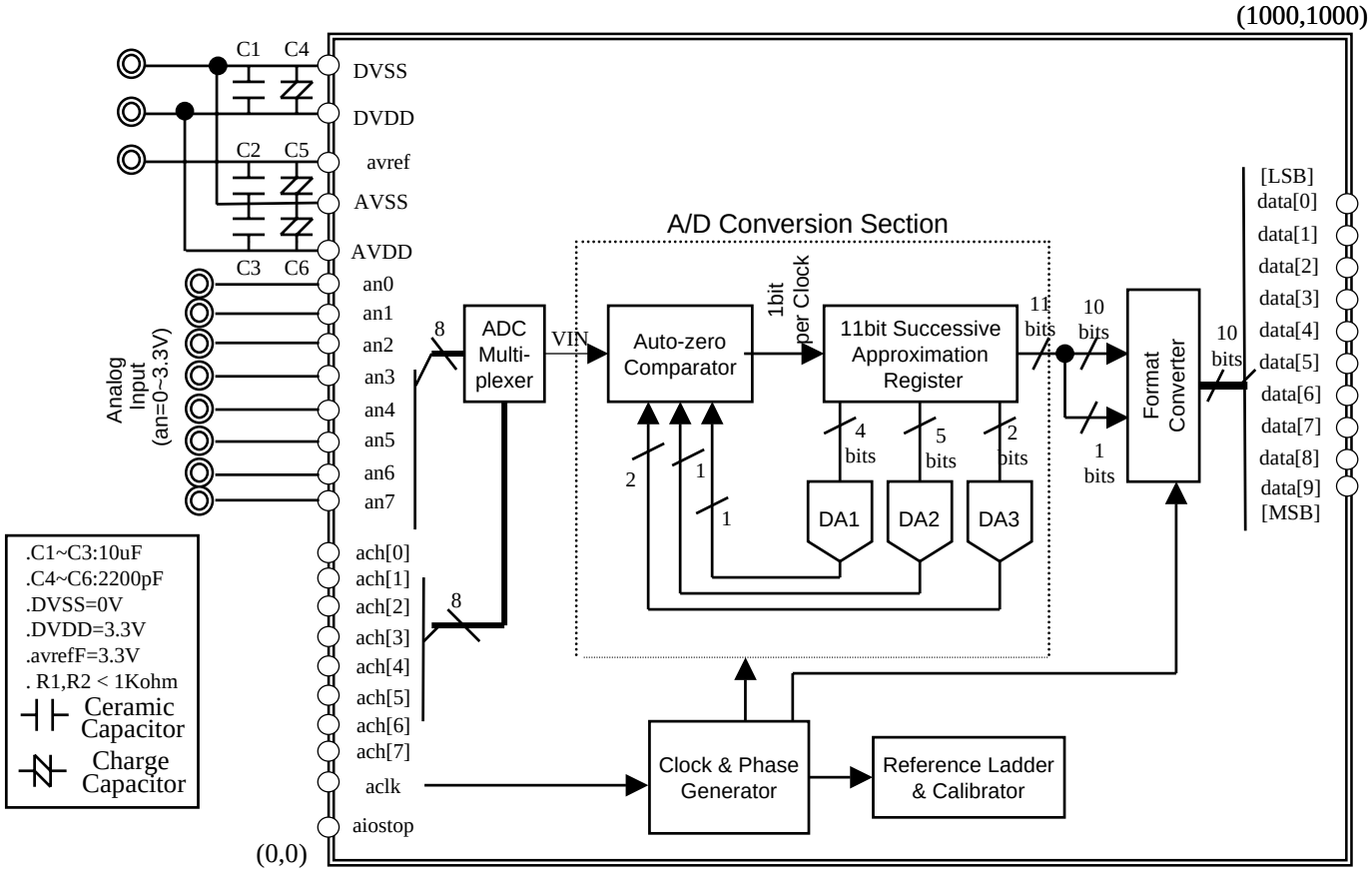
1. General Description

H35AD32S is a 10-bit CMOS(0.35㎛, 1-poly, 3-metal) successive -approximation analog-to-digital converter which has high speed, low power consumption.
The ADC has multiplexed 8 input channels.
The serial output is configured to interface with standard shift registers. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. The voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 10bits of resolution

2. Features

- Power supply : 3.3v
- Resolution:10 bits
- Signal-to-noise ratio(SNR) : 54dB
- 8 channels
- Conversion speed : 500KHz (@ 8Mhz)
- Main clock : 8 MHz
- Power-down mode
- Analog input range : AVSS~ avref
- Cell Size :1000 ㎛ x 1000 ㎛

3. Block Diagram with Recommended Application Circuit



4. Pin Descriptions

Name	Type	Description
avref	Input	Analog Reference
AVSS	Ground	Analog Ground
AVDD	Power	Analog Power
an0	Input	Analog input0
an1	Input	Analog input1
an2	Input	Analog input2
an3	Input	Analog input3
an4	Input	Analog input4
an5	Input	Analog input5
an6	Input	Analog input6
an7	Input	Analog input7
ach[0]	Input	Select Channel [0]
ach[1]	Input	Select Channel [1]
ach[2]	Input	Select Channel [2]
ach[3]	Input	Select Channel [3]
ach[4]	Input	Select Channel [4]
ach[5]	Input	Select Channel [5]
ach[6]	Input	Select Channel [6]
ach[7]	Input	Select Channel [7]
aclk	Input	Clock
aiostop	Input	Power save
data[9]	Output	Digital Output [9]
data[8]	Output	Digital Output [8]
data[7]	Output	Digital Output [7]
data[6]	Output	Digital Output [6]
data[5]	Output	Digital Output [5]
data[4]	Output	Digital Output [4]
data[3]	Output	Digital Output [3]
data[2]	Output	Digital Output [2]
data[1]	Output	Digital Output [1]
data[0]	Output	Digital Output [0]
DVDD	Power	Digital Power
DVSS	Ground	Digital Ground

5. Function Descriptions

This SAR-type ADC contains a SAR register, an auto-zero comparator, three internal DACs, a mux(8x1), a format converter, a clock & phase generator, and a reference ladder & calibrator. The conversion rate ranges up to 1MHz.
These blocks contained in ADC can be described as follows:

5.1 SAR register

This block is a successive approximation register which latches the output of comparator and generates the input of the internal DACs.

5.2 Auto-zero comparator

This comparator is able to reduce the offset error periodically and senses the difference between analog input and DAC's output.

5.3 Internal DACs

These DACs generate analog reference voltage according to SAR register output.

5.4 Multiplexer

One of the eight channel can be selected by the control pins (ach[0] ~ ach[7])

5.5 Format converter

This format converter is to latch the 11-bit SAR output data stream and convert it to a standard 10-bit binary format.

5.6 Clock & Phase generator

The outputs generated in clock & phase generator control SAR-type ADC conversion operation.

5.7 Reference ladder & calibrator

This reference ladder generates the analog reference voltage used by the internal DACs.
The reference ladder taps are adjusted by using an auto-calibration technique.

Normal operation

. aiostop : low
. an0~an7 ≤ avref ≤ AVDD
. aclk : 2MHz ~ 16MHz
. an0 ~ an7 : AVSS~ avref
. Analog input selection

Pin(High)	ach[0]	ach[1]	ach[2]	ach[3]	ach[4]	ach[5]	ach[6]	ach[7]
Channel	an0	an1	an2	an3	an4	an5	an6	an7

Power down operation

. aiostop : high

6. Operating Conditions

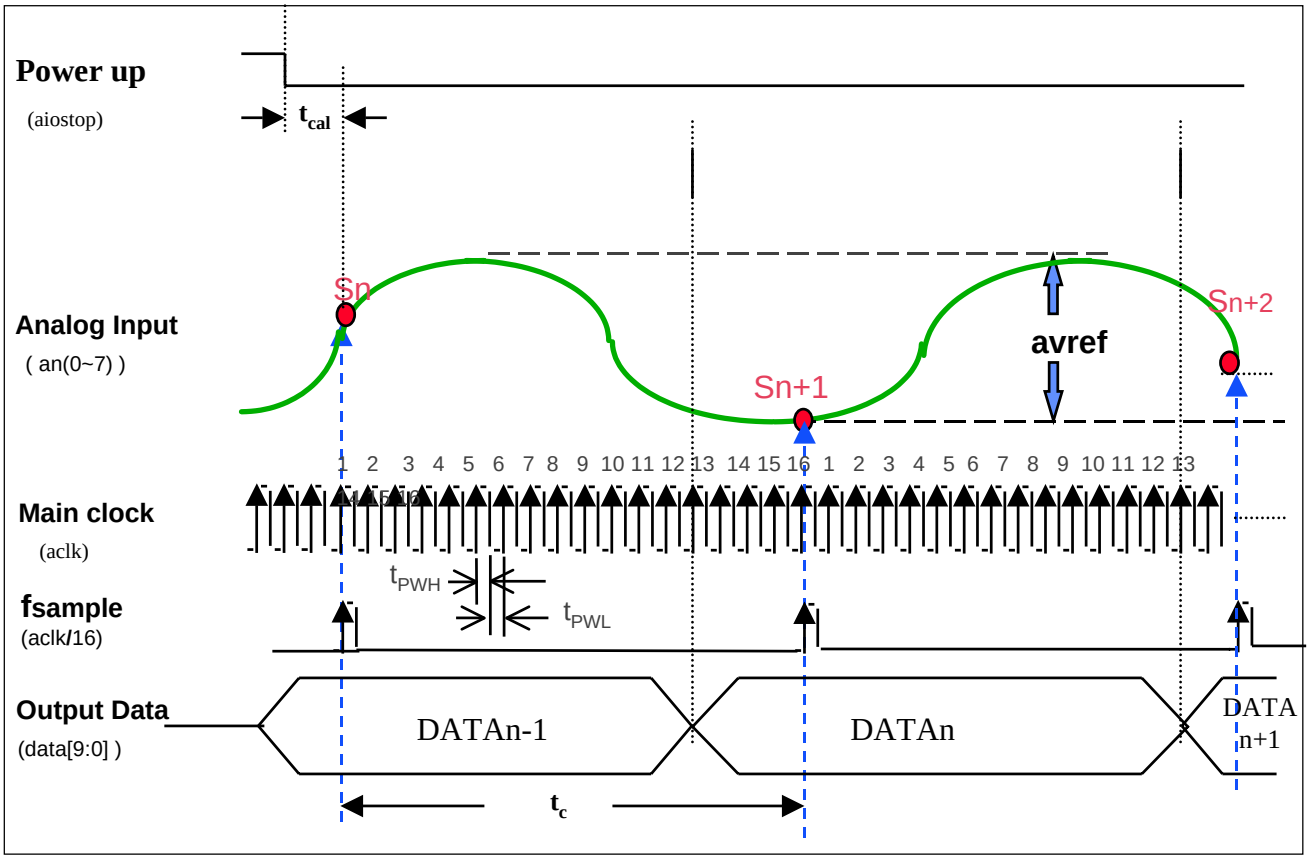
Symbol	Parameter	Min.	Max.	Units
AVDD	Power Supply	3.0	3.6	V
DVDD		3.0	3.6	V
an	Analog Input	AV SS	avref	V
T_{PWL}	Clock pulse width (@8MHz)	62.5		ns
T_{PWH}		62.5		ns
Top	Operation Temperature	0	100	℃

7. Electrical Characteristics

(Analog input frequency Fin=2Khz,aclk =8 Mhz, AVDD=DVDD=avref=3.3V T= 25 ℃)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{dd}	Normal	aclk=8MHz Input=avref Fin=2kHz ramp		4.0		mA
	Power down	aclk=8MHz			40	uA
an	Analog input voltage		AVSS		avref	V
Accuracy	Resolution				10	bits
INL	Integral Nonlinerity	aclk = 8MHz Input =0-avref(V) (Fin = 2kHz ramp)			±2.0	LSB
DNL	Differential Nonlinerity	aclk = 8MHz Input = 0 -avref(V) (Fin = 2kHz ramp)			±1.0	LSB
SNR	Signal-to-Noise Ratio	Fsample=500ksps, Fin =2KHz	50	54		dB
SNDR	Signal-to-Noise Distortion Ratio		48	52		dB
aclk			2	8	16	MHz
t_c	Conversion time		1	4	8	us
avref	Analog Reference Voltage				AVDD	V
tcal	Power up time	Calibration time		16		ms
THD	Total harmonic distortion		50	54		dB
AVDD	Analog power		3.0	3.3	3.6	V
DVDD	Digital power		3.0	3.3	3.6	V
Fin	Analog input frequency				60	Khz

8. Timing Diagram



9. Layout Guide

Power Supply De-coupling

The analog power and the digital power of the H35AD32S should be separated from each other to prevent the glitch which is coupled into the analog power from digital circuitry. The I/O powers are also separated as shown in figure 1. Digital power can be connected to main chip digital power.

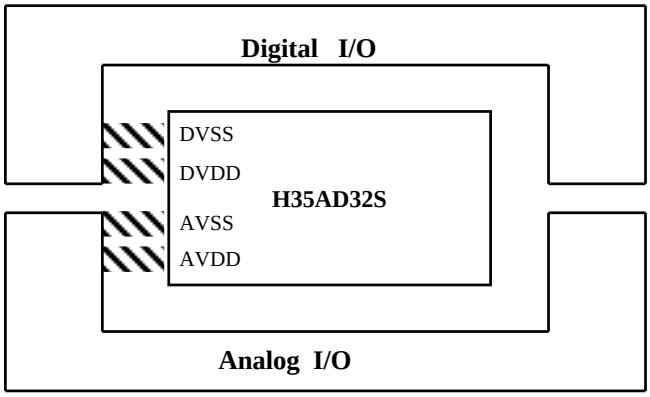


Figure 1. Recommended power scheme

Analog pad

The PC3D00 can be used as an analog I/O pad.

Analog signals

The analog signals, such as an[0]~an[7],avref must be drawn wider than connector width from ADC core to pad because of large current flow.

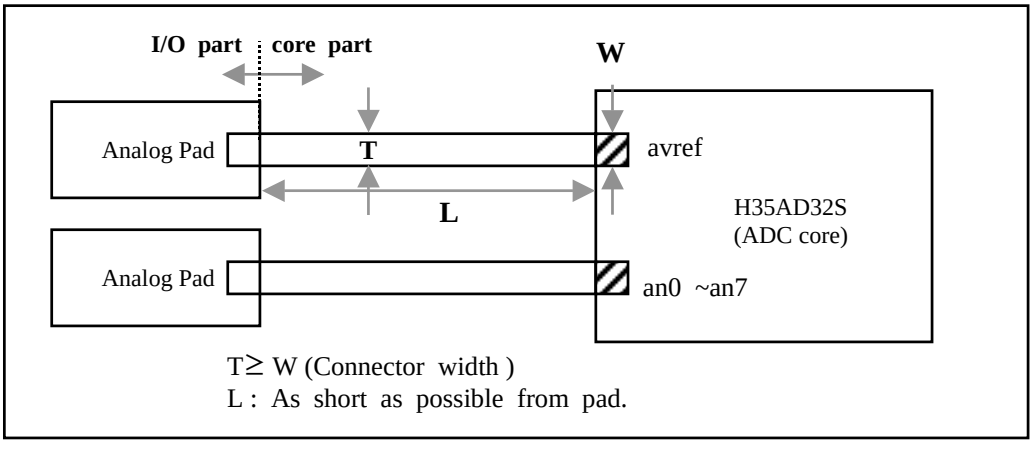


Figure 2. Analog pads connection

Analog pad routing

-avref, an[0]~an[7]: Using AVDD, AVSS

-data[0:9], aiostop, aclk, ach[0]~ach[7]: Using DVDD, DVSS

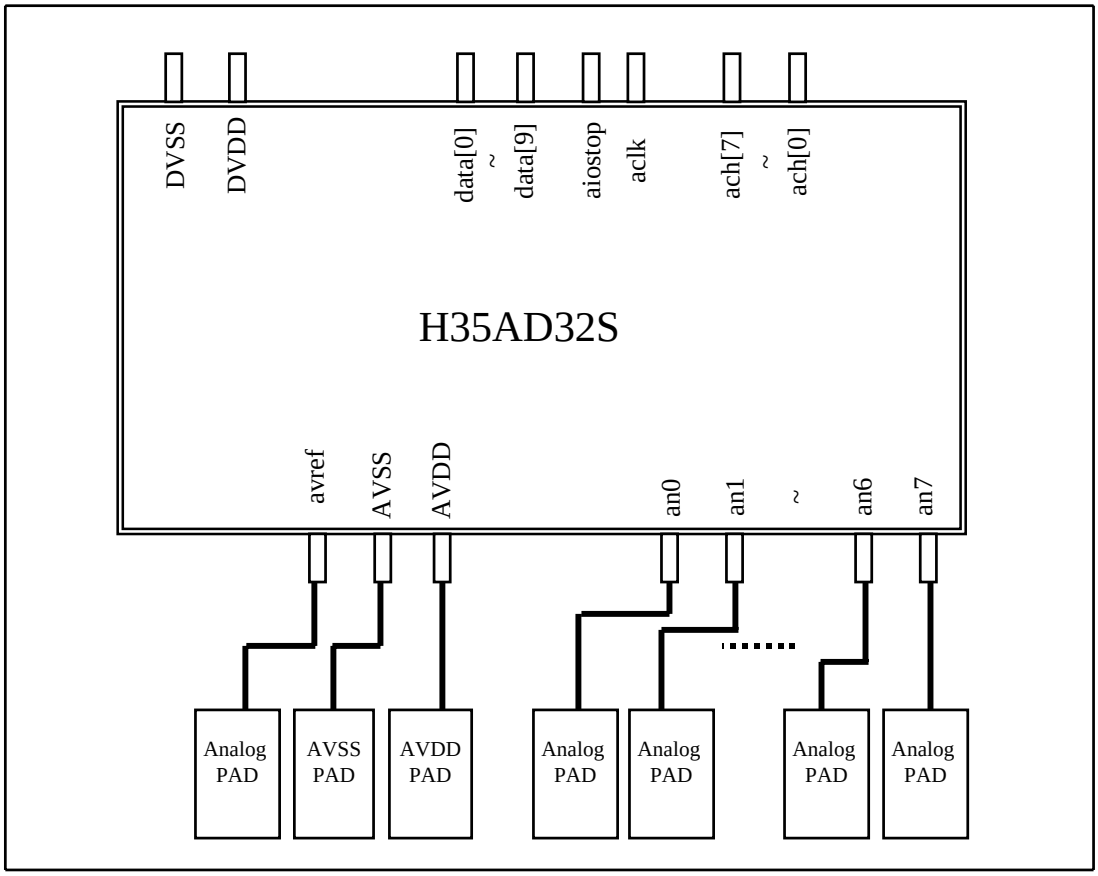


Figure 3. Analog power routing