FEATURES

- **Low V_{OS} (V_{BE} Match) ..... 40μV Typ**
  100μV Max
- **Low TCV_{OS} ..... 0.5μV/° C Max**
- **High h_{FE} ..... 500 Min**
- **Excellent h_{FE} Linearity from 10nA to 10mA**
- **Low Noise Voltage ..... 0.23μV_{p-p} — 0.1Hz to 10Hz**
- **High Breakdown ..... 45V Min**
- **Available in Die Form**

ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
0.1	MAT01AH*	MIL
0.5	MAT01GH	MIL

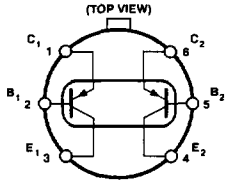
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

The MAT-01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40μV, temperature drift of 0.15μV/° C, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10nA. The high gain at low collector current makes the MAT-01 ideal for use in low-power, low-level input stages.

PIN CONNECTIONS



TO-78
(H-Suffix)

NOTE:
Substrate is connected to the case.

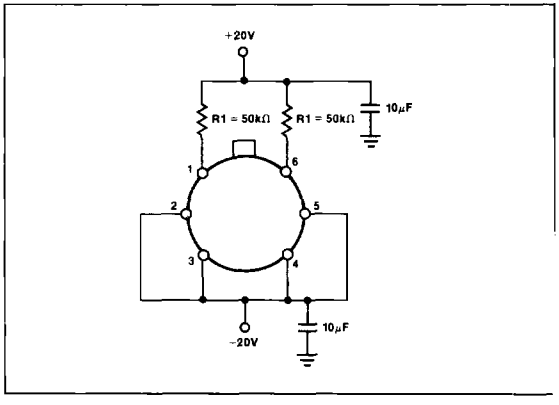
ABSOLUTE MAXIMUM RATINGS (Note 4)

Collector-Base Voltage (BV_{CBO})
MAT-01AH, GH, N 45V
Collector-Emitter Voltage (BV_{CEO})
MAT-01AH, GH, N 45V
Collector-Collector Voltage (BV_{CC})
MAT-01AH, GH, N 45V
Emitter-Emitter Voltage (BV_{EE})
MAT-01AH, GH, N 45V
Emitter-Base Voltage (BV_{EBO}) (Note 1) 5V
Collector Current (I_C) 25mA
Emitter Current (I_E) 25mA
Total Power Dissipation
Case Temperature ≤ 40° C (Note 2) 1.8W
Ambient Temperature ≤ 70° C (Note 3) 500mW
Operating Ambient Temperature ..... −55° C to +125° C
Operating Junction Temperature ..... −55° C to +150° C
Storage Temperature ..... −65° C to +150° C
Lead Temperature (Soldering, 60 sec) ..... 300° C
DICE Junction Temperature ..... −65° C to +150° C

NOTES:

1. Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.
2. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/° C for case temperatures above 40° C.
3. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/° C for ambient temperatures above 70° C.
4. Absolute maximum ratings apply to both DICE and packaged devices.

BURN-IN CIRCUIT



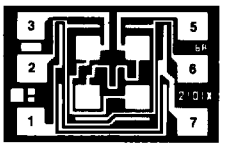
ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH MIN	MAT-01AH TYP	MAT-01AH MAX	MAT-01GH MIN	MAT-01GH TYP	MAT-01GH MAX	UNITS
Breakdown Voltage	BV_{CEO}	I_C = 100μA	45	—	—	45	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	μV/Mo
Long-Term		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.6	—	0.2	3.2	nA
Bias Current	I_B		—	13	20	—	18	40	nA
Current Gain	h_{FE}	I_C = 10nA	—	590	—	—	430	—	
		I_C = 10μA	500	770	—	250	560	—	
		I_C = 10mA	—	840	—	—	610	—	
Current Gain Match	Δh_{FE}	I_C = 10μA	—	0.7	3.0	—	1.0	8.0	%
		100nA ≤ I_C ≤ 10mA	—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	μV_{p-p}
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	7.0	9.0	—	7.0	9.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	6.1	7.6	—	6.1	7.6	
		f_O = 1000Hz (Note 3)	—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	—	0.5	3.0	—	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	—	2	15	—	3	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0 (Note 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0 (Notes 4, 6)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 30V, (Note 6)	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	—	0.12	0.20	—	0.12	0.25	V
		I_B = 1mA, I_C = 10mA	—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	V_{CB} = 15V, I_E = 0	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	—	8.5	—	—	8.5	—	pF

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH MIN	MAT-01AH TYP	MAT-01AH MAX	MAT-01GH MIN	MAT-01GH TYP	MAT-01GH MAX	UNITS
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 7)	—	0.15	0.50	—	0.35	1.8	μV/°C
Offset Current	I_{OS}		—	0.9	8.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	10	90	—	15	150	pA/°C
Bias Current	I_B		—	28	60	—	36	130	nA
Current Gain	h_{FE}		167	400	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 30V, I_E = 0 (Note 4)	—	15	80	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 30V, V_{BE} = 0 (Notes 4, 6)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 30V (Note 6)	—	30	200	—	50	400	nA

DICE CHARACTERISTICS



1. COLLECTOR (1)
2. BASE (1)
3. EMITTER (1)
5. EMITTER (2)
6. BASE (2)
7. COLLECTOR (2)

DIE SIZE 0.035 × 0.025 inch, 875 sq. mils
(0.89 × 0.64 mm, 0.58 sq. mm)

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at V_{CB} = 15V and I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}	I_C = 100μA	45	V MIN
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Current	I_{OS}		3.2	nA MAX
Bias Current	I_B		40	nA MAX
Current Gain	h_{FE}		250	MIN
Current Gain Match	Δh_{FE}		8.0	% MAX
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	8.0	μV/V MAX
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	70	pA/V MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	0.25	V MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in asembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

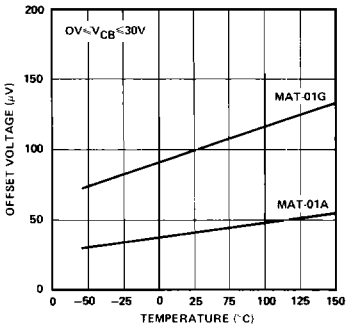
TYPICAL ELECTRICAL CHARACTERISTICS at V_{CB} = 15V and I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}		0.35	μV/°C
Average Offset Current Drift	TCI_{OS}		15	pA/°C
Collector-Emitter-Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0	90	pA
Collector-Base-Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0	25	pA
Gain Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	450	MHz
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1) Long-Term (Note 2)	2.0 0.2	μV/Mo

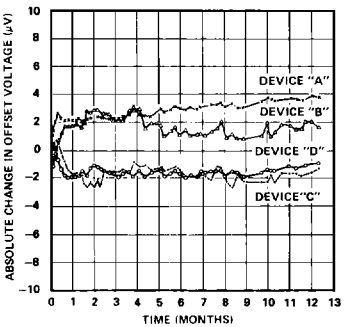
NOTES:
1. Exclude first hour of operation to allow for stabilization.
2. Parameter describes long-term average drift after first month of operation.
3. Sample tested.
4. The collector-base (I_{CBO}) and collector-emitter (I_{CES}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.
5. Guaranteed by I_{OS} test limits over temperature.
6. I_{CC} and I_{CES} are guaranteed by measurement of I_{CBO}.
7. Guaranteed by V_{OS} test ($TCV_{OS} \approx \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$, T = 298°K for T_A = 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

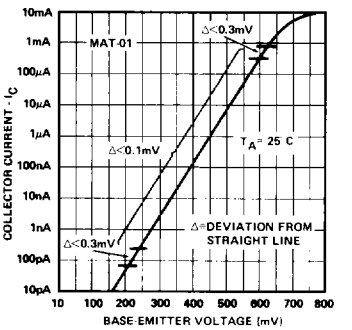
OFFSET VOLTAGE vs TEMPERATURE



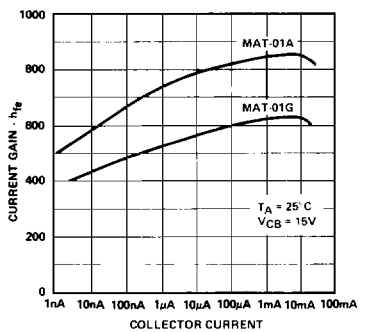
OFFSET VOLTAGE vs TIME



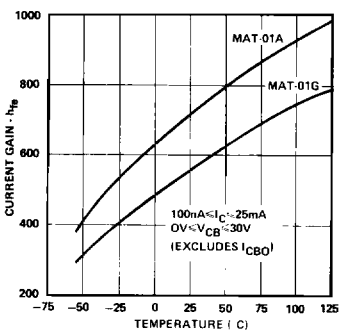
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



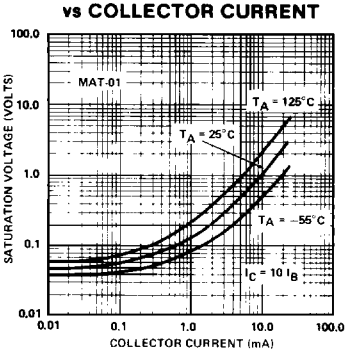
CURRENT GAIN vs COLLECTOR CURRENT



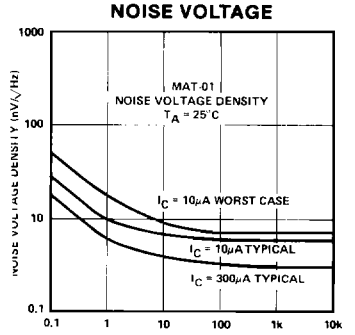
CURRENT GAIN vs TEMPERATURE



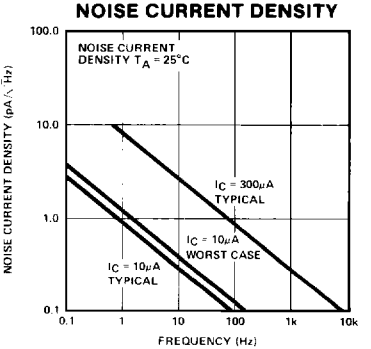
SATURATION VOLTAGE vs COLLECTOR CURRENT



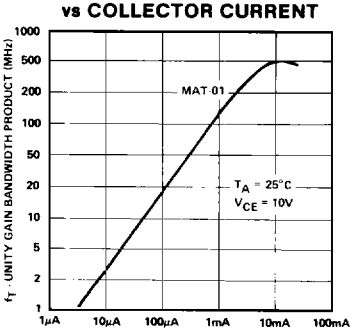
NOISE VOLTAGE



NOISE CURRENT DENSITY



GAIN-BANDWIDTH vs COLLECTOR CURRENT

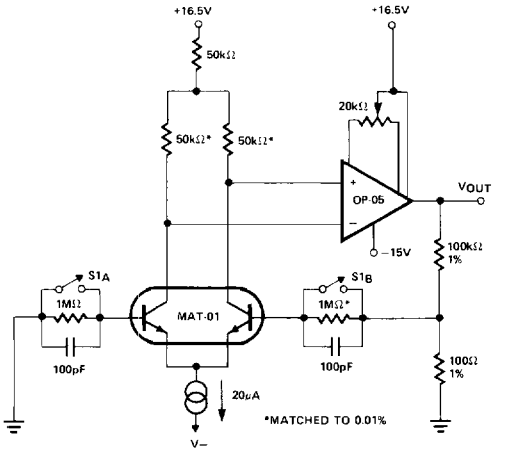


C

MATCHED TRANSISTORS

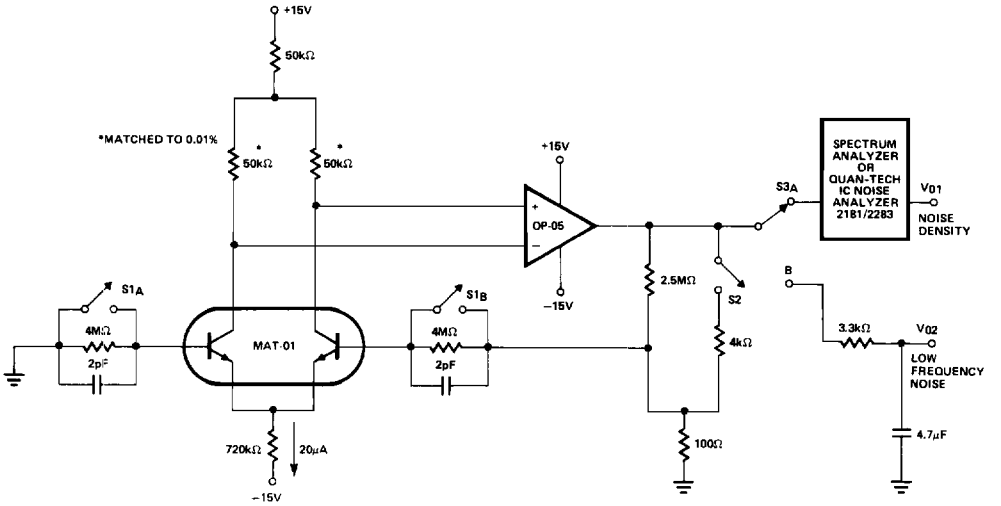
MAT-01 TEST CIRCUITS

MAT-01 MATCHING MEASUREMENT CIRCUIT



TEST	SI_A	SI_B	UNITS	
V_{OS}	X	X	V_{OUT_1}	1 volt per mV
I_{OS}	O	O	$V_{OUT_2} - V_{OUT_1}$	1 volt per nA

MAT-01 NOISE MEASUREMENT CIRCUIT



TEST	SI_A	SI_B	S_2	S_3	READING
Noise Voltage Density (Per Transistor)	X	X	X	A	$V_{O1}/\sqrt{2}$
Noise Current Density (Per Transistor)	O	O	X	A	$V_{O1}/(\sqrt{2} \times 4M\Omega)$
Low Frequency Noise (Referred to Input)	X	X	O	B	$\frac{V_{O2}\ \text{PEAK-TO-PEAK}}{25{,}000}$

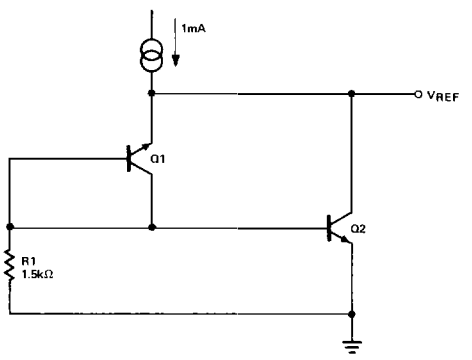
APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Circuit designs should be checked to ensure that reverse bias voltages above 5V cannot be applied during such transient conditions as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Both input terminals should be maintained at the same temperature, preferably close to the temperature of the device's package.

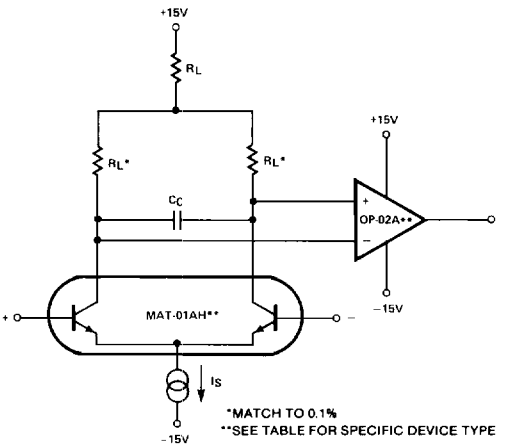
TYPICAL APPLICATIONS

PRECISION REFERENCE



$V_{REF} \approx 7.0V$
$TCV_{REF} \approx 10ppm/°C$
$R_O \approx 40\Omega$
R_1 MAY BE ADJUSTED TO MINIMIZE TCV_{REF}. INCREASING R_1 WILL CAUSE A POSITIVE CHANGE IN TCV_{REF}.
NOTE: h_{FE} OF Q1 WILL BE REDUCED BY OPERATION OF BREAKDOWN MODE.

PRECISION OPERATIONAL AMPLIFIERS

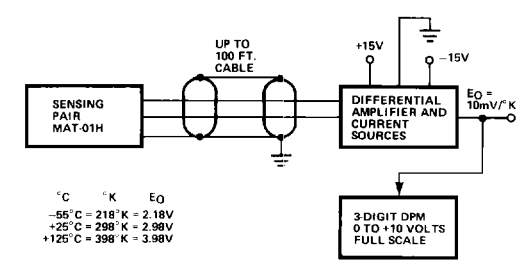


*MATCH TO 0.1%
**SEE TABLE FOR SPECIFIC DEVICE TYPE

THIS CONFIGURATION CAN ALSO BE USED WITH THE LOW POWER OP-21 OR MICROPOWER OP-22 TO ACHIEVE A LOW NOISE AND LOW POWER PRECISION OP-AMP.

	MAT-01AH OP-02A	MAT-01AH OP-02A	MAT-01GH OP-02	MAT-01GH OP-02
V_{OS} Maximum	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{OS} Maximum	0.6μV/°C	1μV/°C	2μV/°C	4μV/°C
I_{OS} Maximum	0.8nA	0.1nA	3.2nA	0.32nA
I_B Maximum	20nA	2nA	40nA	4nA
Gain Minimum	2,000,000	2,000,000	800,000	800,000
I_S	20μA	2μA	20μA	2μA
R_L	100kΩ	1MΩ	100kΩ	1MΩ

BASIC DIGITAL THERMOMETER READOUT IN DEGREES KELVIN (°K)



DIGITAL THERMOMETER WITH READOUT IN °C