VTC Inc.
Value the Customer™

VM5621/VM5622

(2,7) ENCODER-DECODER

August,1994

FEATURES

- Encodes and Decodes IBM (2,7) Code
- 48 Mbits/sec Maximum Code Rate
- Soft-Sector 2T Frequency Address Mark Generation
- Preamble Lock Time = 64 • T (T = one period of 2F clock)
- 4T (1000...) Preamble Frequency Detection
- Two Supply Options:
  VM5622: ±5V Supplies, TTL Above Ground and Differential ECL Below Ground
  VM5621: +5V Supply Only, TTL and ECL Run Above Ground
- VM5621 is Compatible With the VM5351/VM5352
- The VM5621 has a Power Dissipation of 405mW Typca
- The VM5622 has a Power Dissipation of 505mW Typical
- Differential ECL Drivers and Receivers for Clock and Data Interface Lines
- Available in a 28-lead PLCC Package

DESCRIPTION

The (2,7) Encoder/Decoder (ENDEC) performs the encoding and decoding necessary to use the (2,7,1,2,4) Run-Length Limited (RLL) code for disk drive memory systems.

The ENDEC also performs many other functions such as writing of an address mark for soft sectored disk formats, and the reading of a preamble pattern (PLL sync field) that is compatible with the (2,7) RLL code. The ENDEC is fabricated using a high-speed ECL 2.5 bipolar process.

ABSOLUTE MAXIMUM RATINGS

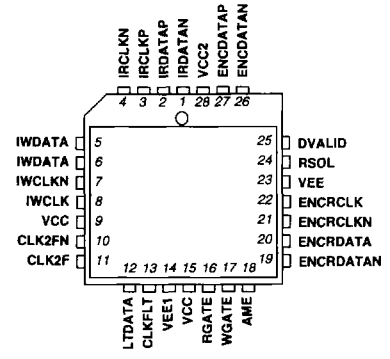
VM5621

Power Supply Voltages
(V_{EE} = 0V) ..... 0V to 7V
Storage Temperature Range ..... -55° to +150°C
Ambient Temperature Range ..... 0° to +70°C
Voltage Applied to TTL Inputs (V_{EE} = 0V) ..... V_{CC} + 0.5V
Voltage Applied to ECL Inputs (V_{EE} = 0V) ..... 0V to V_{CC}
Maximum Power Dissipation 515mW
Junction Temperature ..... 150°C
Thermal Impedance, Θ_{JA}
28-lead PLCC ..... 53°C/W

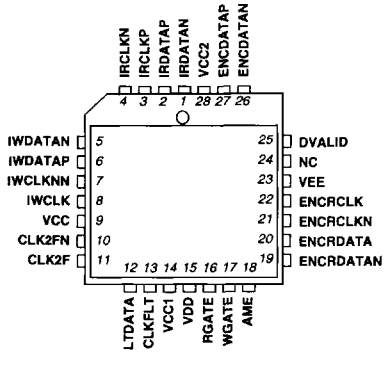
VM5622

Power Supply Voltages
V_{DD} (V_{CC} = 0V) ..... 0V to 7V
V_{EE} (V_{CC} = 0V) ..... 0V to -5.72V
Storage Temperature Range ..... -55° to +150°C
Ambient Temperature Range ..... 0° to +70°C
Voltage Applied to TTL Inputs (V_{CC} = 0V) -0.5V to V_{DD} +0.5V
Voltage Applied to ECL Inputs (V_{CC} = 0V) ..... 0V to V_{EE}
Maximum Power Dissipation 630mW
Junction Temperature ..... 150°C
Thermal Impedance, Θ_{JA}
28-lead PLCC ..... 53°C/W

CONNECTION DIAGRAMS



28-lead PLCC (1 supply)



28-lead PLCC (2 supply)

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
V_{EE} ..... -4.5V to -5.72V
V_{CC}, V_{DD} ..... 4.5V to 5.5V
Ambient Operating Temperature ..... 0° to 70°C
Operating Junction Temperature ..... 0° to 130°C
Data Rate ..... 10 to 48Mbits/sec

DATA RECOVERY CIRCUITS

PIN DESCRIPTIONS

INPUT SIGNALS:

ENCODED READ DATA (ENCRDATA) (differential ECL): This is the encoded data output of the data separator circuit. It is synchronized with the ENCODED READ CLOCK. The positive edge of the ENCODED READ CLOCK signal is used to strobe the ENCODED READ DATA into the (2,7) ENDEC.

ENCODED READ CLOCK (ENCRCLK) (differential ECL): This is the clock synchronized to the ENCODED READ DATA and is generated by the data separator.

READ GATE (RGATE) (TTL): This is a control signal which initiates a read operation when asserted. The input is active low.

INTERFACE WRITE DATA (IWDATA) (differential ECL): This is the unencoded NRZ write data from the disk controller. The INTERFACE WRITE CLOCK strobes the INTERFACE WRITE DATA into the VM5621/VM5622.

INTERFACE WRITE CLOCK (IWCLK) (differential ECL): This clock strobes the INTERFACE WRITE DATA into the encoder and is generated by the controller.

WRITE GATE (WGATE) (TTL): This is a control signal which initiates a write operation when asserted. The input is active low.

ADDRESS MARK ENABLE (AME) (TTL): This is a control signal which works in conjunction with the WRITE GATE input. Assertion of ADDRESS MARK ENABLE (low) concurrently with WRITE GATE asserted (low) causes writing of a 2T frequency address mark.

2F CLOCK (CLK2F) (differential ECL): This signal originates on the drive and is used to clock the encoder and lock to data timer blocks. The frequency of the 2F clock is two times the data bit rate.

RSOL (TTL): Used by an intelligent interface controller to correct a detected frame error (caused by a system noise) active on falling edge.

OUTPUT SIGNALS:

INTERFACE READ DATA (IRDATA) (differential ECL): This is the decoded read data from the disk. A high level represents a one of decoded data. It is strobed into the disk controller by the positive edge of the INTERFACE READ CLOCK.

INTERFACE READ CLOCK (IRCLK) (differential ECL): This is the clock synchronized to the INTERFACE READ DATA and drives the READ CLOCK input of the disk controller. The positive edge of the REFERENCE CLOCK should be used by the disk controller to strobe the READ DATA bit when in the read mode.

LOCK TO DATA (LTDATA) (TTL): This is a control output which signifies that a minimum length of a preamble pattern has been read. This output may be used to switch the Data Separator circuit from a high to a low tracking rate mode. The output is active low.

ENCODED WRITE DATA (ENCDATA) (differential ECL): This is the encoded (2,7) write data in RZ format. It drives the Read/Write amplifier circuit. A high level pulse returning to zero is output for each 'one' that is to be written on the disk's media.

DVALID (ECL): An active high signal in sync with valid encoded data (ENCDATAP, ENCDATAN).

CLKFLT (TTL): An active low signal which detects an 8 or greater gap in the interface write clock.

CIRCUIT CHARACTERISTICS

2T ADDRESS MARK: This address mark actually violates the (2,7) RLL constraints. Instead of detecting a gap, the VM5621/VM5622 will write a 2T frequency address mark but is not capable of detecting the address mark. An external circuit is required for 2T address mark detection.

Decoding Sequence of Events

A read operation is initiated by asserting READ-GATE (low) with AME high. At this time, the LTDATA timer circuit begins to count 2f clock pulses and the data separator IC begins locking to the preamble sync field. LTDATA remains false for 64 2f clock cycles after READ GATE is asserted. After the timer has completed its count, LTDATA is asserted and the LTDATA output goes low, the decoder synchronizes itself to the preamble sync field (4T pattern), and the read data is decoded. Refer to the control timing diagrams.

DATA/ (2,7) CODE MAPPING

NRZ DATA ←		*CODE* ←	
MSB	*LSB*	*MSB*	*LSB*
00		1000	
01		0100	
100		001000	
101		100100	
111		000100	
1100		00001000	
1101		00100100	

Most significant bit (MSB) is read/written first.

DATA RECOVERY CIRCUITS

VTC Inc., 2800 East Old Shakopee Road, Bloomington, MN 55425, 612-853-5100

DC CHARACTERISTICS Unless otherwise specified, ambient operating conditions shall apply, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
TTL Inputs (Note 1)						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.5V, note 4			20	µA
		V_{IH} = 6V, V_{CC} = 5.5V, note 4			100	
Input Low Current	I_{IL}	V_{IN} = 0.5V, V_{CC} = 5.5V, note 4			-0.6	mA
Output High Voltage	V_{OH}	V_{CC} = 4.5V; I_{OH} = -400µA, note 4	2.5			V
Output Low Voltage	V_{OL}	V_{CC} = 4.5V; I_{OL} = 4mA, note 4			0.4	V
Input Clamp Voltage	V_{IK}	V_{CC} = 4.5V; V_{IN} = -18mA, note 4			-1.2	V
Output Short Circuit Current	I_{OS}	V_{CC} = 5.5V; V_{IN} = 0V, notes 3 & 4	-20		-130	mA
Differential ECL Inputs (Notes 2 & 4)						
Common Mode Input Voltage	V_{CIM}		V_{CC} - 2.3		V_{CC} - 0.3	V
Differential Input Voltage	V_{INDIF}		200			mV
Input High Current	I_{IH}	V_{IH} = maximum			25	µA
Input Low Current	I_{IL}	V_{IL} = maximum			25	µA
Voltage Output High	V_{OH}	0°C	V_{CC} - 1.02		V_{CC} - 0.78	V
		25°C	V_{CC} - 0.98		V_{CC} - 0.75	
		70°C	V_{CC} - 0.92		V_{CC} - 0.66	
Voltage Output Low	V_{OL}	0°C	V_{CC} - 1.95		V_{CC} - 1.63	V
		25°C	V_{CC} - 1.95		V_{CC} - 1.63	
		70°C	V_{CC} - 1.95		V_{CC} - 1.63	
MECL 10KH Compatible (Notes 2 & 4)						
Voltage Output High	V_{OH}	0°C	V_{CC} - 1.00		V_{CC} - 0.84	V
		25°C	V_{CC} - 0.96		V_{CC} - 0.81	
		70°C	V_{CC} - 0.90		V_{CC} - 0.74	
Voltage Output Low	V_{OL}	0°C	V_{CC} - 1.95		V_{CC} - 1.63	V
		25°C	V_{CC} - 1.95		V_{CC} - 1.63	
		70°C	V_{CC} - 1.95		V_{CC} - 1.63	

Note 1: TTL inputs will float to a logic HI if left unconnected.

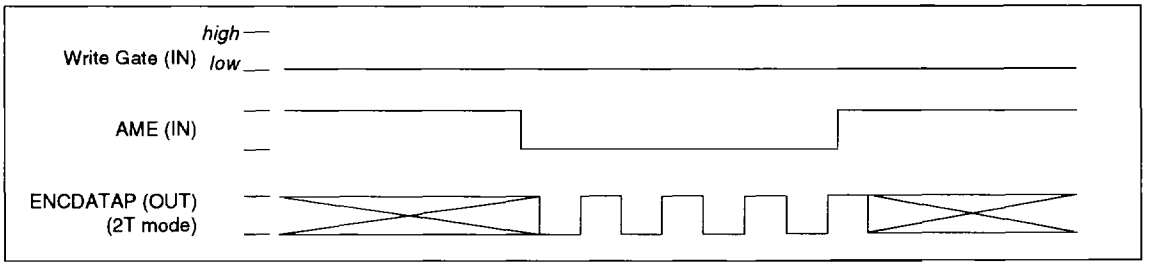
Note 2: All inputs and outputs denoted as ECL track with the V_{CC} supply voltage.

Note 3: Not more than one output shorted at one time duration of test not to exceed one second

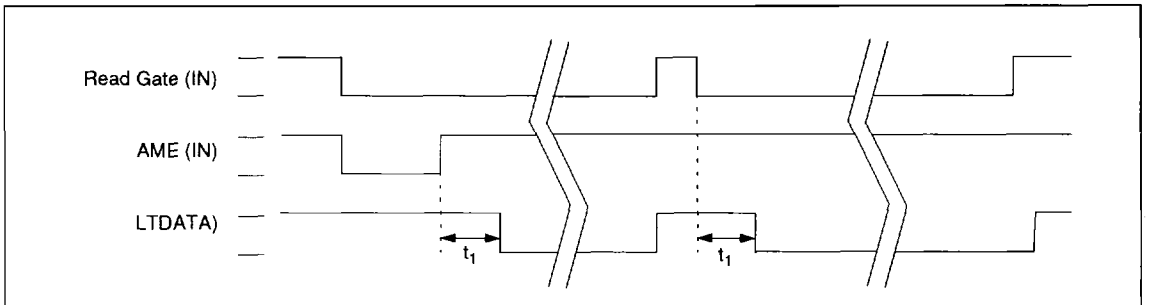
Note 4: DC test limits are specified after thermal equilbrium has been established with the device having a controlled transverse air flow of 750lfpm. VM5621, V_{CC} = 5.0V, V_{EE} = 0, V_{DD} N/A. VM5622, V_{CC} = 0, V_{DD} = 5.0V, V_{EE} = -5.2V. All ECL outputs are loaded with 50Ω to V_{CC} - 2.0V, except DVALID which is loaded with 100Ω to V_{CC} - 2.0V.

CONTROL SIGNAL TIMING

A: Address Mark Write



B: Read Timing (Compatible with SMD Standards)



t_1 = preset lock time of 64 • T (where T is equal to one period of 2F clock)

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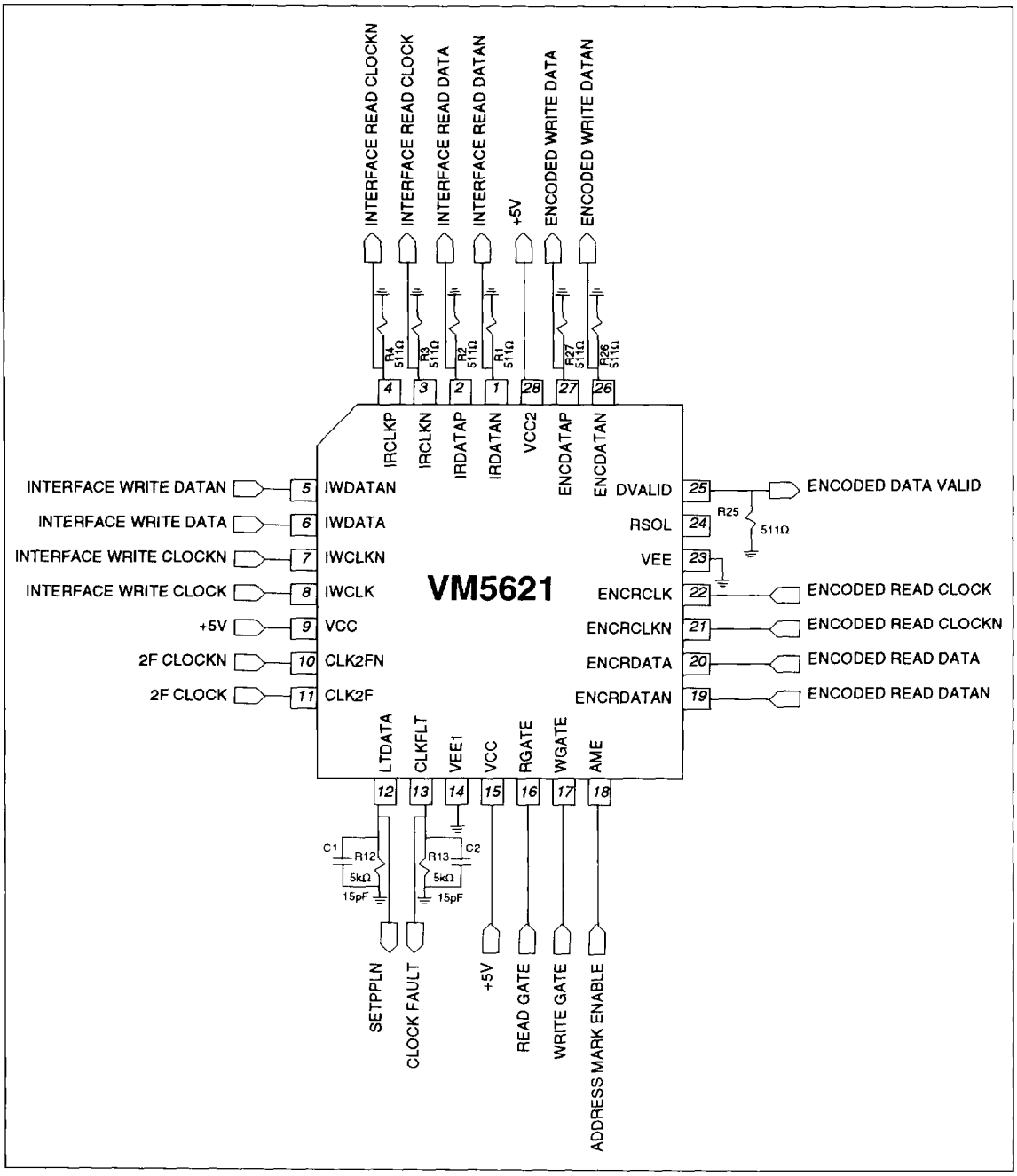

Figure 1: VM5621 Typical Connection Diagram

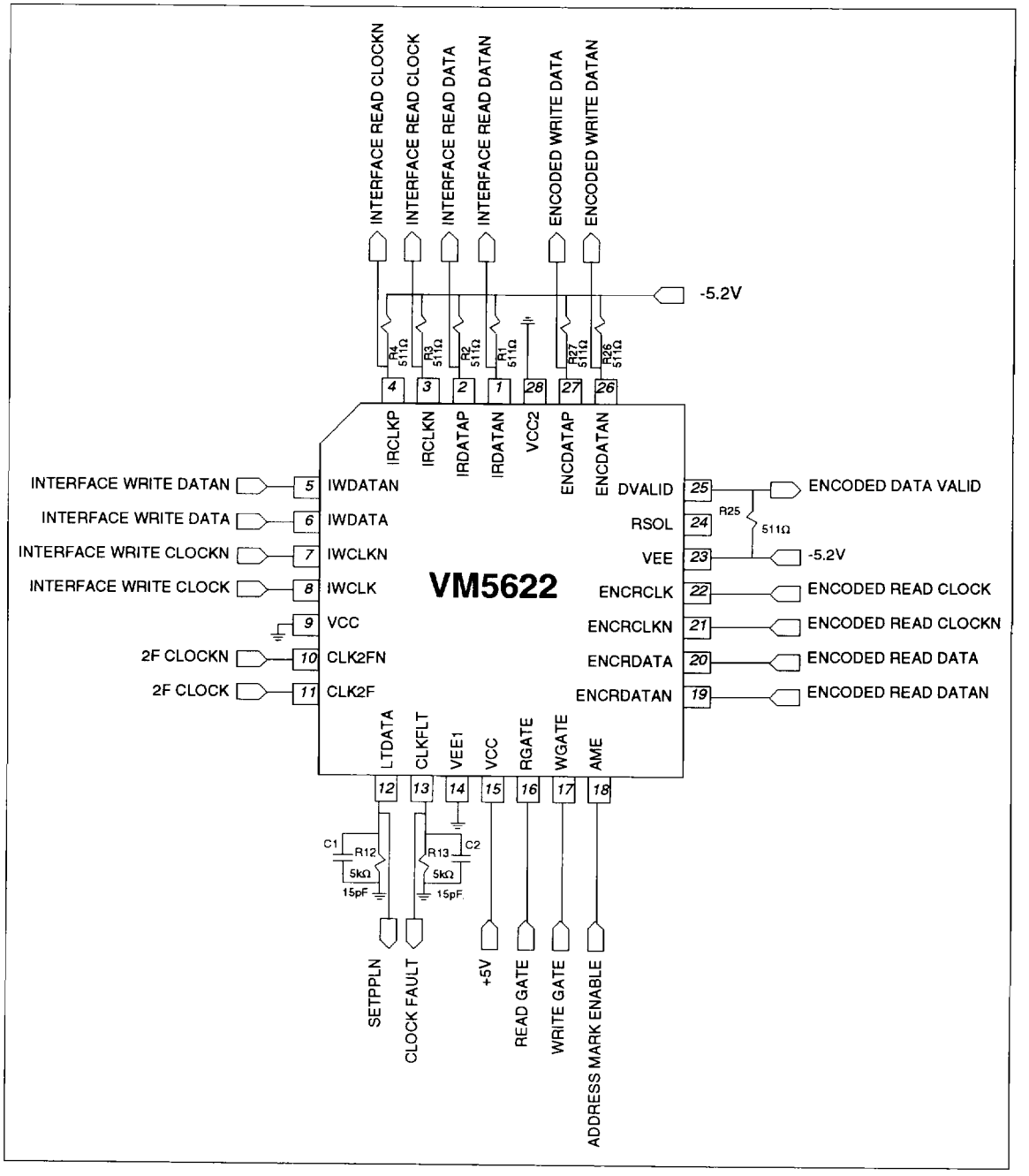

Figure 2: VM5622 Typical Connection Diagram