GENERAL INSTRUMENT	AY2661 1/0/210

34 Res Orig

PRELIMINARY 005644

5644 GI

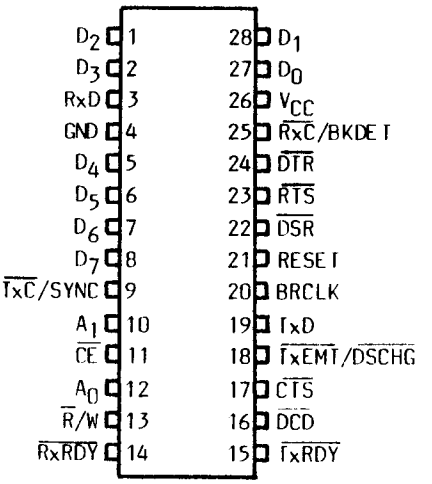
ENHANCED PROGRAMMABLE COMMUNICATION INTERFACE

FEATURES:

- Synchronous and Asynchronous full or half duplex operation
- On-chip baud rate generator - 3 standards
- Double buffering of data
- TTL compatible
- Single +5 volt power supply
- Compatible with SC2661, COM2661

PIN CONFIGURATION
28 LEAD DUAL IN LINE

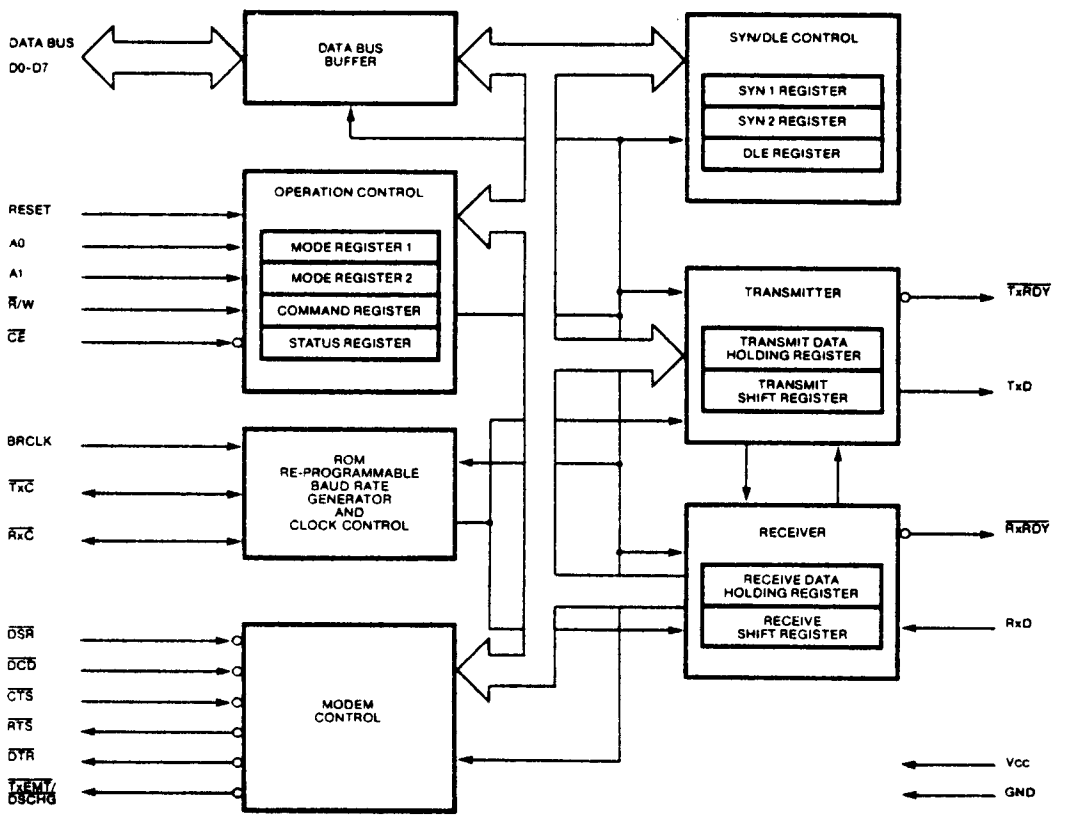
TOP VIEW



DESCRIPTION

The AY2661 is a universal synchronous/asynchronous receiver/transmitter designed for microcomputer system data communications. It may be programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including Bi-Sync. The AY2661 receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the device will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The AY2661 will signal the processor when it has completely received or transmitted a character and requires service. Complete status information including data format errors and control signals is available to the processor at any time.

Fig. 1 - AY2661 BLOCK DIAGRAM



PIN FUNCTIONS

PIN NAME	FUNCTION
BRCLK	Clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$/BKDET	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
$\overline{TxC}$/XSYNC	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output for an external jam synchronization input.
RxD	Serial data input to the receiver. "Mark" is high, "space" is low.
TxD	Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.
$\overline{DSR}$	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1.
$\overline{DCD}$	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1. If $\overline{DCD}$ goes high while receiving, the RxC is internally inhibited.
$\overline{CTS}$	Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{DTR}$	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{RTS}$	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. If the transmit shift register is not empty when CR5 is reset (1 to 0) , then $\overline{RTS}$ will go high one TxC time after the last serial bit is transmitted.
RESET	A high on this input performs a master reset on the AY2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.

PIN FUNCTIONS (continued)

PIN NAME	FUNCTION
A_1-A_0	Address lines used to select internal EPCI registers.
$\overline{R}/W$	Read command when low, write command when high.
$\overline{CE}$	Chip enable command. When low, indicates that control and data lines to the EPCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the three-state condition.
D_7-D_0	8-bit, three-state data bus used to transfer commands, data and status between EPCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
TxEMT/ $\overline{DSCHG}$	This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

AY2661 OPERATION

The functional operation of the AY2661 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc.

RECEIVER

The AY2661 is conditioned to receive data when the DCD input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

When the AY2661 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the AY2661 returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been acheived, the AY2661 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the $\overline{RxRDY}$ output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

TRANSMITTER

The AY2661 is conditioned to transmit when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The AY2661 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the $\overline{TxRDY}$ output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the AY2661 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity if commanded) are generated by the AY2661 unless the processor fails to send a new character to the AY2661 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the AY2661 asserts TxEMI and automatically "fills" the gap by transmitting SYN1s, and SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

AY2661 PROGRAMMING

Prior to initiating data communications, the AY2661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The AY2661 can be reconfigured at any time during program execution. A flow chart of the initialization process follows.

The internal registers of the AY2661 are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A1 and A0 inputs. The conditions necessary to address each register are shown in Fig. 3.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and $\overline{R}/W$=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1 and subsequent operation addressed Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The AY2661 register formats are summarized in Tables 6, 7, 8 and 9. Mode Registers 1 and 2 define the general operational characteristics of the AY2661, while the Command Register controls the operation within this basic framework. The AY2661 indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

FIG. 2 AY2661 INITIALIZATION FLOW CHART

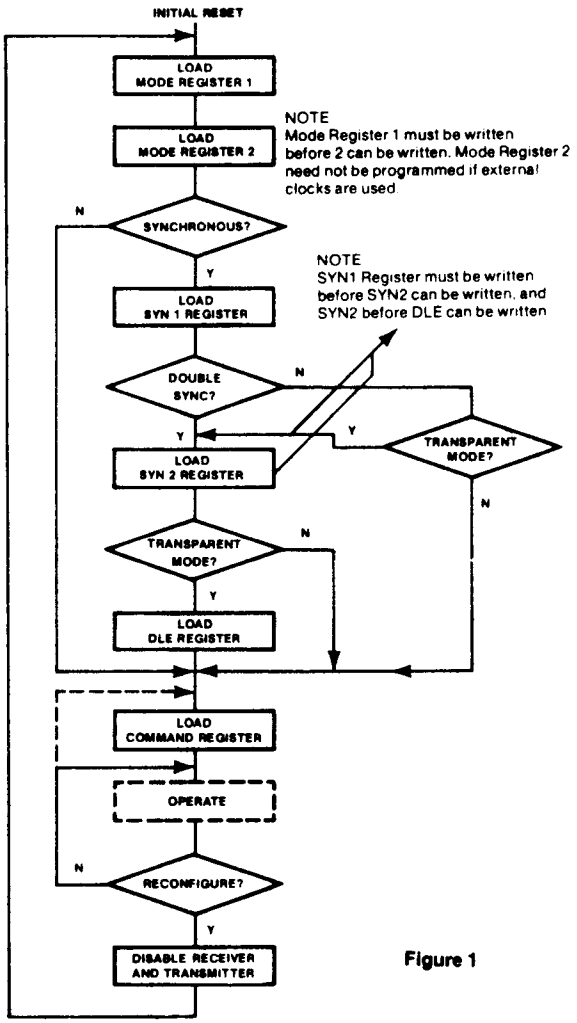


Figure 1

FIG. 3 AY2661 REGISTER ADDRESSING

CE	A1	A0	R/W	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1 and 2
0	1	0	1	Write mode registers 1 and 2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE

See AC Characteristics section for timing requirements.

MODE REGISTER 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
Async: Stop Bit Length 00 = Invalid 01 = 1 stop bit 10 = 1 1/2 stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency Control** 0 = Normal 1 = Transparent						

NOTE

Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

MODE REGISTER 2 (MR2)

MR27 - MR24											MR23 - MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC[1]	RxC/TxC	sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC[1]	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	See baud rates in Fig. 7
0100	E	E	TxC	RxC	1100	E	E	XSYNC[1]	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC[1]	RxC	sync	
0111	I	I	16X	16X	1110	I	I	16X	BKDET	async	

NOTES

1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-2, and DLE-SYN1 detection is disabled.

E = External clock

I = Internal clock (BRG)

1X and 16X are clock outputs

COMMAND REGISTER (CR)

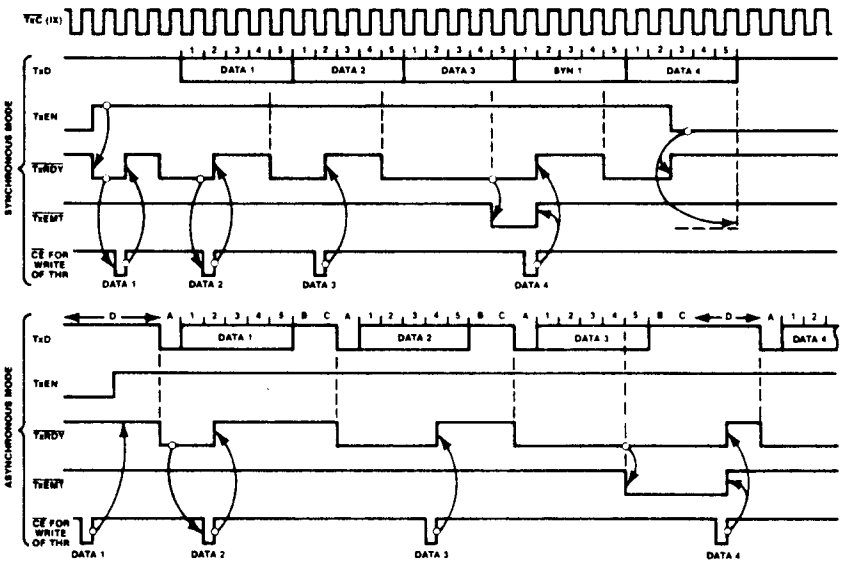
CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request To Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = Normal operation 01 = Async: Automatic echo mode Sync: SYN and/or DLE stripping mode 10 = Local loop back 11 = Remote loop back		0 = Force $\overline{RTS}$ output high one clock time after TxSR serialization 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flags in status register (FE, OE, PE/DLE detect.)	Async: Force break 0 = Normal 1 = Force break Sync: Send DLE 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable	0 = Force $\overline{DTR}$ output high 1 = Force $\overline{DTR}$ output low	0 = Disable 1 = Enable

STATUS REGISTER (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	Data Carrier Detect	FE/SYN Detect	Overrun	PE/DLE Detect	TxEMT/DSCHG	RxRDY	TxRDY
0 = $\overline{DSR}$ input is high 1 = $\overline{DSR}$ input is low	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	Async: 0 = Normal 1 = Framing Error Sync: 0 = Normal 1 = SYN CHAR detected	0 = Normal 1 = Overrun Error	Async: 0 = Normal 1 = Parity error Sync: 0 = Normal 1 = Parity error or DLE received	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

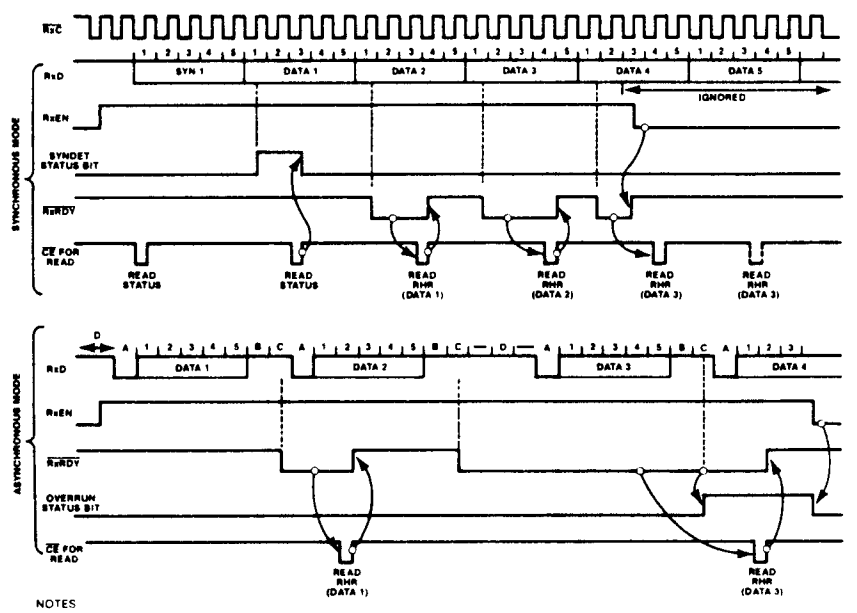
TIMING DIAGRAMS

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit or if parity is enabled at the beginning of the parity bit

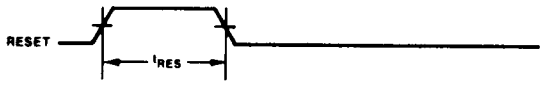
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



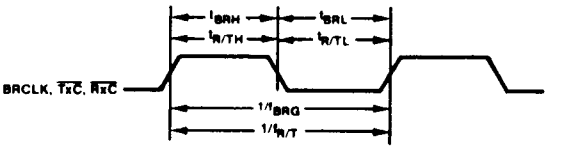
NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TIMING DIAGRAMS (continued)

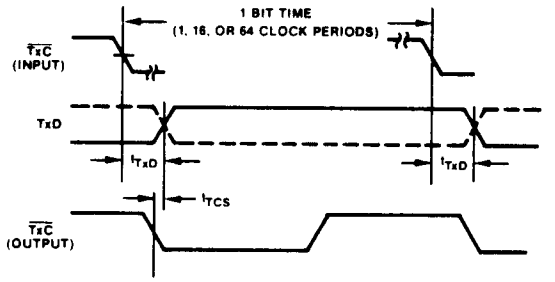
RESET



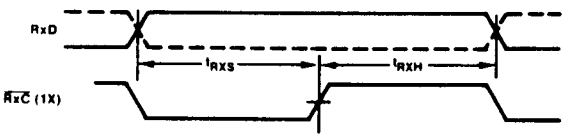
CLOCK



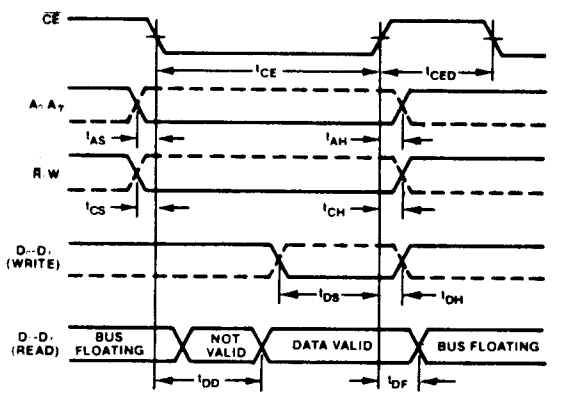
TRANSMIT



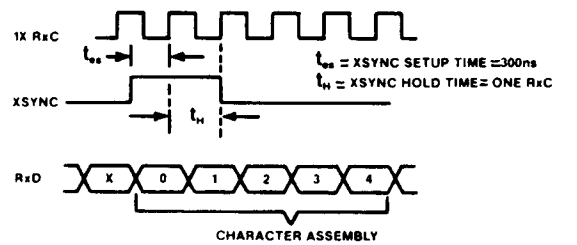
RECEIVE



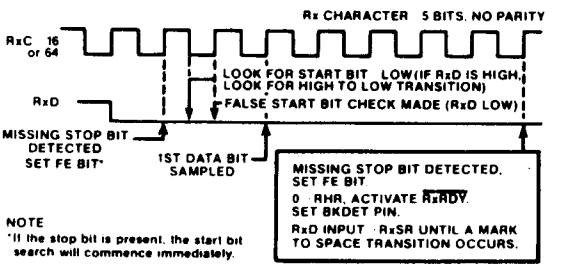
READ AND WRITE



EXTERNAL SYNCHRONIZATION WITH XSYNC



BREAK DETECTION TIMING



NOTE
*If the stop bit is present, the start bit search will commence immediately.

CHARACTERISTICS

Maximum Guaranteed Ratings*

Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.)..... +325°C
Positive Voltage on any Pin,
with respect to ground..... +18.0V
Negative Voltage on any Pin,
with respect to ground..... -0.3V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V +5%

Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
Input voltage						
Low	V_{IL}		-	0.8	V	
High	V_{IH}	2.0	-	-		
Output voltage						
Low	V_{OL}	-	-	0.4	V	I_{OL} = 2.2mA
High	V_{OH}	2.4	-	-		I_{OH} = 400μA
Input leakage current	I_{IL}	-	-	10	μA	V_{IN} = 0 to 5.5V
Output leakage current						
Data bus high	I_{LH}	-	-	10	μA	V_O = 4.0V
Data bus low	I_{LL}	-	-	10	μA	V_O = 0.45V
Power supply current	I_{CC}	-	-	150	mA	
Capacitance						
Input	C_{IN}	-	-	20	pF	fc = 1MHz
Output	C_{OUT}	-	-	20	pF	Unmeasured pins tied
Input/Output	C_{IO}	-	-	20	pF	to ground

CHARACTERISTICS (continued)

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V +5%

Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
Pulse width						
Reset	t_{RES}	1000	-	-	ns	
Chip enable	t_{CE}	250	-	-	ns	
Setup and hold time						
Address setup	t_{AS}	10	-	-	ns	
Address hold	t_{AH}	10	-	-	ns	
R/W control setup	t_{CS}	10	-	-	ns	
R/W control hold	t_{CH}	10	-	-	ns	
Data setup for write	t_{DS}	150	-	-	ns	
Data hold for write	t_{DH}	0	-	-	ns	
Rx data setup	t_{RXS}	300	-	-	ns	
Rx data hold	t_{RXH}	350	-	-	ns	
Data delay time for read	t_{DD}	-	-	200	ns	C_L = 150pF
Data bus floating time for read	t_{DF}	-	-	100	ns	C_L = 150pF
CE to CE delay	t_{CED}	600	-	-	ns	
Input clock frequency						
Baud rate generator (2661-1, -2)	f_{BRG}	1.0	4.9152	4.9202	MHz	
Baud rate generator (2661-5)	f_{BRG}	1.0	5.0688	5.0738	MHz	
TxC or RxC	f_{RI} [1]	dc	-	1.0	MHz	
Clock width						
Baud rate high (2661-1, -2)	t_{BRH}	75	-	-	ns	f_{BRG} = 4.915MHz; measured at V_{IH}
Baud rate high (2661-5)	t_{BRH}	70	-	-	ns	f_{BRG} = 5.0688MHz; measured at V_{IH}
Baud rate low (2661-1, -2)	t_{BRL}	75	-	-	ns	f_{BRG} = 4.915MHz; measured at V_{IL}
Baud rate low (2661-5)	t_{BRL}	70	-	-	ns	f_{BRG} = 5.0688MHz; measured at V_{IL}
TxC or RxC high	t_{RTH1}	480	-	-	ns	
TxC or RxC low	t_{RTL}	480	-	-	ns	
TxD delay from falling edge of TxC	t_{TXD}	-	-	650	ns	C_L = 150pF
Skew between TxD changing and falling edge of TxC output	t_{TCS}	-	0	-	ns	C_L = 150pF

NOTE:

1. f_{RI} and t_{RIL} shown all modes except Local Loopback. For Local Loopback mode f_{RI} = 0.7MHz and t_{RIL} = 700ns min.

BAUD RATE STANDARDS - Fig. 7

AY2661-A
(BRCLK = 4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	-	6144
0001	75	1.2	-	4096
0010	110	1.7598	-0.01	2793
0011	134.5	2.152	-	2284
0100	150	2.4	-	2048
0101	200	3.2	-	1536
0110	300	4.8	-	1024
0111	600	9.6	-	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	-	256
1010	1800	28.7438	-0.19	171
1011	2000	31.9168	-0.26	154
1100	2400	38.4	-	128
1101	4800	76.8	-	64
1110	9600	153.6	-	32
1111	19200	307.2	-	16

AY2661-B
(BRCLK = 4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	-	6144
0010	75	1.2	-	4096
0011	110	1.7598	-0.01	2793
0100	134.5	2.152	-	2284
0101	150	2.4	-	2048
0110	300	4.8	-	1024
0111	600	9.6	-	512
1000	1200	19.2	-	256
1001	1800	28.7438	-0.19	171
1010	2000	31.9168	-0.26	154
1011	2400	38.4	-	128
1100	4800	76.8	-	64
1101	9600	153.6	-	32
1110	19200	307.2	-	16
1111	38400	614.4	-	8

BAUD RATE STANDARDS - Fig. 7 (Cont'd)

AY2661-C
(BRCLK = 5.0688MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	-	6336
0001	75	1.2	-	4224
0010	110	0.76	-	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	-	2112
0101	300	4.8	-	1056
0110	600	9.6	-	528
0111	1200	19.2	-	264
1000	1800	28.8	-	176
1001	2000	32.081	0.253	158
1010	2400	38.4	-	132
1011	3600	57.6	-	88
1100	4800	76.8	-	66
1101	7200	115.2	-	44
1110	9600	153.6	-	33
1111	19200	316.8	3.125	16

NOTE

16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

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