JEIDA Ver. 4 UNPROGRAMMED ONE TIME PROGRAMMABLE ROM

VARIATION

Part Number	Memory Size	Description
BWB065SD*0	64K Bytes	32K × 16 bits JEIDA Ver.4 CMOS OTP ROM CARD
BWB129SD*0	128K Bytes	64K × 16 bits JEIDA Ver.4 CMOS OTP ROM CARD
BWB257SD*0	256K Bytes	128K × 16 bits JEIDA Ver.4 CMOS OTP ROM CARD
BWB513SD*0	512K Bytes	256K × 16 bits JEIDA Ver.4 CMOS OTP ROM CARD
BWB101SD*0	1M Bytes	512K × 16 bits JEIDA Ver.4 CMOS OTP ROM CARD (Under development)
BWB201SD*0	2M Bytes	1M × 16 bits JEIDA Ver.4 CMOS OTP ROM CARD (Under development)

Note: * : Attribute memory type
X : 2K Bytes EEPROM (can be read/written)
Y : No attribute memory (output "FF") (read only)

OUTLINE OF FUNCTIONS AND FEATURES

(1) This memory card conforms to JEIDA Ver. 4.
(2) Size of the card
Width : 54.0 mm
Length : 85.6 mm
Thickness : 3.3 mm
(3) Includes exclusive IC's for the control of I/O and power functions.
(4) Support 2 type attribute memory
4-1) With 2K Bytes EEPROM which can be read/written.
4-2) Without attribute memory which can be read only. (output "FF")
(5) This card is only used for customer's development.
(6) Card Type : 68 pin Two-piece Type

MAXIMUM RATING

Symbol	Description	Note	Min	Max	Unit
V_{CC}	Supply voltage		–0.5	7.0	V
V_{IN}	Input signal voltage	1	–0.5	V_{CC} +0.5	V
V_{OUT}	Output signal voltage	1	–0.5	V_{CC}	V
T_{OPR}	Operating temperature		0	60	°C
T_{STR}	Storage temperature		–20	60	°C
HUM	Humidity	2	10	90	%
P_D	Power dissipation			2.0	W
V_{PP}	Program supply voltage		–0.5	14.0	V

Notes: 1. Under 7.0 V
2. No dew condition

CAPACITANCE
(Ta = 25°C, V_{IN} / V_{OUT} = 0 V, f = 1 MHz)

Symbol	Description	Min	Typ	Max	Unit
C_1	Input capacitance		10	14	pF
C_2	Input/output capacitance		10	14	pF

Note: The above figures are for reference only

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage at read	4.75	5.0	5.25	V
V_{PP}	Supply at read	4.75	5.0	5.25	V
V_{CC}	Supply voltage at write	6.0	6.25	6.5	V
V_{PP}	Supply at write	12.5	12.75	13.0	V
V_{IH}	High level input voltage	3.5	—	V_{CC} +0.3	V
V_{IL}	Low level input voltage	–0.3	—	1.0	V

DC ELECTRICAL CHARACTERISTICS
(V_{CC} = 5 V, Ta = 25°C)

Symbol	Description	Note	Condition	Min	Typ	Max	Unit
I_{LI}	Low level input current	1, 3	V_{IN} = 0 V	–10	—	10	µA
		2		–53	—	–48	µA
I_{HI}	High level input current	1, 2	V_{IN} = 5 V	–10	—	100	µA
		3		10	—	50	µA
V_{OH}	High level output voltage	3	I_{OH} = –2.0 mA	V_{CC}-0.4	—	—	V
V_{OL}	Low level output voltage	3	I_{OL} = 6.0 mA	—	—	V_{SS} +0.4	V

Notes : 1. A0 to A20

2. $\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$, $\overline{OE}$, $\overline{REG}$
   Pull-up to V_{CC} through 100K ohm

3. D_0 to D_{15}
   Pull-down to GND through 100K ohm

CURRENT CONSUMPTION
(Ta = 25°C, VCC = 5 V ±5%)

Symbol	Description	Condition		Min	Typ	Max	Unit
ISTBY	Standby current	$\overline{CE}$ = $\overline{WE}$ = $\overline{OE}$ = $\overline{REG}$ = VCC –0.2 V Other = VIL/VIH		—	1.0	1.5	mA
IACT1	Active current (Read)	$\overline{CE}$ = VIL, IOUT = 0 mA, Other = VIL/VIH	f = 1MHz	—	20	40	mA
			f = Max	—	—	70	mA
IACT2	Active curernt (Program)	Programming (ICC)		—	—	60	mA
IPP1	VPP current (Read)	VPP = VCC ±0.25 V		–20	—	20	µA
IPP2	VPP current (Program)	VPP = 13 V		—	—	100	mA

OPERATING MODES (READ) OF COMMON MEMORY

Mode	$\overline{REG}$	A0	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	D0 to D7	D8 to D15
Standby	*	*	VIH	VIH	*	*	HZ	HZ
Even data read	VIH	VIL	VIL	VIH	VIL	VIH	Output	HZ
ODD data read 1	VIH	VIH	VIL	VIH	VIL	VIH	Output	HZ
ODD data read 2	VIH	*	VIH	VIL	VIL	VIH	HZ	Output
Word read	VIH	*	VIL	VIL	VIL	VIH	Output	Output

Notes: HZ = High impedance
(Pull-down to GND through 100K ohm)
* = Input is VIH or VIL
VPP = VCC ±0.25 V

OPERATING MODES OF ATTRIBUTE MEMORY

Mode	$\overline{REG}$	A0	A1 to A11	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{WE}$	D0 to D7	D8 to D1
Data read	V_{IL} V_{IL}	V_{IL} V_{IH}	* *	V_{IL} V_{IL}	V_{IH} V_{IH}	V_{IL} V_{IL}	V_{IH} V_{IH}	Output HZ	HZ HZ
Word data read	V_{IL}	*	*	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Output	HZ
Data write	V_{IL} V_{IL}	V_{IL} V_{IH}	* *	V_{IL} V_{IL}	V_{IH} V_{IH}	V_{IH} V_{IH}	V_{IL} V_{IL}	Input don't care	don't care don't care
Word data write	V_{IL}	*	*	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Input	don't care

Notes: HZ = High impedance
(Pull-down to GND through 100K ohm)
* = Input is V_{IH} or V_{IL}

OPERATING MODES (PROGRAM) OF COMMON MEMORY
(V_{PP} = 12.75 V ±0.25V, V_{CC} = 6.25 V ±0.25 V)

Mode	$\overline{REG}$	A0	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7	D8 to D15	V_{PP1}	V_{PP2}
Standby	*	*	V_{IH}	V_{IH}	*	*	HZ	HZ	V_{CC}	V_{CC}
Even data program	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Input	don't care	V_{PP}	V_{CC}
Odd data program 1	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Input	don't care	V_{CC}	V_{PP}
Even data program 2	V_{IH}	*	V_{IH}	V_{IL}	V_{IH}	V_{IL}	don't care	Input	V_{CC}	V_{PP}
Word data program	V_{IH}	*	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Input	Input	V_{PP}	V_{PP}

OPERATING MODES (PROGRAM) OF COMMON MEMORY (VPP = 12.75 V ±0.25V, VCC = 6.25 V ±0.25 V)

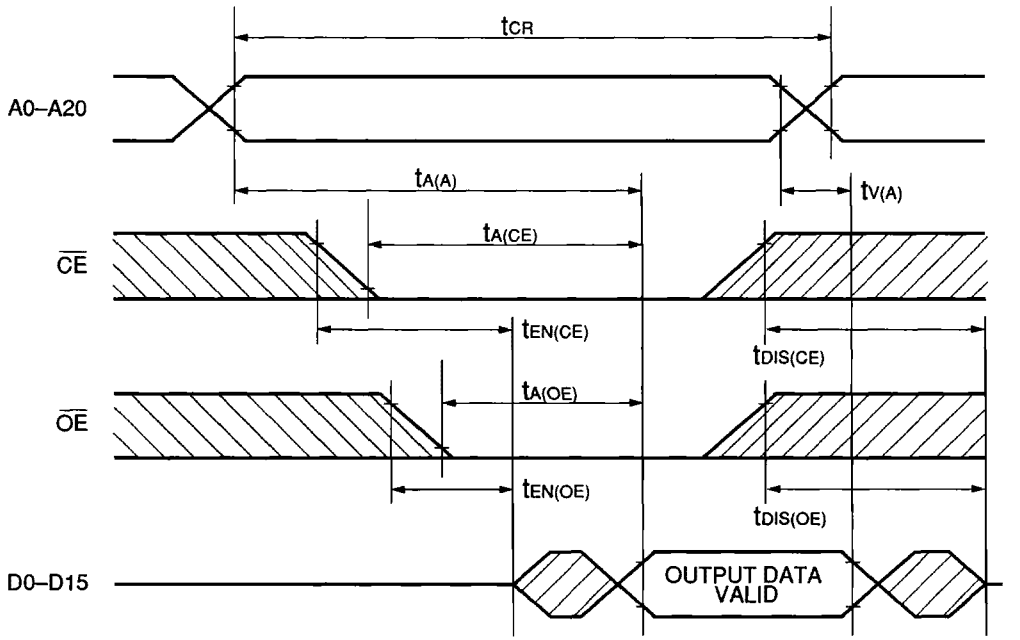
Mode	$\overline{REG}$	A0	$\overline{CE1}$	$\overline{CE2}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7	D8 to D15	VPP1	VPP2
Even data program Verify	VIH	VIL	VIL	VIH	VIL	VIH	Output	HZ	VPP	VCC
Odd data program Verify 1	VIH	VIH	VIL	VIH	VIL	VIH	Output	HZ	VCC	VPP
Odd data program Verify 2	VIH	*	VIH	VIL	VIL	VIH	HZ	Output	VCC	VPP
Word data program verify	VIH	*	VIL	VIL	VIL	VIH	Output	Output	VPP	VPP

Notes: * = Input is VIH or VIL
HZ = High impedance
(Pull-down to GND through 100K ohm)

AC ELECTRICAL CHARACTERISTICS AT READ OF COMMON MEMORY

Symbol	Parameter	Min	Max	Unit
tCR	Read cycle time	250	—	ns
tA (A)	Address access time	—	250	ns
tA (CE)	Card enable access time	—	250	ns
tA (OE)	Output enable access time	—	125	ns
tDIS (CE)	Output disable time from card enable	—	100	ns
tDIS (OE)	Output disable time from output enable	—	100	ns
tEN (CE)	Output enable time from card enable	5	—	ns
tEN (OE)	Output enable time from output enable	5	—	ns
tV (A)	Valid data hold time from address invalid	0	—	ns

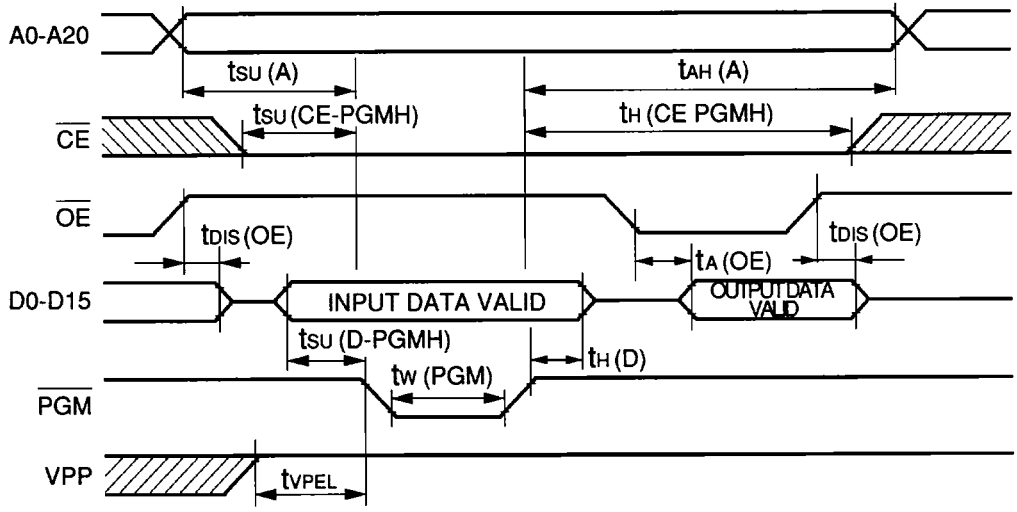
READ TIMING OF COMMON MEMORY



AC ELECTRICAL CHARACTERISTICS AT PROGRAM OF COMMON MEMORY

Symbol	Parameter	Min	Max	Unit
t_{SU} (A)	Address setup time	2	—	us
t_{AH} (A)	Address hold time	2	—	us
t_{SU} (D-PGMH)	Data setup time	2	—	us
t_{H} (D)	Data hold time	2	—	us
t_{SU} (CE-PGMH)	Card enable setup time	2	—	us
t_{H} (CE-PGMH)	Card enable hold time	2	—	us
t_{W} (PGM)	Write pulse width	95	105	us
t_{A} (OE)	Output enable access time	—	150	ns
t_{DIS} (OE)	Output disable time from output enable	—	100	ns
t_{VPEL}	V_{PP} setup time	2	—	us

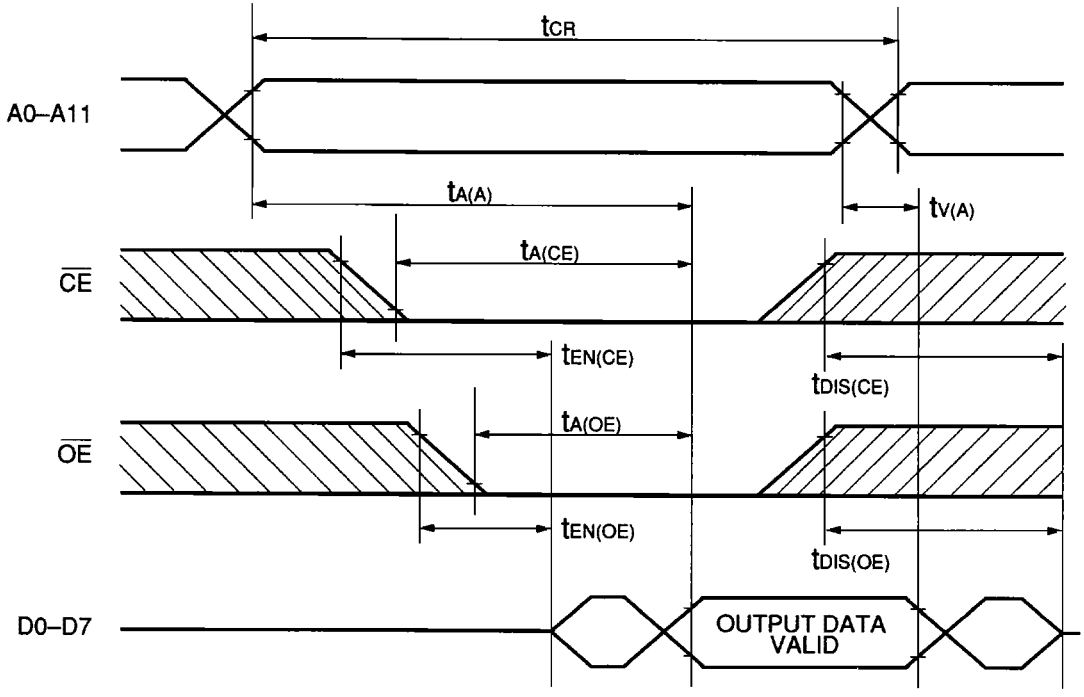
PROGRAM TIMING OF COMMON MEMORY



AC ELECTRICAL CHARACTERISTICS AT READ OF ATTRIBUTE MEMORY

Symbol	Parameter	Min	Max	Unit
t_{CR}	Read cycle time	300	—	ns
t_A (A)	Address access time	—	300	ns
t_A (CE)	Card enable access time	—	300	ns
t_A (OE)	Output enable access time	—	150	ns
t_{DIS} (CE)	Output disable time from card enable	—	100	ns
t_{DIS} (OE)	Output disable time from output enable	—	100	ns
t_{EN} (CE)	Output enable time from card enable	5	—	ns
t_{EN} (OE)	Output enable time from output enable	5	—	ns
t_V (A)	Valid data hold time from address invalid	0	—	ns

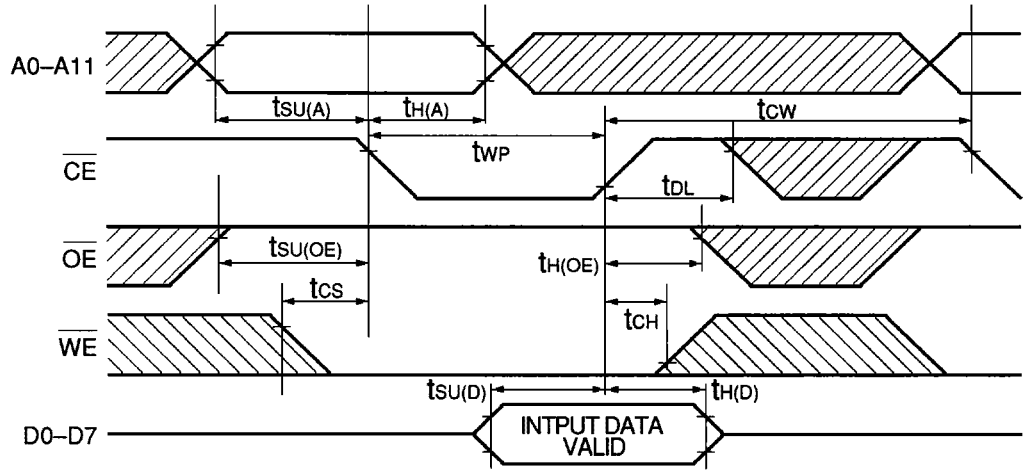
READ TIMING OF ATTRIBUTE MEMORY



WRITE CYCLE OF ATTRIBUTE MEMORY ($\overline{CE}$ CONTROLED WRITE) (2K Bytes EEPROM ATTRIBUTE MEMORY)

Symbol	Parameter	Min	Max	Unit
t_{CW}	Write cycle time	15	—	ms
t_{WP}	Write pulse width	150	—	ns
t_{SU} (A)	Address setup time	30	—	ns
t_{SU} (D)	Data setup time	80	—	ns
t_{H} (D)	Data hold time	30	—	ns
t_{SU} (OE)	Output enable setup time	15	—	ns
t_{H} (OE)	Output enable hold time	15	—	ns
t_{H} (A)	Address hold time	100	—	ns
t_{CS}	Write setup time	30	—	ns
t_{CH}	Write hold time	0	—	ns
t_{DL}	Data latch time	50	—	ns

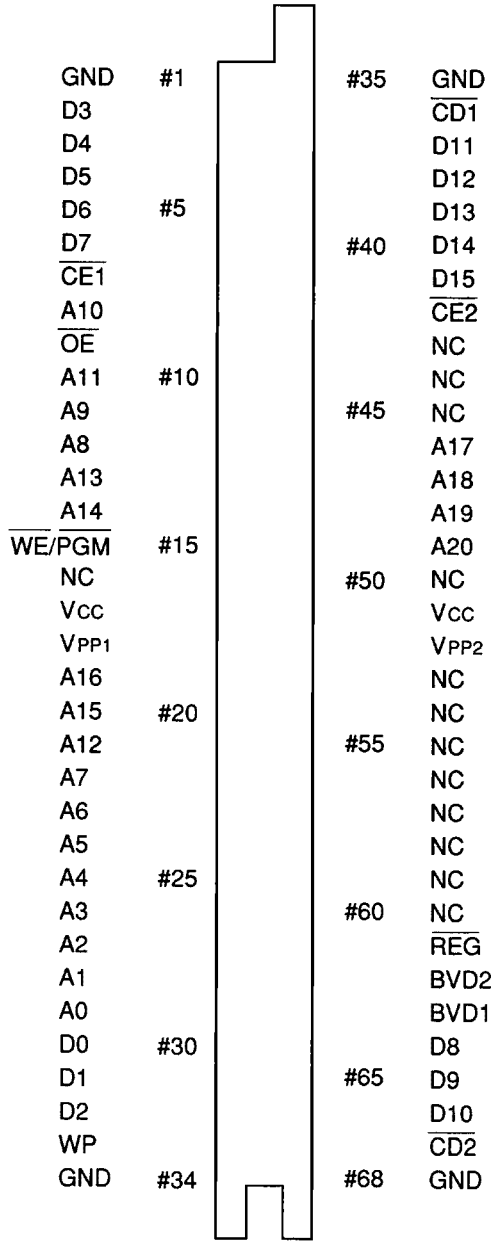
WRITE TIMING OF ATTRIBUTE MEMORY ($\overline{WE}$ CONTROLLED WRITE) (2K Bytes EEPROM ATTRIBUTE MEMORY)



<< AC test conditions >>

Output load : 1 TTL gate + 100 pF (include jig)

PIN ASSIGNMENT



PIN ASSIGNMENT

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	GND	23	A6	46	A17*
2	D3	24	A5	47	A18*
3	D4	25	A4	48	A19*
4	D5	26	A3	49	A20*
5	D6	27	A2	50	NC
6	D7	28	A1	51	V_{CC}
7	$\overline{CE1}$	29	A0	52	V_{PP2}
8	A10	30	D0	53	NC
9	$\overline{OE}$	31	D1	54	NC
10	A11	32	D2	55	NC
11	A9	33	WP**	56	NC
12	A8	34	GND	57	NC
13	A13	35	GND	58	NC
14	A14	36	$\overline{CD1}$	59	NC
15	$\overline{WE/PGM}$	37	D11	60	NC
16	NC	38	D12	61	$\overline{REG}$
17	V_{CC}	39	D13	62	BVD2**
18	V_{PP1}	40	D14	63	BVD1**
19	A16	41	D15	64	D8
20	A15	42	CE2	65	D9
21	A12	43	NC	66	D10
22	A7	44	NC	67	$\overline{CD2}$
		45	NC	68	GND

Notes: *A17 : BWB257, BWB513, BWB101, BWB201
*A18 : BWB513, BWB101, BWB201
*A19 : BWB101, BWB201
*A20 : BWB201
NC : No connect
**WP, BVD1, BVD2 : This line is connected to V_{CC} inside Card.