MOTOROLA

MC74AC192
MC74AC193

Product Preview

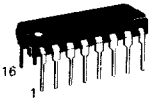
Up/Down Counters with Separate Up/Down Clocks

UP/DOWN COUNTERS WITH SEPARATE UP/DOWN CLOCKS

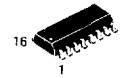
The MC74AC192 is an up/down BCD decade (8421) counter. The MC74AC193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

- High-Speed — 120 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load and Master Reset
- Outputs Source/Sink 24 mA

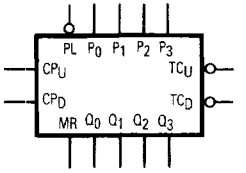


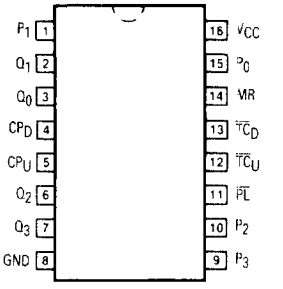
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

CP_U	Count Up Clock Input
CP_D	Count Down Clock Input
MR	Asynchronous Master Reset Input
$\overline{PL}$	Asynchronous Parallel Load Input
P_0–P_3	Parallel Data Inputs
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output
$\overline{TC}_U$	Terminal Count Up (Carry) Output

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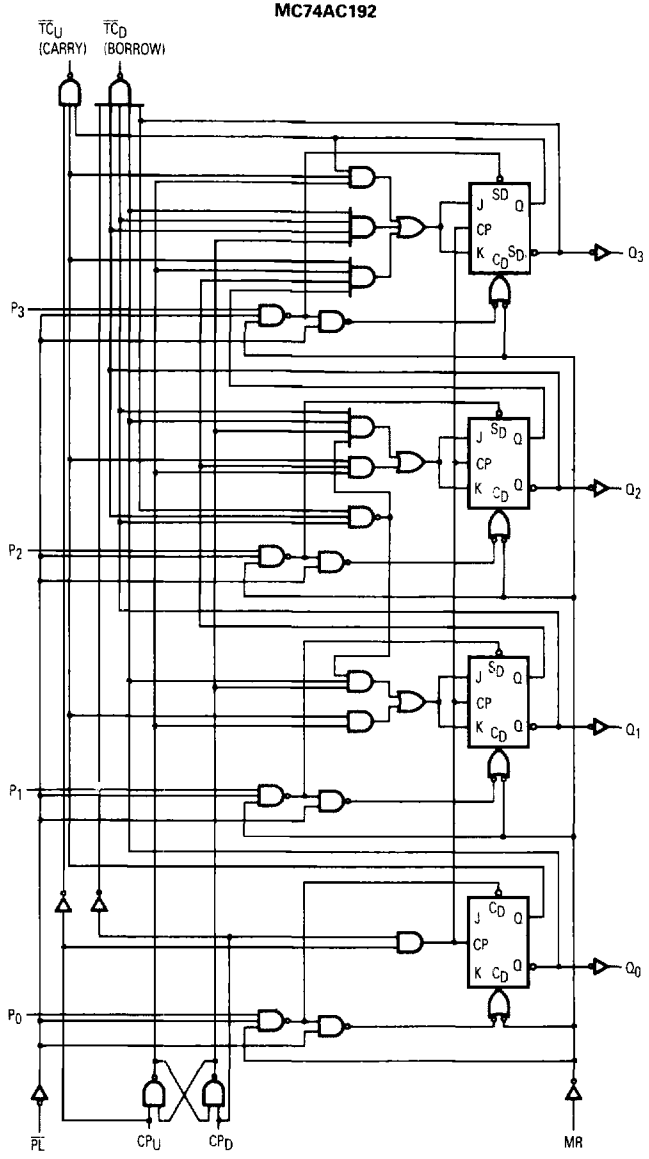
LOGIC DIAGRAM

MC74AC192



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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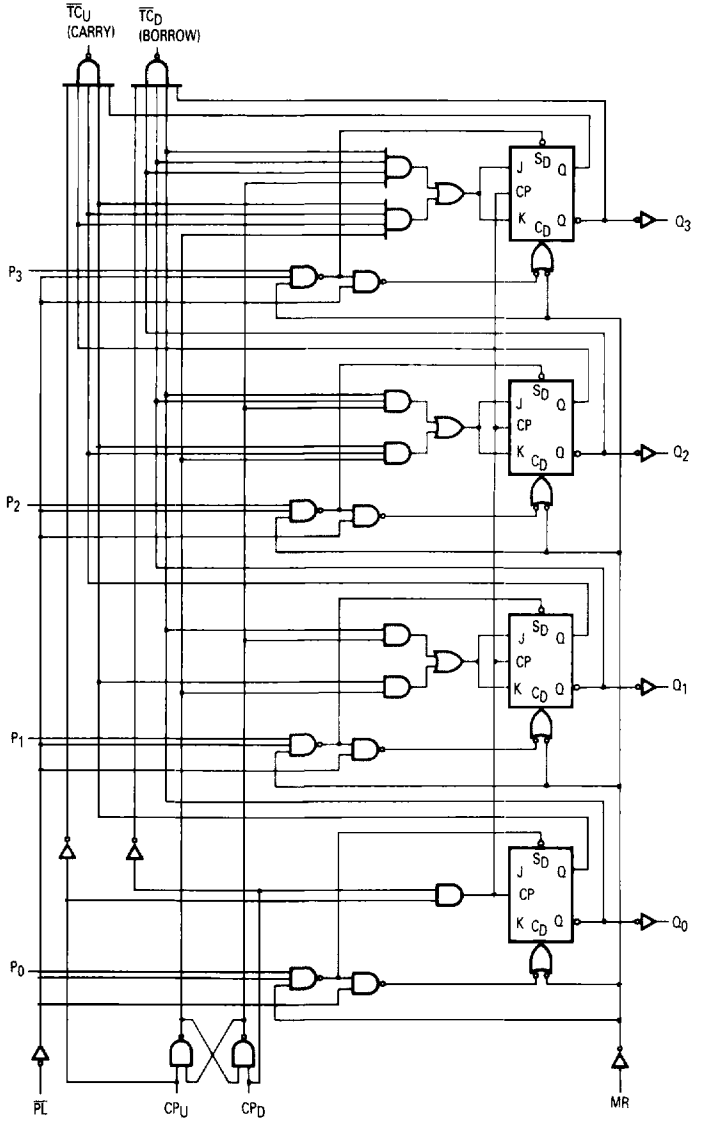
LOGIC DIAGRAM

MC74AC193



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74AC192/74AC193 are asynchronously presettable counters. The MC74AC192 is a decade counter while the MC74AC193 is organized for 4-bit binary operation. They both contain four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state, 9 (MC74AC192) or 15 (MC74AC193), the reset HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot \overline{CP}_U \text{ ('AC192)}$$
$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U \text{ ('AC193)}$$
$$\overline{TC}_U = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

Both the MC74AC192 and the MC74AC193 have an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0–P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

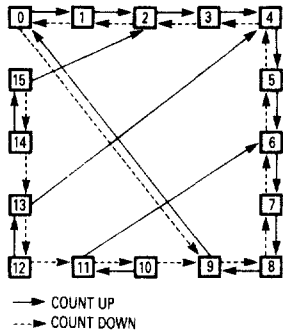
FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

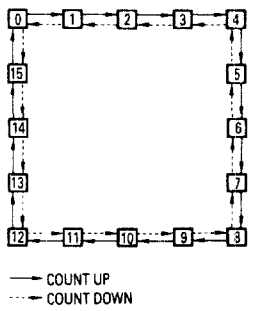
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

STATE DIAGRAMS

MC74AC192



MC74AC193



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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		88 120				MHz	3-3
t_{PLH}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		15 11				ns	3-6
t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		13 9.5				ns	3-6
t_{PLH}	Propagation Delay CP_U or CP_D to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP_U or CP_D to Q_n	3.3 5.0		10.5 7.5				ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		12.5 9.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay MR to Q_n	3.3 5.0		12.5 9.0				ns	3-6
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$	3.3 5.0		12.5 9.0				ns	3-6
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5				ns	3-6
t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	−0.5 −0.5			ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	8.5 6.0			ns	3-6
t_w	CP_U or CP_D Pulse Width, LOW	3.3 5.0	5.5 4.0			ns	3-6
t_w	CP_U or CP_D Pulse Width, LOW (Change of Direction)	3.3 5.0	9.0 6.5			ns	3-6
t_w	MR Pulse Width, HIGH	3.3 5.0	7.0 5.0			ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	3.3 5.0	4.5 3.0			ns	3-9
t_{rec}	Recovery Time MR to CP_U or CP_D	3.3 5.0	8.5 6.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

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