MITSUBISHI BIPOLAR DIGITAL ICs

M54976P

BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

DESCRIPTON

The M54976P is a semiconducnductor integrated circuit fabricated using Bi-CMOS technology. It contains bipolar 8 output drivers of CMOS latch.

FEATURES

- Enable input for output control
- Low supply current ····· $I_{CC} \leqq 10\mu A$ at standby
- Input level is compatible with standard CMOS
- Driver : Withstand voltage ····· $BV_{CEO} \geqq 30$
  Large drive current ····· $(I_{O(max)} = 300mA)$
- Wide operating temperature range ···· $T_a = -20 \sim +75°C$

APPLICATION

Thermal printer head dot driver, Relay driver, Solenoid driver

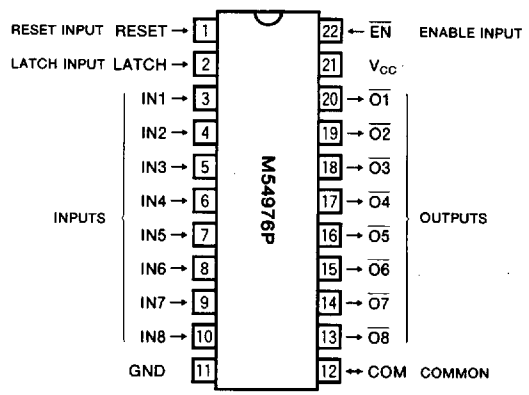
FUNCTION

When data is applied to inputs IN1-IN8 and LATCH input is set to "H", the data will be latchedance with the truth table. Note that when an "H" signal is applied to the RESET input, the latch will maintain the reset state.

When the $\overline{EN}$ input is set to "L" and the data maintained in the latch are "H", the corresponding output will be ON and become "L".

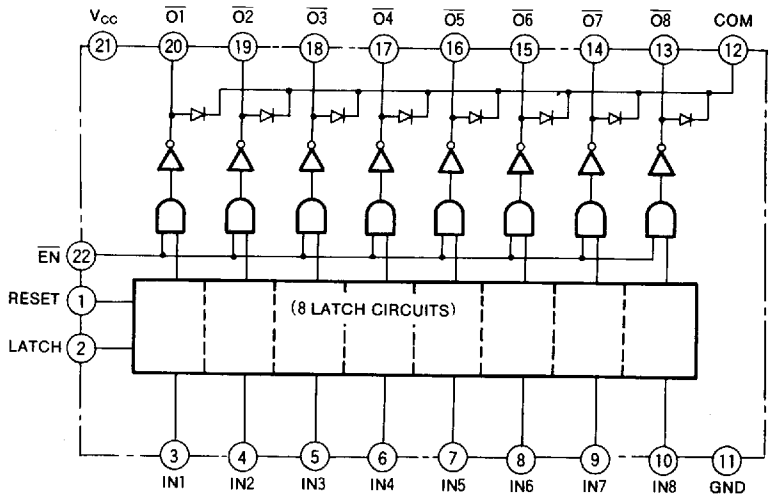
When both the LATCH and RESET inputs are "L", the latch will maintain the prior state irrespective of input signals IN1-IN8.

PIN CONFIGURATION (TOP VIEW)



Outline 22P4

BLOCK DIAGRAM



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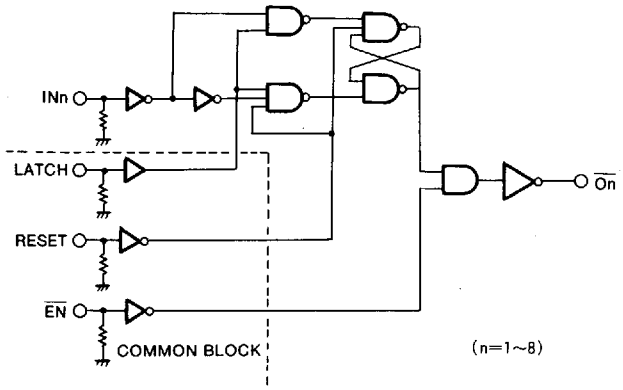
TRUTH TABLE

INPUTS				OUTPUT $\overline{On}$	
INn	LATCH	RESET	$\overline{EN}$	t-1	t
L	H	L	L	X	H
H	H	L	L	X	L
X	X	H	X	X	H
X	X	X	H	X	H
X	L	L	L	L	L
X	L	L	L	H	H

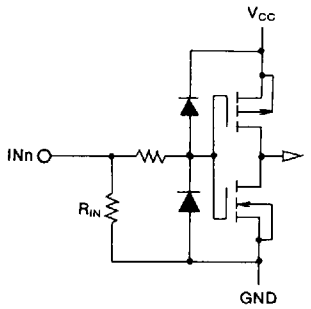
L : "L" level
H : "H" level
X : Irrelevant
t-1 : Previous state
t : Present state
Output H is in the OFF state
Output L is in the ON state

LOGIC DIAGRAM (1 CIRCUIT)

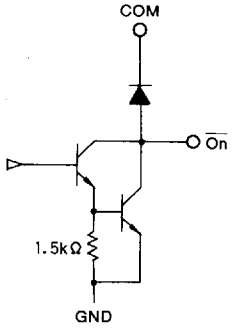


INPUT/OUTPUT EQUIVALENT CIRCUIT SCHEMATICS

1 INPUT CIRCUIT



2 OUTPUT CIRCUIT



BI-CMOS 8-BIT PARALLEL-INPUT, LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (T_a=−20℃~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+8	V
V_I	Input voltage		−0.5~V_{CC}+0.5	V
V_O	Output voltage	Output is OFF	−0.5~+30	V
I_O	Output current	Output is on	350	mA
P_d	Power dissipation	T_a=25℃	1.42	W
Topr	Operating temperature		−20~+75	℃
Tstg	Storage temperature		−55~+125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4	5	6	V
V_O	Applied output voltage	When output is OFF			30	V
I_O	Output current (per circuit)	All outputs ON simultaneously Duty cycle less than 25%			300	mA

ELECTRICAL CHARACTERISTICS (T_a=+25℃, V_{CC}=5V, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	1~10 22	T_a=−20~+75℃	0.7V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.3V_{CC}	V
R_{IN}	Input resistance			50			kΩ
V_{OL1}	Low-level output voltage	13~20	I_{OL}=100mA			1.2	V
V_{OL2}			I_{OL}=200mA			1.4	V
V_{OL3}			I_{OL}=300mA			1.6	V
I_{OLK}	Output leakage current	13~20	V_O=30V			50	μA
V_F	Clamp diode forward current	13~20	I_F=300mA			2	V
I_R	Clamp diode reverse current		V_R=30V			50	μA
I_{CC1}	Supply current	21	All inputs are 0V, all outputs OFF			10	μA
I_{CC2}			Output : 1 circuit ON			1.4	mA

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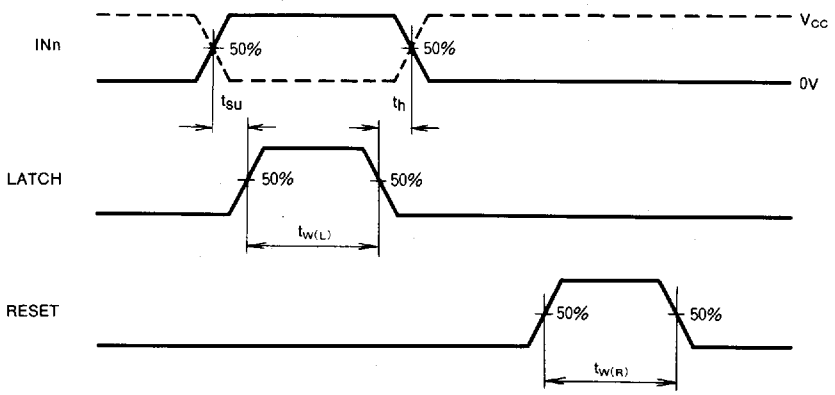
REQUIRED TIMING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(L)}$	Latch pulse width		0.1			μS
$t_{W(R)}$	Reset pulse width		0.1			μS
t_{su}	Data setup time		0			μS
t_h	Data hold time		0.1			μS

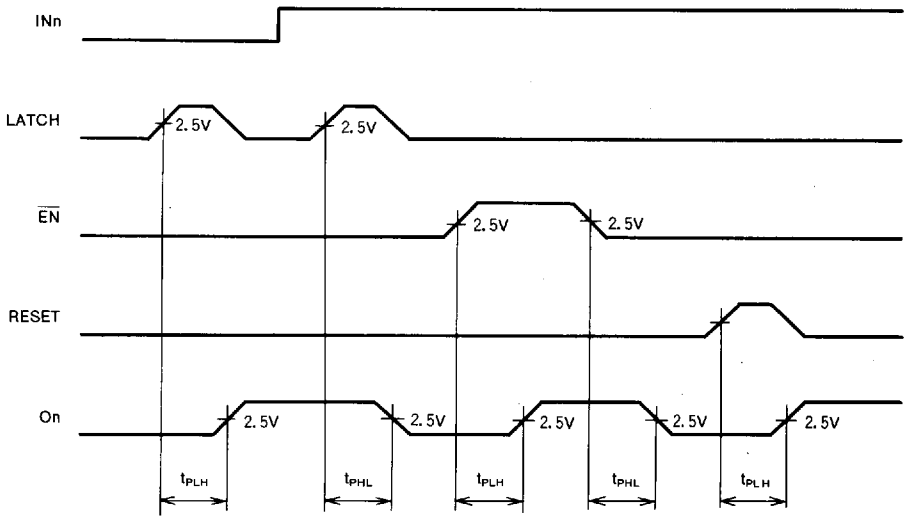
TIMING DIAGRAM



SWITCHING CHARACTERISTICS (T_a=+25℃, V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low to high-level output propagation time (Input LATCH to output $\overline{On}$)	V_{IH}=5V, V_{IL}=0V, R_L=100Ω, C_L=15pF (Note 1)		(0.6)	2	μS
t_{PHL}	High to low-level output propagation time (Input LATCH to output $\overline{On}$)			(0.1)	0.5	μS
t_{PLH}	Low to high-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.6)	2	μS
t_{PHL}	High to low-level output propagation time (Input $\overline{EN}$ to output $\overline{On}$)			(0.1)	0.5	μS
t_{PLH}	Low to high-level output propagation time (Input RESET to output $\overline{On}$)			(0.6)	2	μS

TIMING DIAGRAM



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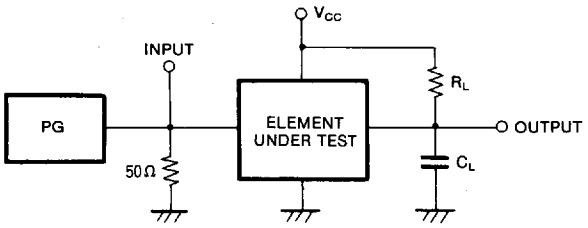
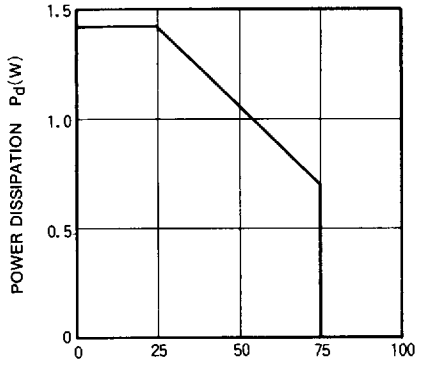
(Note 1) TEST CIRCUIT

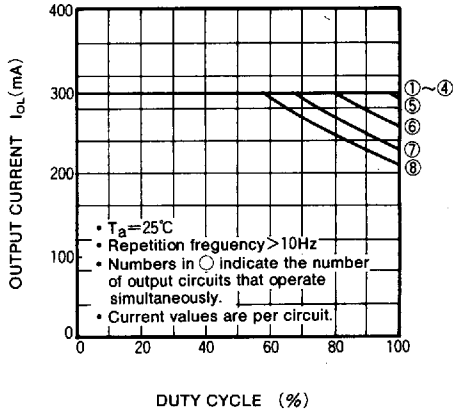


- Input waveform is taken as $t_r \leqq 20ns$ and $t_f \leqq 20ns$
- C_L includes wiring stray capacitance and probe input capacitance.

THERMAL DERATING



DUTY CYCLE VS PERMISSIBLE OUTPUT CURRENT



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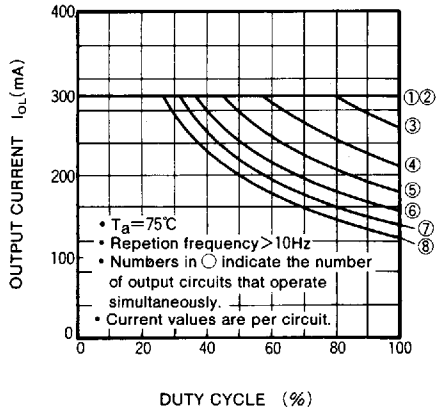

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