Am29203

Four-Bit Bipolar Microprocessor Slice

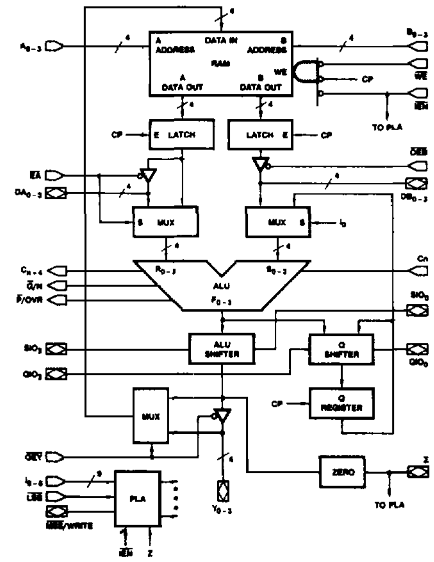
DISTINCTIVE CHARACTERISTICS

- **Expandable Register File –**
  The Am29203 includes the necessary "hooks" to expand the register file externally to any number of registers.
- **Built-in Multiplication Logic –**
  Performing multiplication with the Am2901A requires a few external gates — these gates are contained on-chip in the Am29203. Three special instructions are used for unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.
- **Built-in Division Logic –**
  The Am29203 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- **Built-in Normalization Logic –**
  The mantissa and exponent of a floating-point number can be developed using a single microcycle per shift.
- **Built-in Parity Generation and Sign Extension Circuitry —**
  Can supply parity across the entire ALU outputs and provide sign-extension at any slice boundary.
- **BCD Arithmetic –**
  The Am29203 features automatic BCD add and subtract and conversion between binary and BCD.
- **Two Bidirectional Data Lines**
- **Improved I/O Capability –**
  Both the DA and DB data buses are bidirectional on the Am29203. In addition, the Y port is also bidirectional.

GENERAL DESCRIPTION

The Am29203 is a four-bit expandable bipolar microprocessor slice. The Am29203 performs all functions performed by the industry standard Am2901 and Am2903A, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am29203. In addition to its complete arithmetic and logic instruction set, the Am29203 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, BCD arithmetic and conversion, and other previously time-consuming operations. The Am29203 has three bidirectional ports and features AMD's ion-implanted micro-oxide (IMOX™) technology.

BLOCK DIAGRAM



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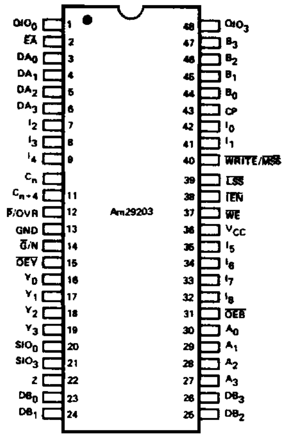
CONNECTION DIAGRAM
Top View

D-48



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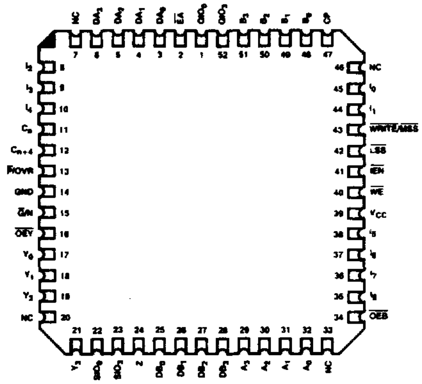

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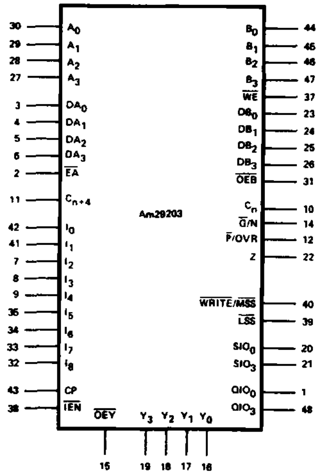
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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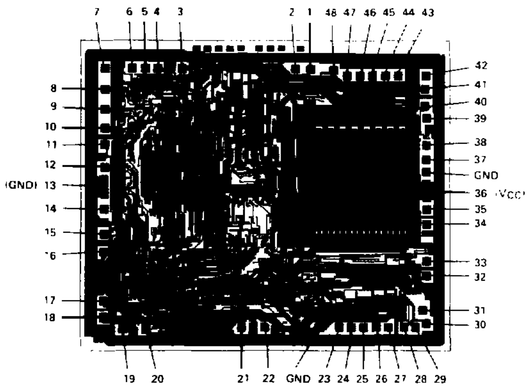
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.163" x 0.197"

Note: Pin numbers correspond to DIP package.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29203 D C B

- B — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- C — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 48-pin CERDIP
  - F – 48-pin flatpak
  - L – 52-pin leadless chip carrier
  - X – Dice
- Am29203 — Device type
  - Bipolar Microprocessor Slice

Valid Combinations	
Am29203	DC, DCB, DMB FMB LC, LMB XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2917A	Bus Transceiver
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am29707	Two-Port RAM
Am27S35	Registered PROM

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Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	A_{0-3}	I	Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.
	B_{0-3}	I	Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.
37	$\overline{WE}$	I	The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
	DA_{0-3}	I/O	A four-bit external data input which can be selected as one of the ALU operand sources; DA_0 is the least significant bit. On the AM29203, the DA path is bidirectional, operating as either an ALU source operand or as an external output for the RAM A-port.
2	$\overline{EA}$	I	A control input which, when HIGH selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
	DB_{0-3}	I/O	A four-bit external data input/output Under control of the $\overline{OEB}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.
31	$\overline{OEB}$	I	A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.
10	C_n	I	The carry-in input to the AM29203 ALU.
	I_{0-8}	I	The nine instruction inputs used to select the Am29203 operation to be performed.
38	$\overline{IEN}$	I	The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the Am29203, $\overline{WRITE}$ is not affected by $\overline{IEN}$, but internally disables the RAM write enable.
11	$C_n + 4$	O	This output generally indicates the carry-out of the Am29203 ALU. Refer to Table 5 for an exact definition of this pin.
14	$\overline{G}$/N	O	A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.
12	$\overline{P}$/OVR	O	A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.
22	Z	I/O	An open-collector input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.
20, 21	SIO_0 SIO_3	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.
1,48	QIO_0 QIO_3	I/O	Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.
39	$\overline{LSS}$	I	An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am29203 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.
40	$\overline{WRITE}/\overline{MSS}$	I/O	When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).
	Y_{0-3}	I/O	Four data inputs/outputs of the Am29203. Under control of the $\overline{OEY}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.
15	$\overline{OEY}$	I	A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.
43	CP	I	The clock input to the Am29203. The Q register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

ARCHITECTURE OF THE Am29203

The Am29203 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPUs, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am29203 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am29203 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OEB}$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port. On the Am29203, $\overline{EA}$ provides the same feature at the DA port.

External data at the Am29203 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto to Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am29203 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{EA}$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OEB}$ and I_0 inputs select RAM output port B, DB external data input, or the Q register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am29203 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table 1 shows all possible pairs of ALU source operands as a function of the $\overline{EA}$, $\overline{OEB}$, and I_0 inputs.

TABLE 1. ALU OPERAND SOURCES

$\overline{EA}$	I_0	$\overline{OEB}$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	Ram Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	Ram Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW
H = HIGH
X = Don't Care

TABLE 2. Am29203 ALU FUNCTIONS

I_4	I_3	I_2	I_1	I_0	ALU Functions
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	F = S Minus R Minus 1 Plus C_n
L	L	H	L	X	F = R Minus S Minus 1 Plus C_n
L	L	H	H	X	F = R Plus S Plus C_n
L	H	L	L	X	F = S Plus C_n
L	H	L	H	X	F = $\overline{S}$ Plus C_n
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	F = R Plus C_n
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	F = $\overline{R}$ Plus C_n
H	L	L	L	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	F_i = $\overline{R_i}$ AND S_i
H	L	H	L	X	F_i = R_i EXCLUSIVE NOR S_i
H	L	H	H	X	F_i = R_i EXCLUSIVE OR S_i
H	H	L	L	X	F_i = R_i AND S_i
H	H	L	H	X	F_i = R_i NOR S_i
H	H	H	L	X	F_i = R_i NAND S_i
H	H	H	H	X	F_i = R_i OR S_i

L = LOW
H = HIGH
i = 0 to 3
X = LOW or HIGH

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am29203 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am29203 executes instructions other than the 16 special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Am29203s may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am29203s are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, G, and carry propagate, P, signals required for a lookahead carry scheme are generated by the Am29203 and are available as outputs of the least significant and intermediate slices.

The Am29203 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. *The ALU generates two other status outputs. These are* negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am29203 instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data *through this bit position (see Figure A). SIO_0 and SIO_3 are* bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am29203 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am29203 applications section for a more detailed description of the Am29203 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am29203 executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations;

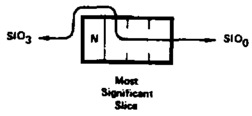
however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the Am29203. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q register.

The Q register and shifter are controlled by the instruction inputs. Table 4 defines the Am29203 special functions and the operations which the Q register and shifter perform for each. When the Am29203 executes instructions other than the special functions, the Q register and shifter operation is controlled by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the Q register and shifter operation as a function of these four bits.

Figure A.

Am29203 Arithmetic Shift Path



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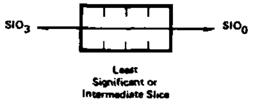

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Am29203 Logical Shift Path

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TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, IEN = LOW

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{WRITE}$	Q Reg & Shifter Function	QIO_3	QIO_0
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \nabla F_2 \nabla F_1 \nabla F_0$ SIO_3
∇ = Exclusive OR
L = LOW
H = HIGH
Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTONS (Note 7)

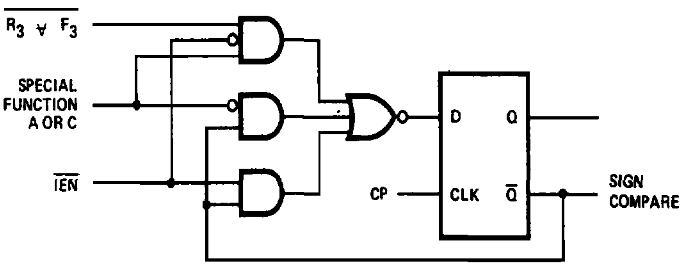
(Hex) $I_8I_7I_6I_5$	I_4	(Hex) $I_3I_2I_1I_0$	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig/ Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
0	L	0	Unsigned Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log F/2 → Y (Note 1)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
1	L	0	BCD to Binary Conversion	(Note 4)	Log F/2 → Y	Input	Input	F_0	Log Q/2 → Q	Input	Q_0	L
1	H	0	Multiprecision BCD to Binary	(Note 4)	Log F/2 → Y	Input	Input	F_0	HOLD	Z	Q_0	L
2	L	0	Two's Complement Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
3	L	0	Decrement by One or Two	$F = S - 2 + C_n$	F → Y	Z	Z	Parity	Hold	Z	Z	L
4	L	0	Increment by One or Two	$F = S + 1 + C_n$	F → Y	Input	Input	Parity	Hold	Z	Z	L
5	L	0	Sign/Magnitude Two's Complement	$F = S + C_n$ if $Z = L$ $F = \overline{S} + C_n$ if $Z = H$	F → Y (Note 3)	Input	Input	Parity	Hold	Z	Z	L
6	L	0	Two's Complement Multiply, Last Cycle	$F = S + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
7	L	0	BCD Divide by Two	(Note 4)	F → Y	Z	Z	Parity	Hold	Z	Z	L
8	L	0	Single Length Normalize	$F = S + C_n$	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
9	L	0	Binary to BCD Conversion	(Note 5)	Log 2F → Y	F_3	F_3	Input	Log 2Q → Q	Q_3	Input	L
9	H	0	Multiprecision Binary to BCD	(Note 5)	Log 2F → Y	F_3	F_3	Input	Hold	Z	Input	L
A	L	0	Double Length Normalize and First Divide Op	$F = S + C_n$	Log 2F → Y	$R_3 \nabla F_3$	F_3	Input	Log 2Q → Q	Q_3	Input	L
B	L	0	BCD Add	$F = R + S + C_n$BCD (Note 6)	F → Y	0	0	Z	Hold	Z	Z	L
C	L	0	Two's Complement Divide	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log 2F → Y	$\overline{R_3 \nabla F}$	F_3	Input	Log 2Q → Q	Q_3	Input	L
D	L	0	BCD Subtract	$F = R - S - 1 + C_n$ BCD (Note 6)	F → Y	0	0	Z	Hold	Z	Z	L
E	L	0	Two's Complement Divide Correction and Remainder	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
F	L	0	BCD Subtract	$F = S - R - 1 + C_n$ BCD (Note 6)	F → Y	0	0	Z	Hold	Z	Z	L

Notes:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \nabla$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \nabla F_3$ is generated at the Y_3 output.
4. On each slice, F = S if magnitude of S_{0-3} is less than 8 and F = S minus 3 if magnitude of S_{0-3} is 8 or greater.
5. On each slice, F = S if magnitude of S_{0-3} is less than 5 and F = S plus 3 if magnitude of S_{0-3} is 5 or greater. Addition is module 16.
6. Additions and subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.

L = LOW
H = HIGH
X = Don't Care

Hi-Z = High Impedance
∇ = Exclusive OR
Parity = $SIO_3 \nabla F_3 \nabla F_2 \nabla F_1 \nabla F_0$

Figure B. Sign Compare Flip-Flop



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The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

Output Buffers

The DB, DA, and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls.

The Y output buffers are enabled when the $\overline{OEY}$ input is LOW and are in the high impedance state when $\overline{OEY}$ is HIGH. The DB output buffers are enabled when the $\overline{OEB}$ input is LOW and the DA buffers are enabled when $\overline{EA}$ is LOW.

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am29203 instructions. On the Am29203, the Z pin will be HIGH if $\overline{OEY}$ is HIGH, allowing zero detection on less than the full word.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}/\overline{MSS}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am29203 instruction inputs.

On the Am29203, when $\overline{IEN}$ is HIGH, the Q register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the Q register and Sign Compare Flip-Flop can be written according to the Am29203 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am29203 divide operation (see Figure B). On the Am29203, $\overline{IEN}$ controls internal writing, but does not affect $\overline{WRITE}$. The $\overline{IEN}$ signal can then be controlled separately at each chip to facilitate byte operations.

Programming the Am29203 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}/\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}/\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{W}/\overline{MSS}$ pin must be tied HIGH through a resistor. $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ should not be connected together.

Am29203 SPECIAL FUNCTIONS

The Am29203 provides 16 Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation and Decrementation by One or Two
- BCD add, subtract, and divide by two.
- Single-and double-precision BCD to Binary and Binary to BCD conversion.

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am29203. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

The BCD arithmetic special functions can be used to add or subtract two BCD numbers and generate a valid BCD result in one microcycle. In addition a BCD divide by two adjust instruction can be used to obtain a valid BCD representation after shifting a number down by one bit.

The BCD/Binary conversion special function instructions facilitate single- and double-precision algorithms to convert from BCD to Binary and from Binary to BCD.

Refer to Am29203 applications section for a more detailed description of these Special Functions.

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	Gi (i = 0 to 3)	Pi (i = 0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		X ($\overline{OEY}$ = L)		
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Intermediate Slice	Least Sig. Slice
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	1	X	$\overline{R_i} \wedge S_i$	$\overline{R_i} \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	2	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	5	X	0	$\overline{S_i}$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	7	X	0	$\overline{R_i}$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	8	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	9	X	$\overline{R_i} \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	B	X	$\overline{R_i} \wedge S_i$	$\overline{R_i} \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	D	X	$\overline{R_i} \wedge \overline{S_i}$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
X	F	X	$\overline{R_i} \wedge \overline{S_i}$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
1	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)	(Note 7)	$G \vee PC_n$	$C_{n+3} \nabla C_{N+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
4	0	L	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \nabla C_{N+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
5	0	L	0	S_i if Z = L $\overline{S_i}$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \nabla S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $\overline{R_i} \wedge S_i$ if Z = H	S_i if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
8	0	L	0	S_i	(Note 3)	$Q_2 \nabla Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$
9	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$
9	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$	$\overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$
A	0	L	0	S_i	(Note 4)	$F_2 \nabla F_1$	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	(Note 8)	(Note 8)	(Note 9)	(Note 9)	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R_i} \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	$R_i \wedge \overline{S_i}$	$R_i \vee \overline{S_i}$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R_i} \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	$\overline{R_i} \wedge S_i$	$\overline{R_i} \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$	$\overline{Y_0}\ \overline{Y_1}\ \overline{Y_2}\ \overline{Y_3}$

Notes:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_i = S_i$
3. At the most significant slice, $C_{n+4} = Q_3 \nabla Q_2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \nabla F_2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}\ \overline{F_0}\ \overline{F_1}\ \overline{F_2}\ \overline{F_3}$.
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = S_{0,1,2,3}$.
7. If $\overline{LSS}$ is LOW, $P_0 = S_0$ and $P_{1,2,3} = 1$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3} = 1$.
8. On all slices $\overline{P} = (\overline{P_0} + \overline{P_3})\ (\overline{P_0} + \overline{G_2})\ (\overline{P_0} + \overline{G_1} + \overline{P_2})$.
9. On all slices $\overline{G} = \overline{G_3}\ (\overline{G_0} + \overline{G_1} + \overline{P_2})\ (\overline{G_0} + \overline{G_1})\ (\overline{P_1} + \overline{G_2})\ (\overline{P_3} + \overline{P_1} \cdot \overline{P}_2 \cdot \overline{G_0})$.

L = LOW = 0
H = HIGH = 1
$\vee$ = OR
$\wedge$ = AND
∇ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3\ G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1\ P_2$

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Refer to Page 13-1 for Essential Information on Military Devices

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C
Ambient Temperature Under Bias .... −55°C to +125°C
Supply Voltage to Ground Potential
  Continuous .... −0.5V to +7.0V
DC Voltage Applied to Outputs For
  High Output State .... −0.5V to $+V_{CC}$ max
DC Input Voltage .... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current .... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
  Temperature .... 0°C to +70°C
  Supply Voltage .... +4.75V to +5.25V
Military (M) Devices
  Temperature .... −55°C to +125°C
  Supply Voltage .... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N	2.4			Volts
				I_{OH} = −800µA $DB_{0\text{-}3}$, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}	2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN, V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA(COM'L) I_{OL} = 16mA(MIL)			0.5	Volts
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA(COM'L) I_{OL} = 8.0mA(MIL)			0.5	
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, $\overline{WRITE}$ SIO_3, QIO_0 QIO_3, SIO_0	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V (Note 4)		C_n			−3.6	mA
				Y_0, Y_1, Y_2, Y_3			−1.13	
				I_0, I_1, I_2, I_3, I_4 DA_0, DA_1, DA_2, DA_3			−0.72	
				SIO_0, SIO_3, QIO_0, $\overline{MSS}$ QIO_3, DB_0, DB_1, DB_2, DB_3			−0.77	
				All other inputs			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V (Note 4)		C_n			200	µA
				Y_0, Y_1, Y_2, Y_3			110	
				I_0-I_4, DA_0-DA_3			40	
				SIO_0, SIO_3, $\overline{MSS}$ QIO_3, $DB_{0\text{-}3}$, QIO_0			90	
				All other inputs			20	

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Refer to Page 13-1 for Essential Information on Military Devices

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX, (Note 4)	$Y_0 - Y_3$	V_O = 2.4V			110	μA
				V_O = 0.5V			−1130	
			DB_{0-3}, QIO_0, QIO_3, SIO_0, SIO_3, $\overline{WRITE}$/$\overline{MSS}$	V_O = 2.4V			90	
				V_O = 0.5V			−770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX	COM'L	T_A = 0 to 70°C			350	mA
				T_A = 70°C			291	
			MIL	T_C = −55 to 125°C			395	
				T_C = 125°C			258	

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC}=5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$, and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worse case I_{CC} is at minimum temperature.
6. Three input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).

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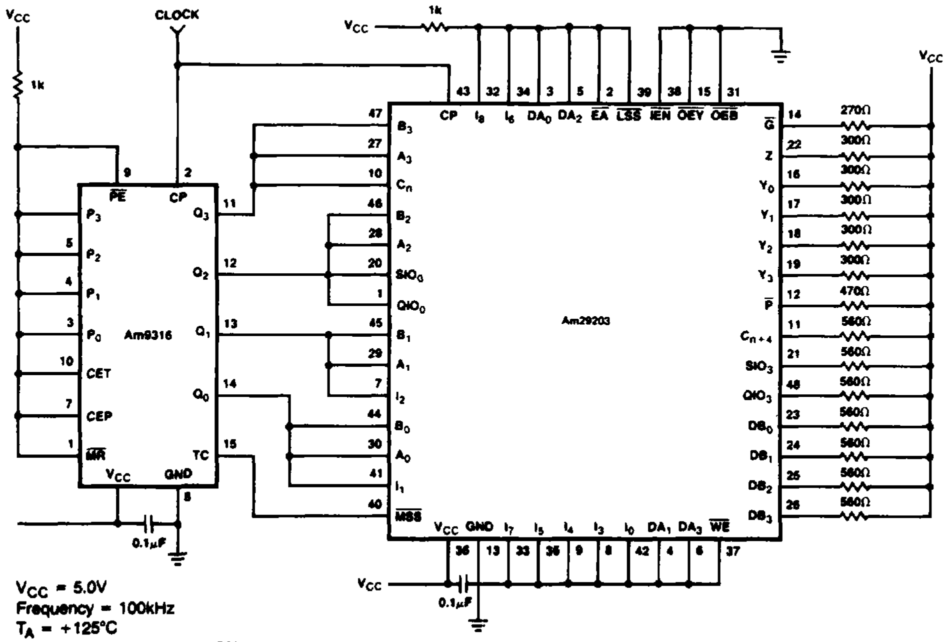
Refer to Page 13-1 for Essential Information on Military Devices

Am29203 Burn-in and Life Test Circuit



V_{CC} = 5.0V
Frequency = 100kHz
T_A = +125°C
All registers are 1/4 watt ±5%
This circuit conforms to MIL-STD-883, Methods 1005 and 1015, Condition D.
One Am9316 Can Drive Maximum of Five Am29203s.

TC001520

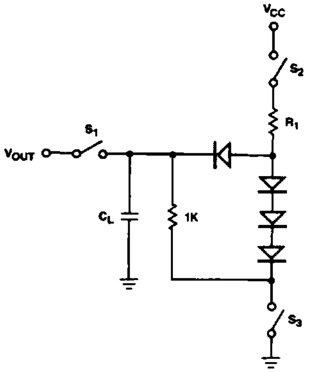
Notes on Testing

Incoming test procedures on this device should be carefully planned taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current when the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3.0V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function and AC tests as three distinct groups of tests.
6. To assist in testing AMD, offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

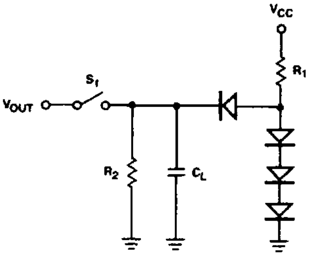
SWITCHING TEST CIRCUIT

A. THREE-STATE OUTPUTS



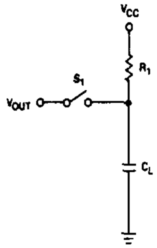
TC001430

B. NORMAL OUTPUTS



TC001380

C. OPEN-COLLECTOR OUTPUTS



TC001420

$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{1K}} \qquad R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{R_2}} \qquad R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in hand in test fixture.
2. S_1, S_2, S_3 are closed during function test and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. *C_L = 5.0pF for output disable tests.*

TEST OUTPUT LOADS FOR Am29203

Pin #	Pin Label	Test Circuit	R_1	R_2
1	QIO_0	A	458	1K
11	C_{n+4}	B	478	3K
12	$\overline{P}$/OVR	B	383	3K
14	$\overline{G}$/N	B	212	1.5K
16–19	Y_{0-3}	A	241	1K
20	SIO_0	A	458	1K
21	SIO_3	A	458	1K
22	Z	C	281	–
23–26	DB_{0-3}	A	458	1K
40	$\overline{WRITE}/\overline{MSS}$	A	458	1K
48	QIO_3	A	458	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

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Am290203 GUARANTEED COMMERCIAL RANGE PERFORMACE

The Am290203 switching characteristics are a function of the power supply voltage, the temperature, and the operating mode of the devices. The data has been condensed onto the tables below.

INDEX TO SWITCHING TABLES

Table	Data Type	Conditions	Applicable To
A	Clock and Write Pulse	4.75 to 5.25V, 0 to 70°C	All Functions
B	Enable/Disable Times	4.75 to 5.25V, 0 to 70°C	All Functions
C	Setup and Hold Times	4.75 to 5.25V, 0 to 70°C	All Functions
I-2	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Standard and Increment/Decrement by 1 or 2
I-3	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Multiply Instructions
I-4	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Divide Instructions
I-5	Combinational Delays	4.75 to 5.25V, 0 to 70°C	BCD Instructions
I-6	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Sign Magnitude to Two's Complement Conversion
I-7	Combinational Delays	4.75 to 5.25V, 0 to 70°C	Single Length Normalization

Am29203 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am29203 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE A. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Time CP and $\overline{WE}$ both LOW to Write	15ns

TABLE B. ENABLE/DISABLE TIMES ALL FUNCTIONS

From	To	Enable	Disable
$\overline{OEY}$	Y	25	21
$\overline{OEB}$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
I_{8765}	QIO	38	38
I_{43210}	QIO	38	38
$\overline{LSS}$	$\overline{WR}$	25	21

Note: C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

COMBINATIONAL PROPAGATION DELAYS C_L = 50pF
1-2 STANDARD AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS

	To											
From	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA, DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 Parity
A, B Addr	67	55	52	74	64	71	30	–	–	44	62	84
DA, DB	58	50	44	65	54	60	–	–	–	35	59	68
C_n	30	18	–	35	26	26	–	–	–	21	27	40
I_{8-0}	64	64	50	72	59	62	–	34	26	48	62	74
CK	58	42	43	61	54	60	21	–	21	35	54	65
$\overline{MSS}$	33	–	41	40	36	44	–	–	–	40	40	44
$SIO_{0,3}$	23	–	–	29	–	–	–	–	–	–	29	19

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Refer to Page 13-1 for Essential Information on Military Devices

TABLE C. SET-UP AND HOLD TIMES ALL FUNCTIONS

From	With Respect to	HIGH-to-LOW Set-up	HIGH-to-LOW Hold	LOW-to-HIGH Set-up	LOW-to-HIGH Hold	Comments
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q
$\overline{WE}$ HIGH	CP	15	Tpwl		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	Tpwl		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
I_{8765}	CP	28	Tpwl		0	
$\overline{IEN}$ HIGH	CP	24	Tpwl		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
I_{43210}	CP	24	Tpwl		0	

Note: 1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OEY}$ = 0).

1–5 BCD INSTRUCTIONS (SF 1, SF 7, SF 9, SF B, SF D, SF F)

From	Slice	To: Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA DB	$\overline{WR}$	QIO	SIO_0	SIO_3	SIO Parity
A, B Addr	MSS	77	55	–	72	68	68	30	–	–	44	62	84
	IS	77	55	61	72	–	–	30	–	–	44	62	84
	LSS	77	55	61	72	–	–	30	–	–	44	62	84
DA, DB	MSS	61	50	–	65	58	59	–	–	–	35	59	68
	IS	61	50	49	65	–	–	–	–	–	35	59	68
	LSS	61	50	49	65	–	–	–	–	–	35	59	68
C_n	MSS	36	23	–	35	33	33	–	–	–	29	34	40
	IS	36	23	–	35	–	–	–	–	–	29	34	40
	LSS	36	23	–	35	–	–	–	–	–	29	34	40
I_{8-0}	MSS	72	64	–	72	59	62	–	–	26	48	62	74
	IS	72	64	60	72	–	–	–	–	26	48	62	74
	LSS	72	64	60	72	–	–	–	34	26	48	62	74
CK	MSS	68	52	–	68/29[1]	64	60	21	–	21	35	54	65
	IS	68	52	55	68/29[1]	–	–	21	–	21	35	54	65
	LSS	68	52	55	68/29[1]	–	–	21	–	21	35	54	65
Z	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–	–	–

Note 1: Binary to BCD and multiprecision Binary to BCD instructions only.

BCD to Binary conversion (SF 1)
BCD divide by two (SF 7)
Binary to BCD conversion (SF 9)
BCD add (SF B)
BCD substract (SF D, SF F)

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Guaranteed Combinational Delays
$T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to $5.25V$
1-3 MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

From	To											
	Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA DB	$\overline{WR}$	QIO_0	SIO_0	SIO Parity
A, B Addr	MSS	67	55	–	–	64	71	30	–	–	44	–
	IS	67	55	52	–	–	–	30	–	–	44	–
	LSS	67	55	52	–	–	–	30	–	–	44	–
DA, DB	MSS	59	50	–	–	54	60	–	–	–	35	–
	IS	58	50	44	–	–	–	–	–	–	35	–
	LSS	58	50	44	–	–	–	–	–	–	35	–
C_n	MSS	34	18	–	–	26	26	–	–	–	21	–
	IS	30	18	–	–	–	–	–	–	–	21	–
	LSS	30	18	–	–	–	–	–	–	–	21	–
I_{8-0}	MSS	104	76	–	–	90	96	–	–	26	68	–
	IS	91	76	74	–	–	–	–	–	26	68	–
	LSS	91	76	74	31	–	–	–	34	26	68	–
CK	MSS	62	42	–	–	54	60	21	–	21	35	–
	IS	58	42	43	–	–	–	21	–	21	35	–
	LSS	95	79	79	29	–	–	21	–	21	71	–
Z	MSS	72	50	–	–	64	64	–	–	–	42	–
	IS	66	50	50	–	–	–	–	–	–	42	–
	LSS	–	–	–	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–	–

Unsigned Multiply

SF 0: $F = S + Cn$ if $Z = L$
$F = S + R + Cn$ if $Z = H$
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply

SF 2: $F = S + Cn$ if $Z = L$
$F = R + S + Cn$ if $Z = H$
$Y_3 = F_3 \nabla OVR$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle

SF 6: $F = S + Cn$ if $Z = L$
$F = S - R - 1 + Cn$ if $Z = H$
$Y_3 = OVR \nabla F_3$ (MSS)
$Z = Q_0$ (LSS)

Guaranteed Combinational Delays
$T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to $5.25V$
1-2 STANDARD AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF 3 and SF 4)

From	To											
	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA, DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 Parity
A, B Addr	67	55	52	74	64	71	30	–	–	44	62	84
DA, DB	58	50	44	65	54	60	–	–	–	35	59	68
C_n	30	18	–	35	26	26	–	–	–	21	27	40
I_{8-0}	64	64	50	72	59	62	–	34	26	48	62	74
CK	58	42	43	61	54	60	21	–	21	35	54	65
$\overline{MSS}$	33	–	41	40	36	44	–	–	–	40	40	44
$SIO_{0,3}$	23	–	–	29	–	–	–	–	–	–	29	19

Decrement SF3: $F = S - 2 + C_n$

Increment SF4: $F = S + 1 + C_n$

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Guaranteed Combinational Delays
$T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to $5.25V$
1-6 SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

		To										
From	Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA DB	$\overline{WR}$	QIO	$\overline{SIO}$	SIO_0 Parity
A,B Addr	MSS	98	88	–	42	97	104	30	–	–	–	132
	IS	67	55	52	–	–	–	30	–	–	–	84
	LSS	67	55	52	–	–	–	30	–	–	–	84
DA, DB	MSS	93	83	–	37	92	99	–	–	–	–	127
	IS	58	50	44	–	–	–	–	–	–	–	68
	LSS	58	50	44	–	–	–	–	–	–	–	68
C_n	MSS	30	18	–	–	29	26	–	–	–	–	40
	IS	30	18	–	–	–	–	–	–	–	–	40
	LSS	30	18	–	–	–	–	–	–	–	–	40
I_{8-0}	MSS	89	73	–	28	91	84	–	–	–	–	118
	IS	86	73	72	–	–	–	–	–	–	–	96
	LSS	86	73	72	–	–	–	–	34	–	–	96
CK	MSS	96	82	–	36	89	98	21	–	–	–	126
	IS	58	42	43	–	–	–	21	–	–	–	65
	LSS	58	42	43	–	–	–	21	–	–	–	65
Z	MSS	–	–	–	–	–	–	–	–	–	–	–
	IS	62	46	44	–	–	–	–	–	–	–	90
	LSS	62	46	44	–	–	–	–	–	–	–	90
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	–	–	–	–	–	–	–	–	–	–	–

SF 5:
F = $S + C_n$ if Z = L
F = $\overline{S} + C_n$ if Z = H
Y_3 = $S_3 \nabla F_3$ (MSS)
Z = S_3 (MSS)

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Refer to Page 13-1 for Essential Information on Military Devices

Guaranteed Combinational Delays
$T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to $5.25V$
1-7 SINGLE LENGTH NORMALIZATION (SF 8)

From		To										
	Slice	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA DB	$\overline{WR}$	QIO_3	SIO_3	SIO Parity
A,B Addr	MSS	67	–	–	–	–	–	30	–	–	62	–
	IS	67	55	52	–	–	–	30	–	–	62	–
	LSS	67	55	52	–	–	–	30	–	–	62	–
DA, DB	MSS	58	–	–	–	–	–	–	–	–	59	–
	IS	58	50	44	–	–	–	–	–	–	59	–
	LSS	58	50	44	–	–	–	–	–	–	59	–
C_n	MSS	30	–	–	–	–	–	–	–	–	27	–
	IS	30	18	–	–	–	–	–	–	–	27	–
	LSS	30	18	–	–	–	–	–	–	–	27	–
I_{0-5}	MSS	55	46	–	29	24	25	–	–	26	60	–
	IS	52	50	30	29	–	–	–	–	26	54	–
	LSS	52	50	30	29	–	–	–	34	26	54	–
CK	MSS	58	26	–	29	23	27	21	–	21	54	–
	IS	58	42	43	29	–	–	21	–	21	54	–
	LSS	58	42	43	29	–	–	21	–	21	54	–
Z	MSS	–	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	–	–	–	–	–	–	–	–	–	–	–

SF 8:

F $= S + C_n$

N $= Q_3(MSS)$

C_{n+4} $= Q_3 \nabla Q_2(MSS)$

OVR $= Q_2 \nabla Q_1(MSS)$

Z $= \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}$

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Guaranteed Combinational Delays
$T_A = 0$ to $+70°C$, $V_{CC} = 4.75$ to $5.25V$
1–4 DIVIDE INSTRUCTIONS (SF A, SF C, SF E)

From	To											
	Slice	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	SIO_3	DA, DB	QIO_3	$\overline{WR}$	SIO Parity
A, B Addr	MSS	67	55/60[1]	–	74	64	71	30	–	–	62	–
	IS	67	55	52	74	–	–	30	–	–	62	–
	LSS	67	55	52	74	–	–	30	–	–	62	–
DA, DB	MSS	58	50/55[1]	–	65	54	60	–	–	–	59	–
	IS	58	50	44	65	–	–	–	–	–	59	–
	LSS	58	50	44	65	–	–	–	–	–	59	–
C_n	MSS	30	18/41[1]	–	35	26	26	–	–	–	30/27[1]	–
	IS	30	18	–	35	–	–	–	–	–	27	–
	LSS	30	18	–	35	–	–	–	–	–	27	–
I_{8-0}	MSS	80/55[1]	75	–	47[1]/31[2]	77	77	–	–	26	90/71[1]	–
	IS	80/55[1]	75	–	47[1]	–	–	–	–	26	85/52[1]	–
	LSS	80/55[1]	75	–	47[1]	–	–	–	34	26	85/52[1]	–
CK	MSS	58[1]/89[2]	50[1]/73[2]	–	61[1]/29[2]	54[1]/92[2]	60[1]/92[2]	21	–	21	87[2]/54[1]	–
	IS	58	42	43	61[1]	–	–	21	–	21	54	–
	LSS	58	42	43	61[1]	–	–	21	–	21	54	–
Z	MSS	–	–	–	–	–	–	–	–	–	–	–
	IS	61	44	46	–	–	–	–	–	–	58	–
	LSS	61	44	46	–	–	–	–	–	–	58	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	–	–	–	–
SIO_{0-3}	Any	23	–	–	–	–	–	–	–	–	–	–

Notes:
1. Only 1st divide and normalization.
2. Only two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op

SF A:
$F = S + CN$
$N = F_3$ (MSS)
$SIO_3 = F_3 \nabla R_3$ (MSS)
$C_{n+4} = F_3 \nabla F_2$ (MSS),
$OVR = F_2 \nabla F_1$ (MSS)
$Z = \overline{Q_0}\ \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}\ \overline{F_0}\ \overline{F_1}\ \overline{F_2}\ \overline{F_3}$

Two's Complement Divide

SF C:
$F = R + S + Cn$ if $Z = L$
$F = S - R - 1 + Cn$ if $Z = H$
$SIO_3 = \overline{F_3 \nabla R_3}$ (MSS)
$Z = \overline{F_3 \nabla R_3}$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder

SF E:
$F = R + S + Cn$ if $Z = L$
$F = S - R - 1 + Cn$ if $Z = H$
$Z = \overline{F_3 \nabla R_3}$ (MSS) from previous cycle

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Refer to Page 13-1 for Essential Information on Military Devices