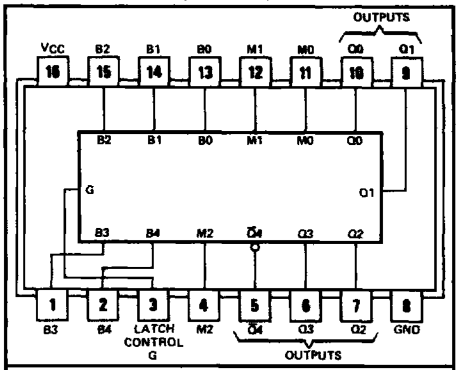
TYPES SN54LS261, SN74LS261
2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

BULLETIN NO. DL-S 7612123, MARCH 1974—REVISED OCTOBER 1976

- Fast Multiplication . . . 5-Bit Product in 26 ns Typ
- Power Dissipation . . . 110 mW Typical
- Latch Outputs for Synchronous Operation
- Expandable for m-Bit-by-n-Bit Applications
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families
- Diode-Clamped Inputs Simplify System Design

SN54LS261 . . . J OR W PACKAGE
SN74LS261 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

description

These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most-significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

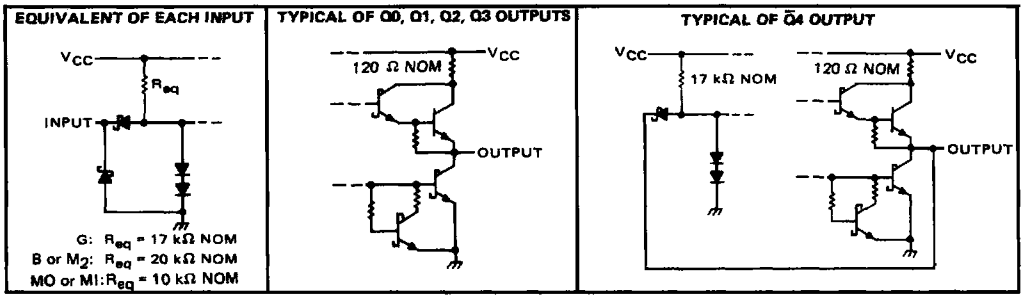
The SN54LS261 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS261 for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER M2	M1	M0	$\overline{Q4}$	Q3	Q2	Q1	Q0
L	X	X	X	$\overline{Q4}_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\overline{B4}$	B4	B3	B2	B1
H	L	H	L	$\overline{B4}$	B4	B3	B2	B1
H	L	H	H	$\overline{B4}$	B3	B2	B1	B0
H	H	L	L	B4	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$	$\overline{B0}$
H	H	L	H	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	L	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant
$\overline{Q4}_0$ . . . $Q0_0$ = The logic level of the same output before the high-to-low transition of G.
B4 . . . B0 = The logic level of the indicated multiplicand (B) input.

schematics of inputs and outputs



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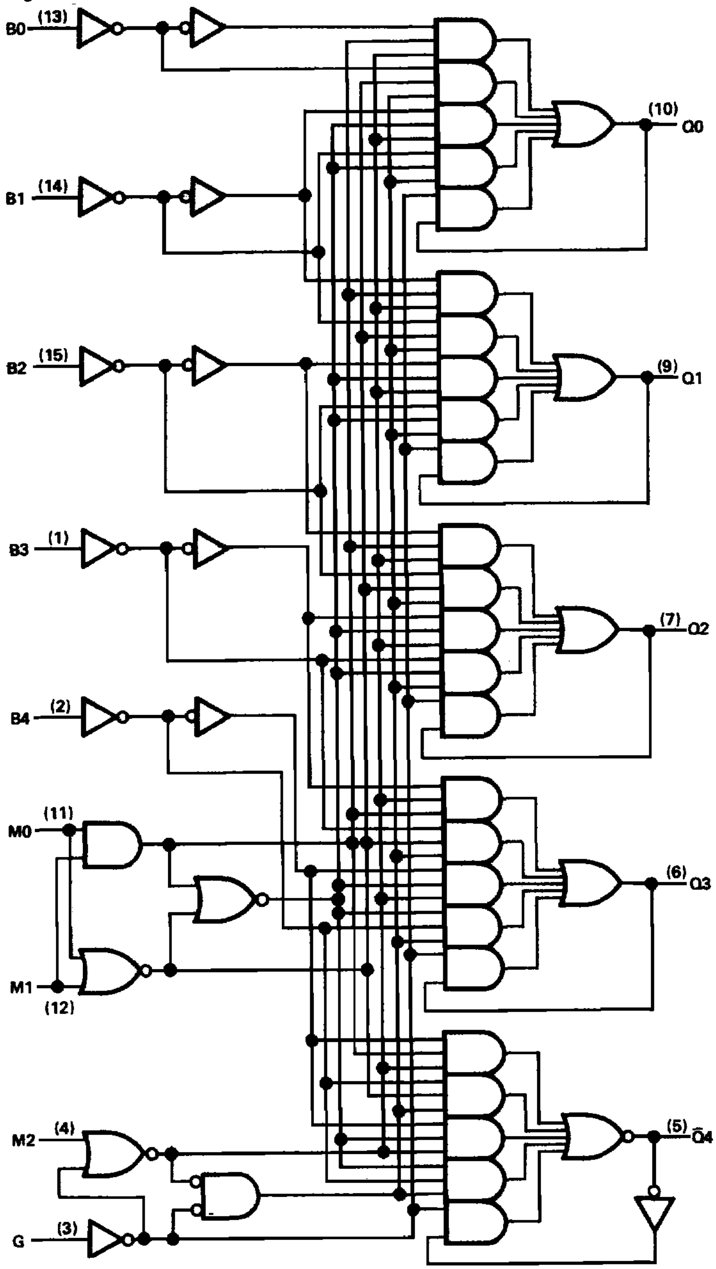
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS261	−55°C to 125°C
SN74LS261	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS261 MIN	SN54LS261 NOM	SN54LS261 MAX	SN74LS261 MIN	SN74LS261 NOM	SN74LS261 MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Width of enable pulse, t_w		25			25			ns
Setup time, t_{su}	Any M input	17↓			17↓			ns
	Any B input	15↓			15↓			
Hold time, t_h	Any M input	0↓			0↓			ns
	Any B input	0↓			0↓			
Operating free-air temperature, T_A		−55		125	0		70	°C

↓The arrow indicates that the falling edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS261 MIN	SN54LS261 TYP‡	SN54LS261 MAX	SN74LS261 MIN	SN74LS261 TYP‡	SN74LS261 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V	MO or MI			0.2			0.2	mA
			All others			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	MO or MI			40			40	μA
			All others			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	MO or MI			−0.8			−0.8	mA
			All others			−0.4			−0.4	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs at 0 V, Outputs open.		22		38		20	40	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the output short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable G	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Note 2		22	35	ns
t_{PHL}					20	30	ns
t_{PLH}	Any M input	Any Q			25	40	ns
t_{PHL}					22	35	ns
t_{PLH}	Any B input	Any Q			27	42	ns
t_{PHL}					24	37	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

TYPICAL APPLICATION DATA

Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:

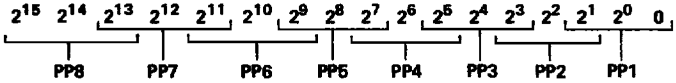
```
        DECIMAL            BINARY                      2-BIT-AT-A-TIME BINARY

                      Sign                                 Sign
                      Bit                                  Bit
                       ↓                                    ↓
B         26           011010                               011010
M         29           011101                             (+2) (−1) (+1)
         234           011010  ⎫                     00000011010  ⎫   3
         52           000000   ⎪                     111100110    ⎬ Partial
         754         011010    ⎪     6               0110100      ⎭ Products
                    011010     ⎬  Partial            01011110010
                   011010      ⎪  Products           ↑ \___ ___/
                  000000       ⎭                   Sign   Product
                  01011110010                      Bit
                  ↑ \___ ___/
                Sign  Product
                Bit
```

Two points should be noted in the two-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer.

A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.



TYPICAL APPLICATION DATA

2. Generate partial product (PPi) as shown in the following table:

MULTIPLIER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2^{2i-1}	2^{2i-2}	2^{2i-3}		
0	0	0	0	Replace multiplicand by zero
0	0	1	+1 B	Copy multiplicand
0	1	0	+1 B	Copy multiplicand
0	1	1	+2 B	Shift multiplicand left one bit
1	0	0	−2 B	Shift two's complement of multiplicand left one bit
1	0	1	−1 B	Replace multiplicand by two's complement
1	1	0	−1 B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

3. Weight the partial products by indexing each two places left relative to the next-less-significant product.

4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.

EXAMPLE OF ALGORITHM

M = 29 = 011101	Operator Symbol	B = 26 = 011010
010	+1 B	00000011010
110	−1 B	111100110
011	+2 B	0110100

The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 'LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.

2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2^{2i+15} of each partial product and also in bit position 2^{16} of the first partial product (PP1).

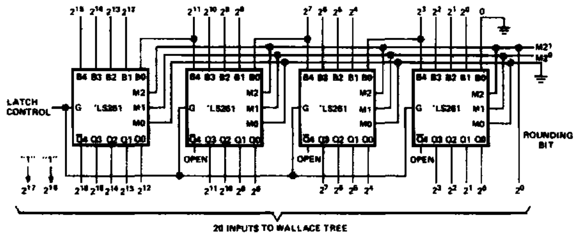


FIGURE A—FIRST PARTIAL PRODUCT, PP1

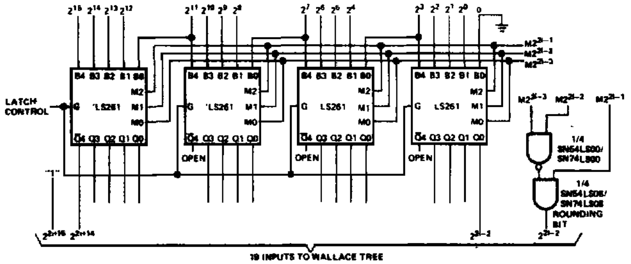


FIGURE B—OTHER PARTIAL PRODUCTS, PPi

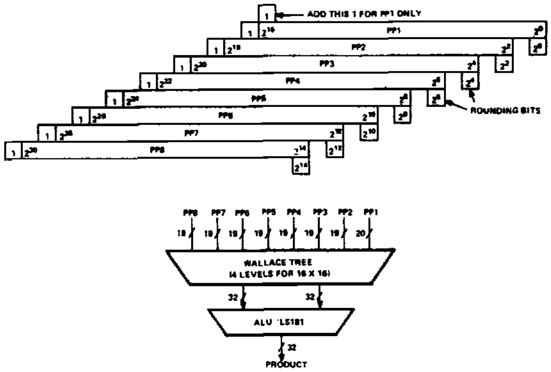


FIGURE C—MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 'LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 'LS261s m x n ÷ 16 'LS00s, and m x n ÷ 16 'LS08s. The size of the Wallace tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

32	SN54LS261/SN74LS261
2	SN54LS00/SN74LS00
2	SN54LS08/SN74LS08
56	SN54LS183/SN74LS183
7	SN54LS181/SN74LS181
2	SN54S182/SN74S182