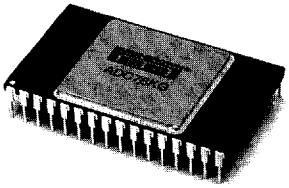
BURR-BROWN®



ADC76

ABRIDGED DATA SHEET
For Additional Technical Information, Request PDS-1063.

16-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003% max (KG, BG)
- NO MISSING CODES GUARANTEED FROM –25°C TO +85°C
- 17µs CONVERSION TIME (16-Bit)
- SERIAL AND PARALLEL OUTPUTS

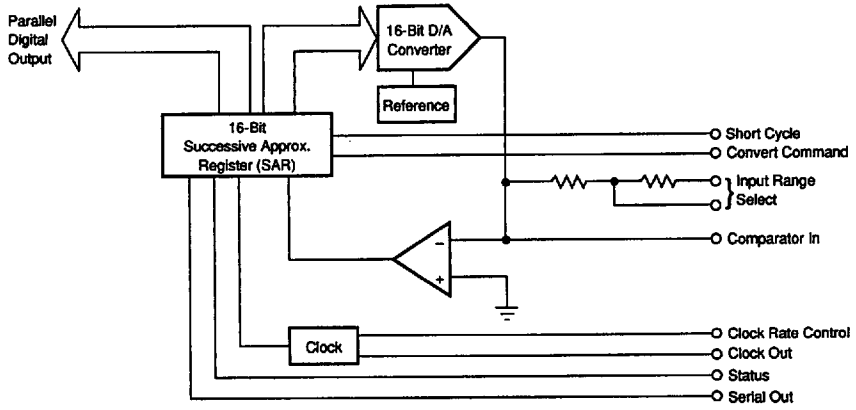
DESCRIPTION

The ADC76 is a high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art laser-trimmed IC thin-film resistors and is packaged in a hermetic 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

It is specified for operation over two temperature ranges: 0°C to +70°C (J, K) and –25°C to +85°C (A, B).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



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SPECIFICATIONS

ELECTRICAL

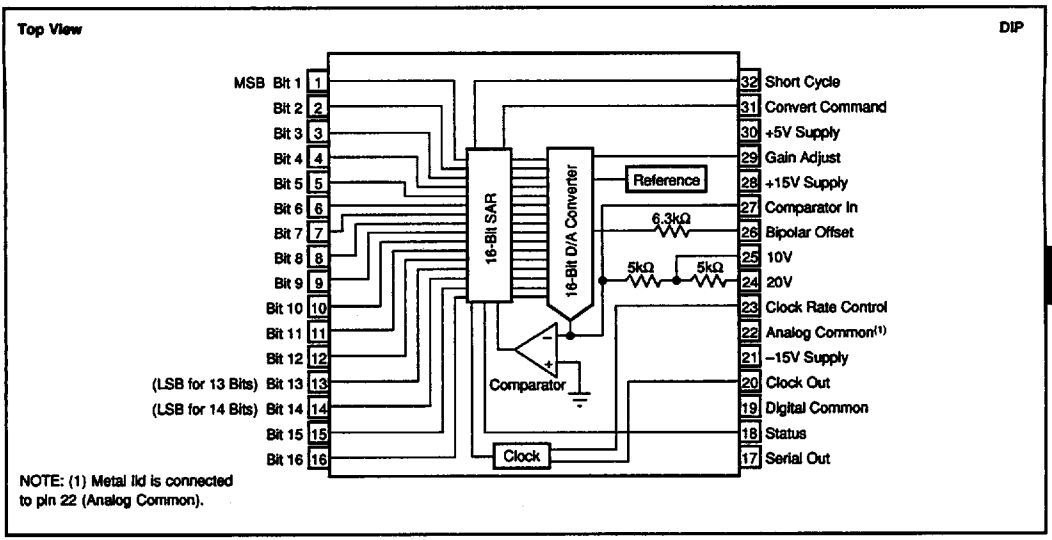
At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76J, K MIN	ADC76J, K TYP	ADC76J, K MAX	ADC76A, B MIN	ADC76A, B TYP	ADC76A, B MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10			*		V
		0 to +20			*		
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS[1]							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error[2]		±0.1	±0.2		*	*	%
Offset Error: Unipolar[2]		±0.05	±0.1		*	*	% of FSR[3]
Bipolar[2]		±0.1	±0.2		*	*	% of FSR
Linearity Error: K, B			±0.003			*	% of FSR
J, A			±0.006			*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0.003			*		% of FSR
Noise (3σ, p-p)		±0.001	±0.003		*	*	% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_s
+5VDC		0.001			*		% of FSR/%V_s
CONVERSION TIME[4]							
14 Bits			15			*	µs
15 Bits			16			*	µs
16 Bits			17			*	µs
WARM-UP TIME	5			*			Min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4		*	*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3		*	*	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13-bit)	0		+70	–25		+85	°C
K, B (14-bit)	0		+70	–25		+85	°C
OUTPUT DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes[5]: Unipolar		CSB			*		
Bipolar		COB, CTC[6]			*		
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status		Logic "1" during conversion			*		
Status Output Drive			2			*	TTL Loads
Internal Clock: Clock Output Drive			2			*	TTL Loads
Frequency[7]	933		1400	*		*	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.655			*		W
Rated Voltage: Analog	±11.4	±15	±16	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+10	+15		*	*	mA
–15VDC		–28	–35		*	*	mA
+5VDC		+17	+20		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	–25		+85	°C
Storage	–55		+125	*		*	°C

*Specification same as ADC76J, K.

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1" = 2.4V, min. (2) Adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB—Complementary Straight Binary, COB—Complementary Offset Binary, CTC—Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz.

PIN CONFIGURATION



NOTE: (1) Metal lid is connected to pin 22 (Analog Common).

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{cc}$ to Common	0V to +16.5V
$-V_{cc}$ to Common	0V to –16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	300°C

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC76JG	32-Pin Hermetic DIP	172-5
ADC76KG	32-Pin Hermetic DIP	172-5
ADC76AG	32-Pin Hermetic DIP	172-5
ADC76BG	32-Pin Hermetic DIP	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	LINEARITY ERROR max (% of FSR)	TEMPERATURE RANGE
ADC76AG	±0.006	–25°C to +85°C
ADC76BG	±0.003	–25°C to +85°C
ADC76JG	±0.006	0°C to +70°C
ADC76KG	±0.003	0°C to +70°C

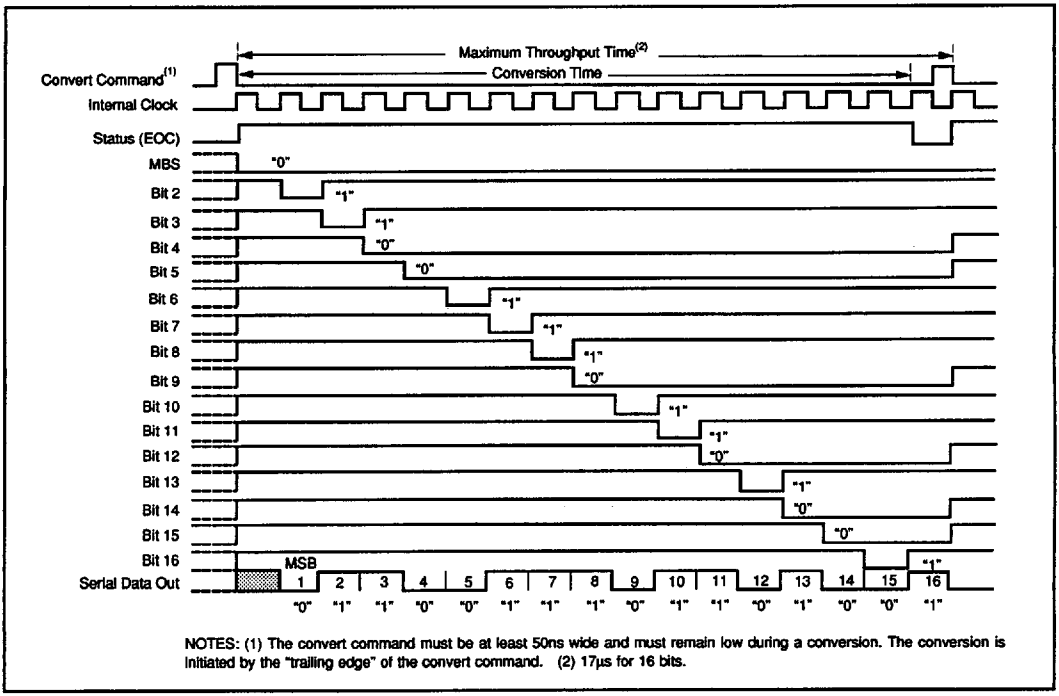


FIGURE 1. ADC76 Timing Diagram.

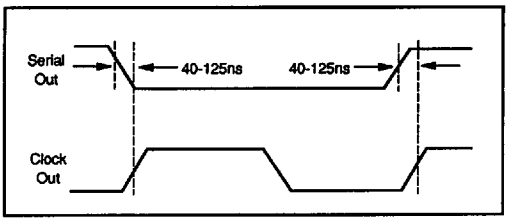


FIGURE 2. Timing Relationship of Serial Data to Clock.

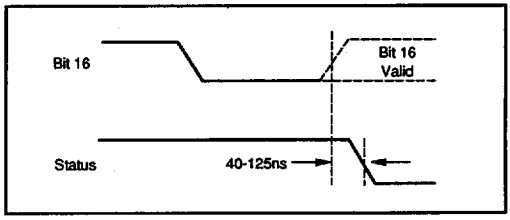


FIGURE 3. Timing Relationship of Valid Data to Status.

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	n = 14	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values MSB LSB							
000 ... 000(4)	+Full Scale	+10V–3/2LSB	+5V–3/2LSB	+2.5V–3/2LSB	+10V–3/2LSB	+5V–3/2LSB	+20V–3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.