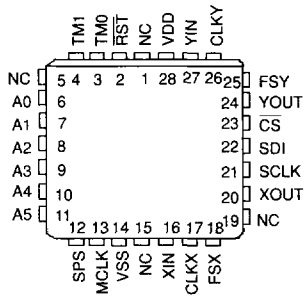
DALLAS SEMICONDUCTOR

DS2164Q
G.726 ADPCM Processor

FEATURES

- Compresses/expands 64Kbps PCM voice to/from either 32Kbps, 24Kbps, or 16Kbps as per the CCITT/ ITU G.726 specification
- Dual, fully independent channel architecture; device can be programmed to perform either:
  - two expansions
  - two compressions
  - one expansion and one compression
- Interconnects directly to combo-codec devices
- Input to output delay is less than 375 µs
- Simple serial port used to configure the device
- Onboard Time Slot Assigner Circuit (TSAC) function allows data to be input/output at various time slots
- Supports Channel Associated Signaling
- Each channel can be independently idled or placed into bypass
- Available hardware mode requires no host processor; ideal for voice storage applications
- Backward-compatible with the DS2165 ADPCM Processor Chip
- Single +5V supply; low-power CMOS technology
- Available in 28-pin PLCC

PIN ASSIGNMENT



28-Pin PLCC

DESCRIPTION

The DS2164Q ADPCM Processor Chip is a dedicated Digital Signal Processing (DSP) chip that has been optimized to perform Adaptive Differential Pulse Code Modulation (ADPCM) speech compression at three different rates. The chip can be programmed to compress (expand) 64Kbps voice data down to (up from) either 32Kbps, 24Kbps, or 16Kbps. The compression follows the algorithm specified by CCITT Recommendation G.726. The DS2164Q can switch compression algorithms on-the-fly. This allows the user to make maximum use of the available bandwidth on a dynamic basis.

OVERVIEW

The DS2164Q contains three major functional blocks: a high performance (10 MIPS) DSP engine, two independent PCM interfaces (X and Y) which connect directly to serial Time Division Multiplexed (TDM) backplanes, and a serial port that can configure the device on-the-fly via an external controller. A 10 MHz master clock is required by the DSP engine. The DS2164Q can be configured to perform either two expansions, two compressions, or one expansion and one compression. The PCM/ADPCM data interfaces support data rates from 256 KHz to 4.096 MHz. Typically, the PCM data rates

will be 1.544 MHz for μ-law and 2.048 MHz for A-law. Each channel on the device samples the serial input PCM or ADPCM bit stream during a user-programmed input time slot, processes the data and outputs the result during a user-programmed output time slot.

Each PCM interface has a control register which specifies functional characteristics (compress, expand, bypass, and idle), data format (μ-law or A-law), and algorithm reset control. With the SPS pin strapped high, the software mode is enabled and the serial port can be used to configure the device. In this mode, a novel addressing scheme allows multiple devices to share a common 3-wire control bus, simplifying system-level interconnect.

With SPS low, the hardware mode is enabled. This mode disables the serial port and maps certain control register bits to some of the address and serial port pins. Under the hardware mode, no external host controller is required and all PCM/ADPCM input and output time slots default to time slot 0.

HARDWARE RESET

$\overline{RST}$ allows the user to reset both channel algorithms and the contents of the internal registers. This pin must be held low for at least 1 ms on system power-up after the master clock is stable to ensure that that the device has initialized properly. $\overline{RST}$ should also be asserted when changing to or from the hardware mode. $\overline{RST}$ clears all bits of the Control Register for both channels except the IPD bits; the IPD bits for both channels are set to 1.

SOFTWARE MODE

Tying SPS high enables the software mode. In this mode, an external host controller writes configuration data to the DS2164Q via the serial port through inputs SCLK, SDI, and $\overline{CS}$. (See Figure 2.) Each write to the DS2164Q is either a 2-byte write or a 4-byte write. A 2-byte write consists of the Address/Command Byte (ACB), followed by a byte to configure the Control Register (CR) for either the X or Y channel. The 4-byte write consists of the ACB, followed by a byte to configure the CR, and then one byte to set the input time slot and another byte to set the output time slot.

ADDRESS/COMMAND BYTE

In the software mode, the address/command byte is the first byte written to the serial port; it identifies which of the 64 possible ADPCM processors sharing the port wiring is to be updated. Address data must match that at inputs A0 to A5. If no match occurs, the device ignores the following configuration data. If an address match occurs, the next three bytes written are accepted as control, input and output time slot data. Bit ACB.6 determines which side (X or Y) of the device is to be updated. The PCM and ADPCM outputs are tristated during register updates.

CONTROL REGISTER

The control register establishes idle, algorithm reset, bypass, data format and channel coding for the selected channel.

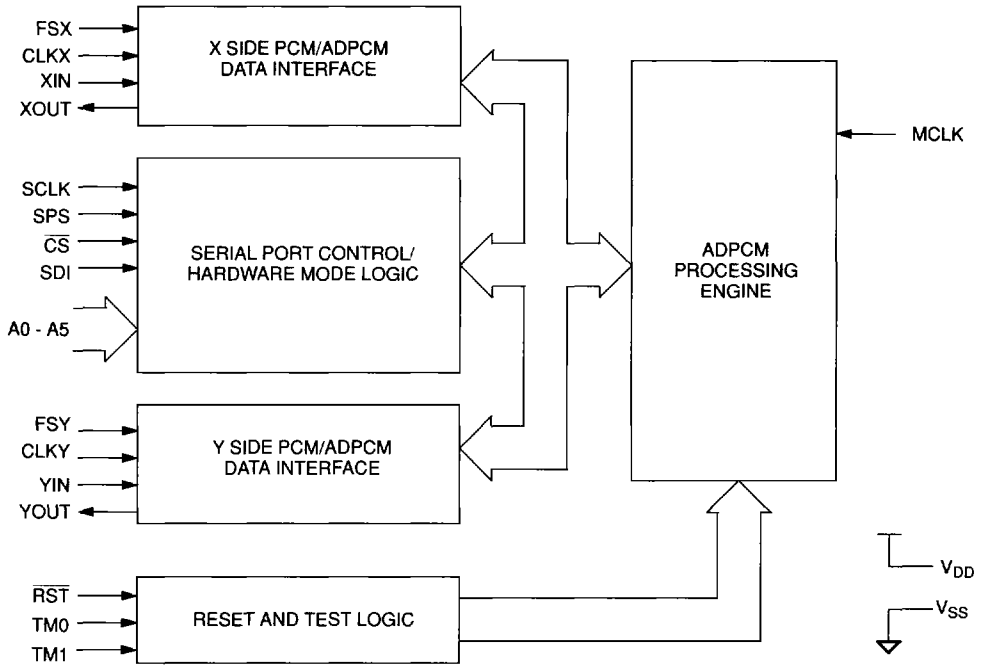
The X and Y side PCM interfaces can be independently disabled (output 3-stated) via IPD. When IPD is set for both channels, the device enters a low-power standby mode. In this mode, the serial port must not be operated faster than 39 KHz.

ALRST resets the algorithm coefficients for the selected channel to their initial values. ALRST will be cleared by the device when the algorithm reset is complete.

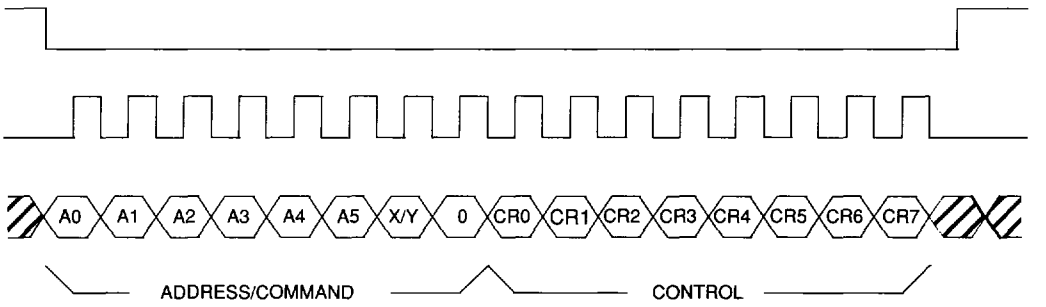
PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
2	$\overline{RST}$	I	**Reset.** A high-low-high transition resets the algorithm. The device should be reset on power up and when changing to or from the hardware mode.
3 4	TM0 TM1	I	**Test Modes 0 and 1.** Tie to V_{SS} for normal operation.
6 7 8 9 10 11	A0 A1 A2 A3 A4 A5	I	**Address Select.** A0 = LSB; A5 = MSB Must match address/command word to enable the serial port.
12	SPS	I	**Serial Port Select.** Tie to V_{DD} to select the serial port; tie to V_{SS} to select the hardware mode.
13	MCLK	I	**Master Clock.** 10 MHz clock for the ADPCM processing engine; may be asynchronous to SCLK, CLKX, and CLKY.
14	V_{SS}	–	**Signal Ground.** 0.0 volts.
16	XIN	I	**X Data In.** Sampled on falling edge of CLKX during selected time slots.
17	CLKX	I	**X Data Clock.** Data clock for the X side PCM interface; must be synchronous with FSX.
18	FSX	I	**X Frame Sync.** 8 KHz frame sync for the X side PCM interface.
20	XOUT	O	**X Data Output.** Updated on rising edge of CLKX during selected time slots.
21	SCLK	I	**Serial Data Clock.** Used to write to the serial port registers.
22	SDI	I	**Serial Data In.** Data for onboard control registers; sampled on the rising edge of SCLK. LSB sent first.
23	$\overline{CS}$	I	**Chip Select.** Must be low to write to the serial port.
24	YOUT	O	**Y Data Output.** Updated on rising edge of CLKY during selected time slots.
25	FSY	I	**Y Frame Sync.** 8 KHz frame sync for the Y side PCM interface.
26	CLKY	I	**Y Data Clock.** Data clock for the Y side PCM interface; must be synchronous with FSY.
27	YIN	I	**Y Data In.** Sampled on falling edge of CLKY during selected time slots.
28	V_{DD}	–	**Positive Supply.** 5.0 volts.

DS2164Q BLOCK DIAGRAM Figure 1



SERIAL PORT WRITE Figure 2



NOTE:
1. A 2-byte write is shown.

The bypass feature is enabled when BYP is set and IPD is cleared. During bypass, no expansion or compression occurs. Bypass operates on bytewide (8 bits) slots when CP/$\overline{EX}$ is set and on nibble-wide (4 bits) slots when CP/$\overline{EX}$ is cleared.

A-law (U/$\overline{A}$ = 0) and μ-law (U/$\overline{A}$ = 1) PCM coding is independently selected for the X and Y channels via CR.2. If BYP and IPD are cleared, then CP/$\overline{EX}$ determines if the input data is to be compressed or expanded.

ADDRESS/COMMAND BYTE Figure 3

(MSB)							(LSB)
–	X/$\overline{Y}$	A5	A4	A3	A2	A1	A0

SYMBOL	POSITION	NAME AND DESCRIPTION
–	ACB.7	Reserved; must be 0 for proper operation
X/$\overline{Y}$	ACB.6	X/$\overline{Y}$ Channel Select 0 = update channel Y characteristics 1 = update channel X characteristics
A5	ACB.5	MSB of Device Address
A4	ACB.4	
A3	ACB.3	
A2	ACB.2	
A1	ACB.1	
A0	ACB.0	LSB of Device Address

CONTROL REGISTER Figure 4

(MSB)							(LSB)
AS0	AS1	IPD	ALRST	BYP	U/$\overline{A}$	AS2	CP/$\overline{EX}$

SYMBOL	POSITION	NAME AND DESCRIPTION
AS0	CR.7	Algorithm Select 0. See Table 2.
AS1	CR.6	Algorithm Select 1. See Table 2.
IPD	CR.5	Idle and Power Down. 0 = channel enabled 1 = channel disabled (output 3-stated)
ALRST	CR.4	Algorithm Reset. 0 = normal operation 1 = reset algorithm for selected channel
BYP	CR.3	Bypass. 0 = normal operation 1 = bypass selected channel
U/$\overline{A}$	CR.2	Data Format. 0 = A-law 1 = μ-law
AS2	CR.1	Algorithm Select 2. See Table 2.
CP/$\overline{EX}$	CR.0	Channel Coding. 0 = expand (decode) selected channel 1 = compress (encode) selected channel

ALGORITHM SELECT BITS Table 2

ALGORITHM SELECTED	AS2	AS1	AS0
64Kbps to/from 32Kbps	0	0	0
64Kbps to/from 24Kbps	1	1	1
64Kbps to/from 16Kbps	1	0	1

INPUT TIME SLOT REGISTER Figure 5

(MSB)							(LSB)
–	–	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	ITR.7	Reserved; must be 0 for proper operation.
-	ITR.6	Reserved; must be 0 for proper operation.
D5	ITR.5	MSB of input time slot register.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input time slot register.

OUTPUT TIME SLOT REGISTER Figure 6

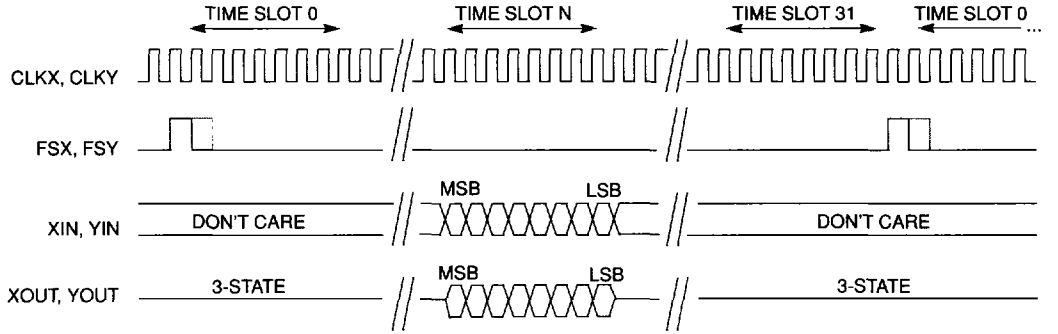
(MSB)							(LSB)
–	–	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
-	OTR.7	Reserved; must be 0 for proper operation.
-	OTR.6	Reserved; must be 0 for proper operation.
D5	OTR.5	MSB of output time slot register.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output time slot register.

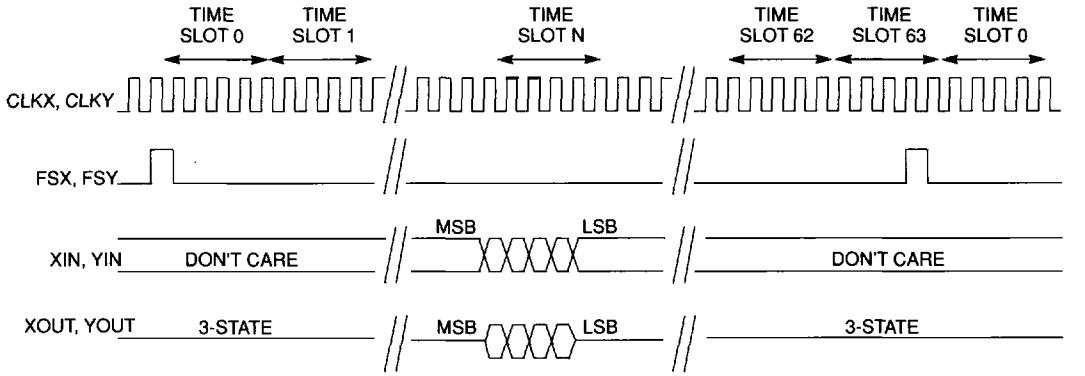
TIME SLOT ASSIGNMENT/ORGANIZATION

Onboard counters establish when PCM and ADPCM I/O occurs. The counters are programmed via the time slot registers. Time slot size (number of bits wide) is determined by the state of CP/$\overline{EX}$. The number of time slots available is determined by both the state of CP/$\overline{EX}$ and U/$\overline{A}$. (See Figures 7 through 10.) For example, if the X channel is set to compress (CP/$\overline{EX}$ = 1) and it is set to expect μ-law data (U/$\overline{A}$ = 1), then the input port (XIN) is set up for 32 8-bit time slots and the output port (XOUT) is set up for 64 4-bit time slots. The time slot organization is not dependent on which algorithm has been selected. NOTE: Time slots are counted from the frame sync signal starting at the first rising edge of either CLKX or CLKY after the frame sync.

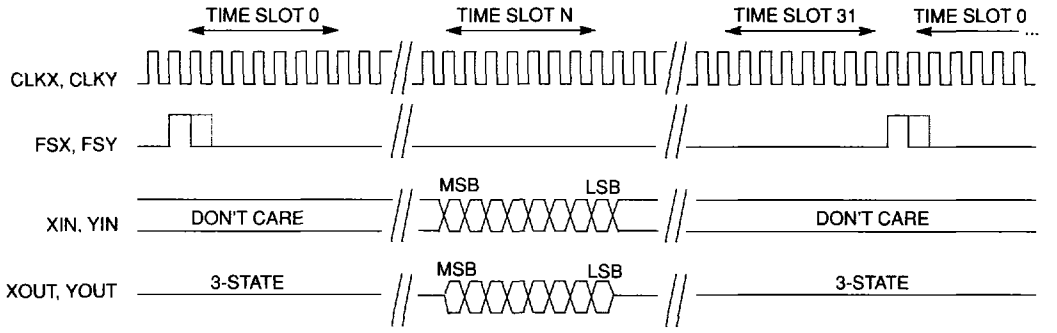
DS2164Q μ-LAW PCM INTERFACE Figure 7



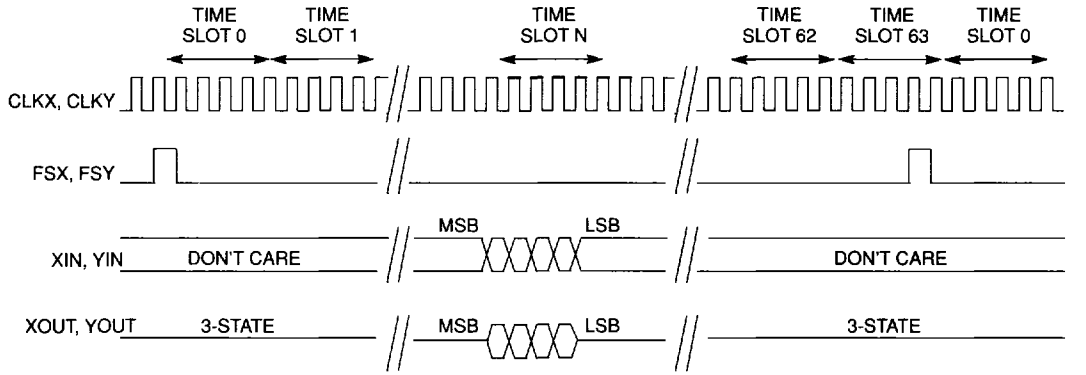
DS2164Q μ-LAW ADPCM INTERFACE Figure 8



DS2164Q A-LAW PCM INTERFACE Figure 9



DS2164Q A-LAW ADPCM INTERFACE Figure 10



HARDWARE MODE

The hardware mode is intended for applications that do not have an external controller available or do not require the extended features offered by the serial port. Tying the SPS pin to V_{SS} disables the serial port, clears all internal register bits and maps the IPD, U/$\overline{A}$, and CP/$\overline{EX}$ bits for both channels to external bits. (See Table 3.) In the hardware mode, both the input and output time slots default to time slot 0.

HARDWARE MODE Table 3

PIN # / NAME	REG. LOCATION	NAME AND DESCRIPTION
4 / A0	CP/$\overline{EX}$ (Channel X)	Channel X Coding Configuration 0 = Expand 1 = Compress
5 / A1	AS0/AS1/AS2 (Channel X & Y)	Algorithm Select (see Table 5)
6 / A2	U/$\overline{A}$ (Channel X)	Channel X Data Format 0 = A-law 1 = μ-law
7 / A3	CP/$\overline{EX}$ (Channel Y)	Channel Y Coding Configuration 0 = Expand 1 = Compress
8 / A4	AS0/AS1/AS2 (Channel X & Y)	Algorithm Select (see Table 5)
9 / A5	U/$\overline{A}$ (Channel Y)	Channel Y Data Format 0 = A-law 1 = μ-law
18 / SDI	IPD (Channel Y)	Channel Y Idle Select 0 = Channel active 1 = Channel idle
19 / $\overline{CS}$	IPD (Channel X)	Channel X Idle Select 0 = Channel active 1 = Channel idle

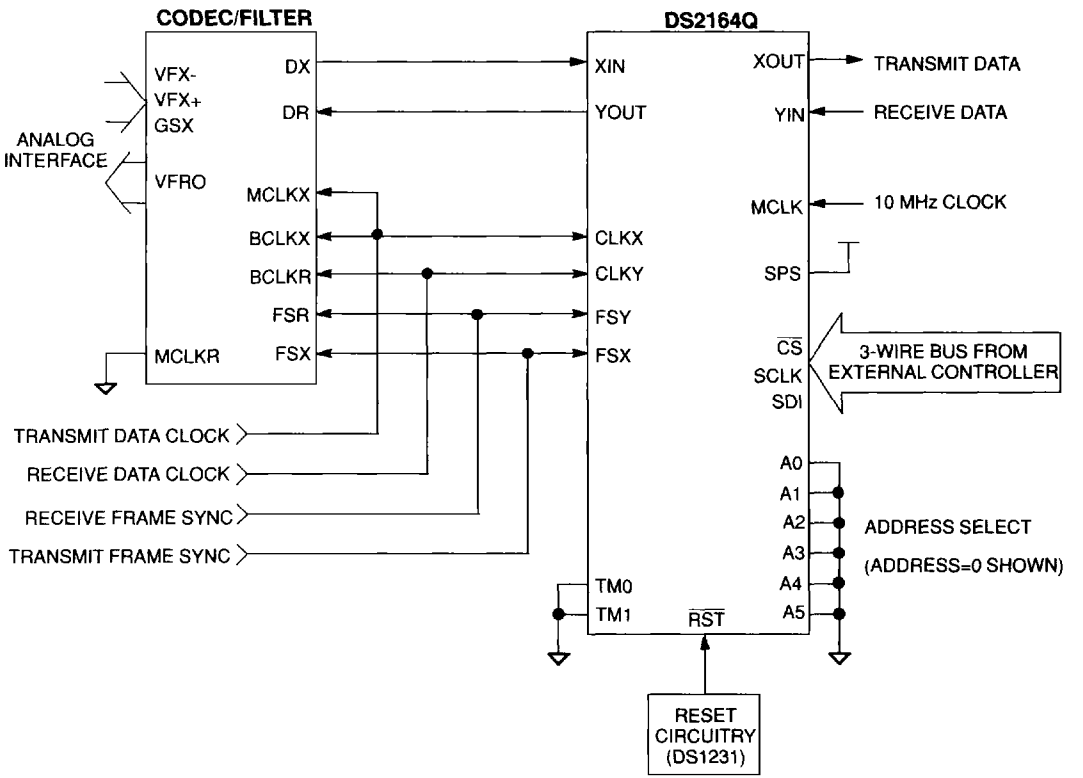
NOTES:

1. SCLK must be tied to V_{SS} when the hardware mode is selected.
2. When both channels are idled, power consumption is significantly reduced.
3. The DS2164Q will power-up within 800 ms after either channel is returned to active from an idle state.

ALGORITHM SELECT FOR HARDWARE MODE Table 4

ALGORITHM	CONFIGURATION OF A1 AND A4
64Kbps to/from 32Kbps	Tie both A1 and A4 to V_{SS}.
64Kbps to/from 24Kbps	Hold A1 and A4 low during a hardware reset; take both A1 and A4 high after the $\overline{RST}$ pin has returned high (allow 3 µs after $\overline{RST}$ returns high before taking A1 and A4 high).
64Kbps to/from 16Kbps	Tie both A1 and A4 to V_{DD}.

DS2164Q CONNECTION TO CODEC/FILTER Figure 11



NOTE:

Suggested Codec/Filters

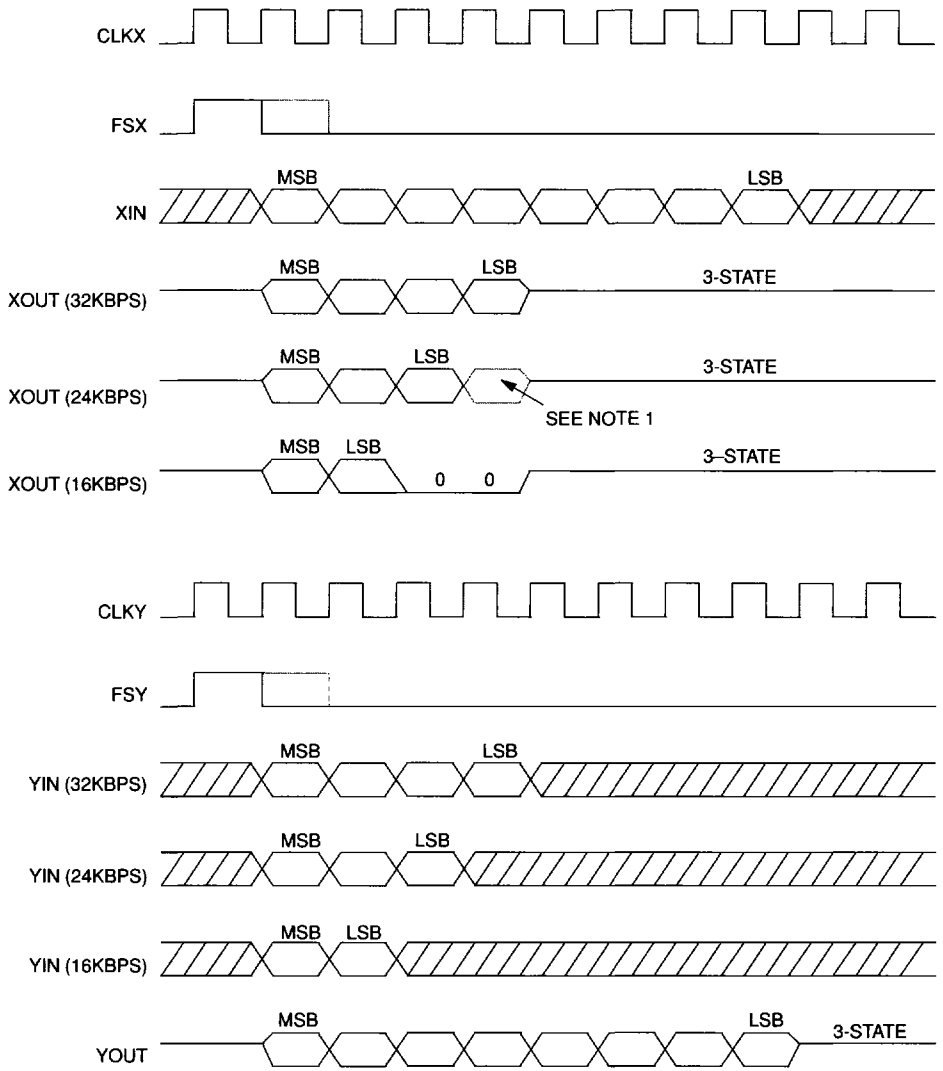
TP305X	National Semiconductor
ETC505X	SGS–Thomson Microelectronics
MC1455XX	Motorola
TCM29CXX	Texas Instruments
HD44238C	Hitachi

*other generic Codec/Filter devices can be substituted.

PCM AND ADPCM INPUT/OUTPUT

Since the organization of the input and output time slots on the DS2164Q does not depend on the algorithm selected, it always assumes that PCM input and output will be in 8-bit bytes and that ADPCM input and output will be in 4-bit bytes. Figure 12 demonstrates how the DS2164Q handles the I/O for the three different algorithms. In the figure, it is assumed that channel X is in the compression mode (CP/$\overline{EX}$ = 1) and channel Y is in the expansion mode (CP/$\overline{EX}$ = 0). Also, it is assumed that both the input and output time slots for both channels are set to 0.

PCM AND ADPCM I/O EXAMPLE Figure 12



NOTE:

1. The bit after the LSB in the 24Kbps ADPCM output will only be a 1 when the DS2164Q is operated in the software mode and is programmed to perform 24Kbps compression; in all other configurations, it will be a 0.

TIME SLOT RESTRICTIONS

Under certain conditions, the DS2164Q does contain some restrictions on the output time slots that are available. These restrictions are covered in detail in a separate application note. No restrictions occur if the DS2164Q is operated in the hardware mode.

INPUT TO OUTPUT DELAY

With all three compressions algorithms, the total delay, from the time the PCM data sample is captured by the DS2164Q to the time it is output, is always less than 375 µs. The exact delay is determined by the input and output time slots selected for each channel.

CHANNEL ASSOCIATED SIGNALING

The DS2164Q supports Channel Associated Signaling (CAS) via its ability to automatically change from the 32Kbps compression algorithm to the 24Kbps algorithm. If the DS2164Q is configured to perform the 32Kbps algorithm, then in both the hardware and software mode, it will sense the frame sync inputs (FSX and FSY) for a double wide frame sync pulse. Whenever the DS2164Q receives a double wide pulse, it will automatically switch from the 32Kbps algorithm to the 24Kbps algorithm. Switching to the 24Kbps algorithm allows the user to insert signaling data into the LSB bit position of the ADPCM output because this bit does not contain any useful speech information.

ON-THE-FLY ALGORITHM SELECTION

In the software mode, the user can switch between the three available algorithms on-the-fly. That is, the DS2164Q does not need to be reset or stopped to make the change from one algorithm to another. The DS2164Q reads the Control Register before it starts to process each PCM or ADPCM sample. If the user wishes to switch algorithms, then the Control Register must be updated via the serial port before the first input sample to be processed with the new algorithm arrives at either XIN or YIN. The PCM and ACPCM outputs will tristate during register updates.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		20		mA	1,2
Idle Supply Current	I_{DDPD}		1		mA	1,2,3
Input Leakage	I_I	-1.0		+1.0	µA	
Output Leakage	I_O	-1.0		+1.0	µA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. CLKX = CLKY = 1.544 MHz; MCLK = 10 MHz.
2. Outputs open; inputs swinging full supply levels.
3. Both channels in idle mode.
4. XOUT and YOUT are 3-stated.

PCM INTERFACE
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CLKX, CLKY Period	t_{PXY}	244		3906	ns	1
CLKX, CLKY Pulse Width	t_{WXYL} t_{WXYH}	100			ns	
CLKX, CLKY Rise Fall Times	t_{RXY} t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	2
Setup Time from FSX, FSY high to CLKX, CLKY low	t_{SF}	50			ns	2
Hold Time from CLKX, CLKY low to FSX, FSY low	t_{HF}	100			ns	2
Setup Time for XIN, YIN to CLKX, CLKY low	t_{SD}	50			ns	2
Hold Time for XIN, YIN to CLKX, CLKY low	t_{HD}	50			ns	2
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	3
Delay Time from CLKX, CLKY to XOUT, YOUT 3-stated	t_{DXYZ}	20		150	ns	2,3,4

NOTES:

1. Maximum width of FSX and FSY is one CLKX or CLKY period (except for signaling frames).
2. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.
3. Load = 150 pF + 2 LSTTL loads.
4. For LSB of PCM or ADPCM byte.

MASTER CLOCK / RESET
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	1
MCLK Pulse Width	t_{WMH}, t_{WML}	45	50	55	ns	
MCLK Rise/Fall Times	t_{RM}, t_{FM}			10	ns	
$\overline{RST}$ Pulse Width	t_{RST}	1			ms	

NOTE:

1. MCLK = 10 MHz ± 500 ppm

SERIAL PORT
AC ELECTRICAL CHARACTERISTICS

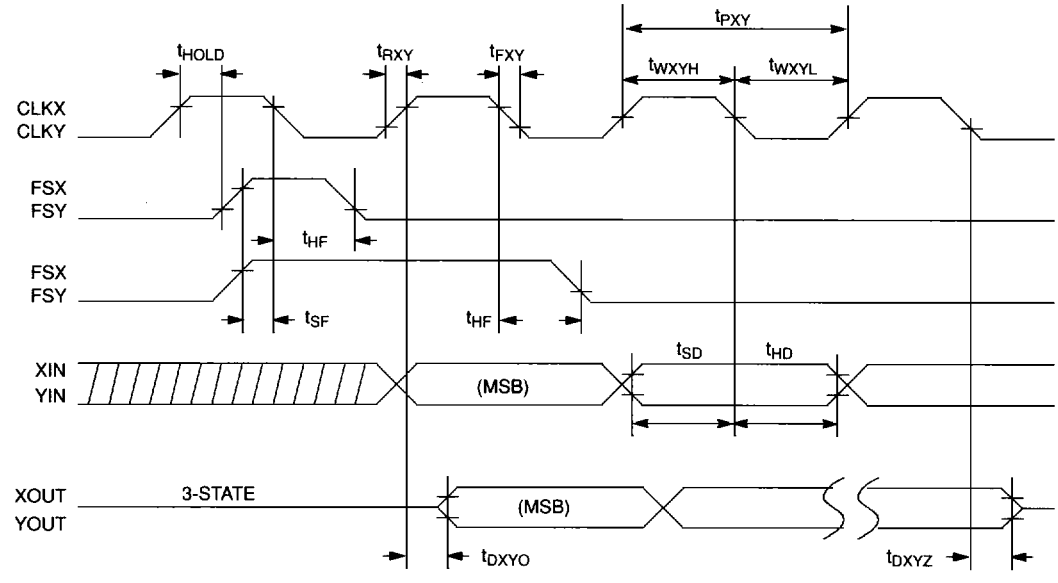
(0°C to 70°C; V_{DD}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Set Up	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Time	t_R, t_F			100	ns	1
CS to SCLK Setup	t_{CC}	50			ns	1
SCLK to $\overline{CS}$ Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to $\overline{CS}$ Falling	t_{SCC}	50			ns	1

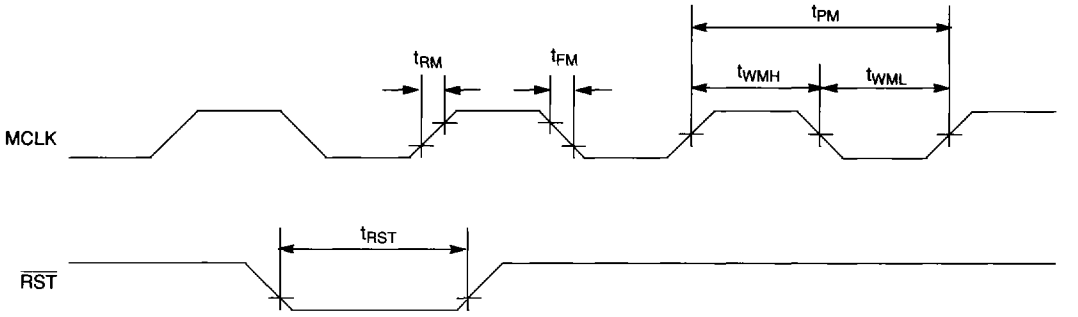
NOTE:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10ns maximum rise and fall times.

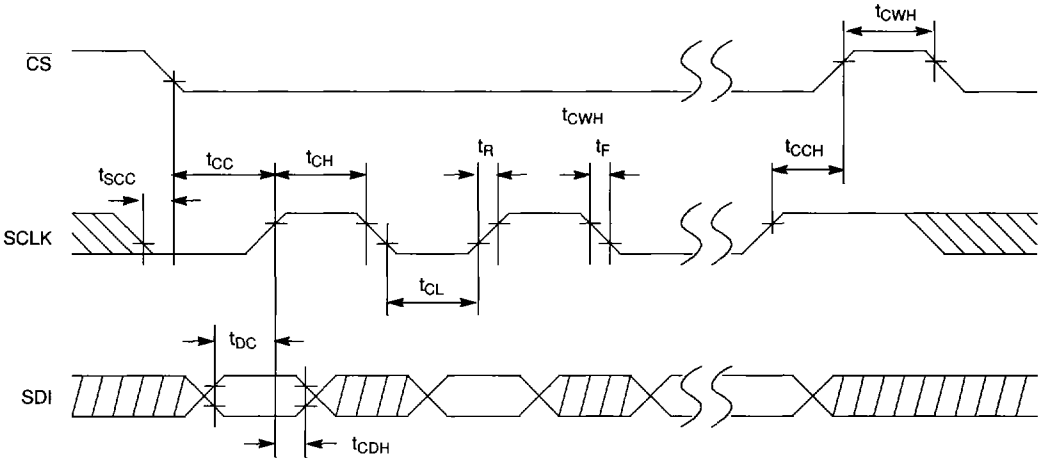
PCM INTERFACE AC TIMING DIAGRAM Figure 13



MASTER CLOCK/RESET AC TIMING DIAGRAM Figure 14



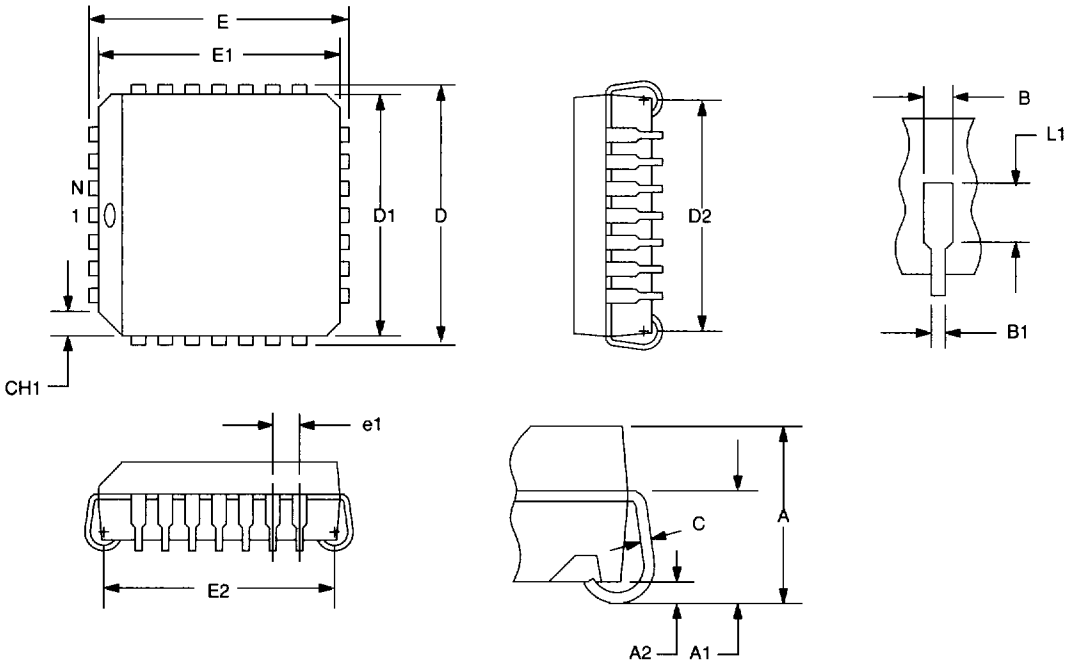
SERIAL PORT AC TIMING DIAGRAM Figure 15



NOTE:

1. SCLK may be either high or low when $\overline{CS}$ is taken low.

DS2164Q G.726 ADPCM PROCESSOR 28-PIN PLCC



DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	–
N	28	–
e1	0.050 BSC	
CH1	0.042	0.048