



LU97—AC-Link Soft Modem Chip Set

Features

- Operating system support:
 - Windows* 95, 98, 2000
 - PC '99 compliant
 - ACPI compliant
- High-speed data mode capabilities:
 - ITU-T V.90 data rates 28000 bits/s—56000 bits/s[†]
 - Ultrahigh compression throughput due to parallel access directly to the host PC
 - ITU-T V.34 extended rates: 33600 bits/s—2400 bits/s V.32terbo, V.32bis, and fallbacks
 - TIA/EIA[§] 602 standard for AT command set
 - V.42 error correction (LAPM and MNP[‡])
 - V.42bis and MNP Class 5 data compression
- FAX mode capabilities:
 - ITU-T V.17, V.29, V.27ter, and V.21 Ch 2
 - TIA/EIA 578 Class 1 FAX
- Video-ready modem interface (VRM) V.80
- Complete DAA includes the following:
 - AC'97/MC'97 2.1 compliant
 - International line interface
 - Compliant with FCC, CTR21, JATE, and other PTTs
 - 3.3 V to 5 V power supply
 - 2400 V isolation
 - Integrated ring detector
 - Integrated analog front end (AFE)
 - 2-wire to 4-wire hybrid
 - Low-power standby mode
 - Low-profile SOIC packages
- Applications:
 - Modem riser cards
 - Mobile daughter cards

Introduction

The Lucent Technologies LU97 chip set is an integrated direct access arrangement (DAA) chip set that provides a low-cost, isolated, silicon-based MC'97 compliant interface to the telephone line. The chip set saves cost and board area by eliminating the need for a modem AFE or serial codec. It also eliminates the need for an isolation transformer, relays, optoisolators, and a 2-wire to 4-wire hybrid. The LU97 chip set complies with AC'97/MC'97 Interface Specification Rev. 2.1.

The chip set is fully programmable to meet worldwide telephone line interface requirements, including those described by CTR21, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the LU97 chip set include ac termination, dc termination, ringer impedance, and ringer threshold. The LU97 chip set has been designed to meet stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

The LU97 chip set achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Lucent's proprietary signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common-mode interference, or noise coupling. All transmit, receive, control, and ring detect data are communicated through this barrier.

The LU97 chip set is available in two 16-pin small outline packages with an AC'97 interface on the CSP1037 and a telephone line interface on the CSP1037A/B. The CSP1037A is designed for domestic DAAs, while the CSP1037B is for international DAAs.

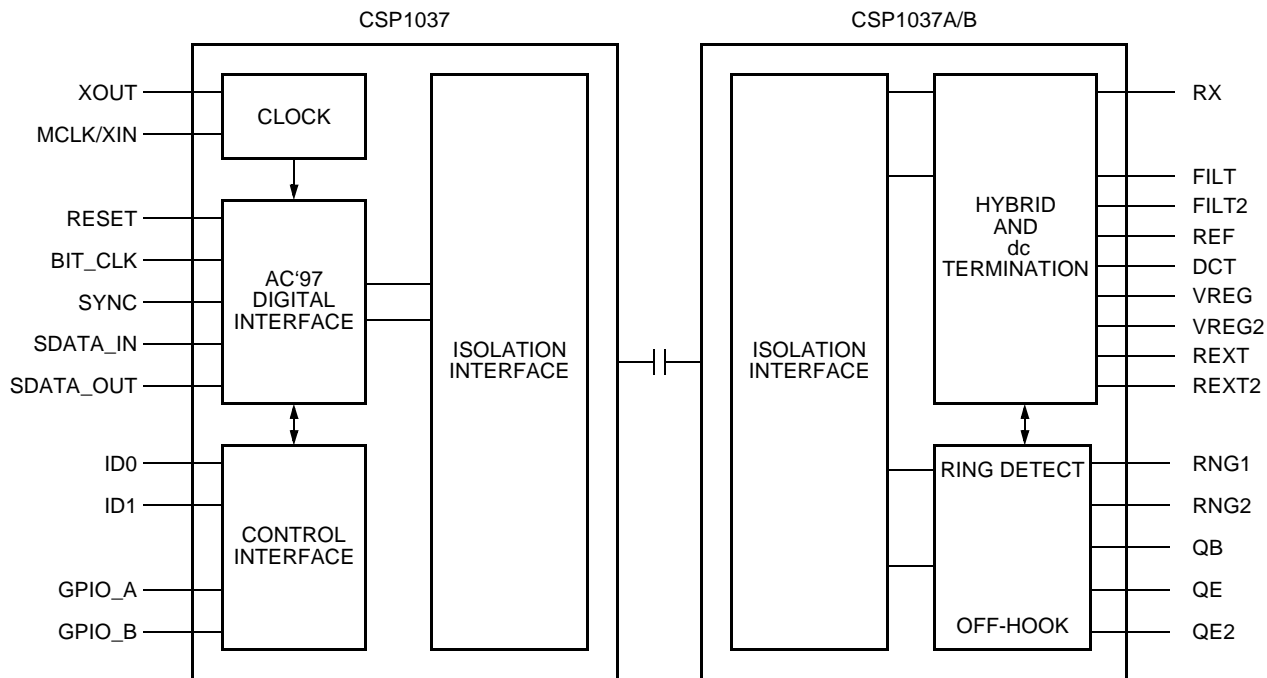
* Windows and Windows NT are registered trademarks of Microsoft Corporation.

† Actual speeds over U.S. telephone lines vary and are less than 56K, due to current FCC regulations and line conditions.

‡ MNP is a registered trademark of Microcom, Inc.

§ EIA is a registered trademark of Electronic Industries Association.

Functional Description



5-8164 (F)

Figure 1. Functional Block Diagram

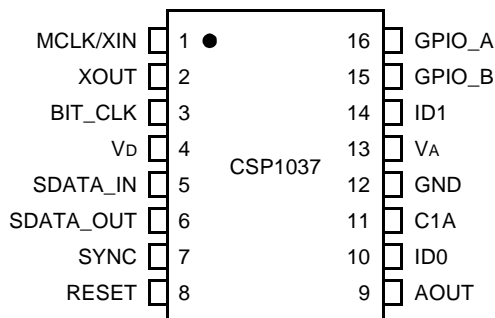
The LU97 chip set is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet international telephone line requirements. The LU97 chip set is available in two 16-pin small outline packages (AC'97 interface on CSP1037 and telephone line interface on CSP1037A/B). The chip set eliminates the need for an AFE, an isolation transformer, relays, optoisolators, and a 2-wire to 4-wire hybrid. The LU97 chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The CSP1037 complies with AC'97/MC'97 Interface Specification Rev. 2.1.

The chip set is fully programmable to meet worldwide telephone line interface requirements, including those described by CTR21, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the LU97 chip set include ac termination, dc termination, ringer impedance, and ringer threshold. The LU97 chip set has been designed to meet stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

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Pin Information

CSP1037 Pin Information



5-8163 (F)

Figure 2. CSP1037 Pin Locations, 16-Pin SOIC

Table 1. CSP1037 Pin Locations, 16-Pin SOIC

Pin	Name	Type	Pin	Name	Type	Pin	Name	Type	Pin	Name	Type
1	MCLK/XIN	I	5	SDATA_IN	O	9	AOUT	O	13	VA	P
2	XOUT	O	6	SDATA_OUT	I	10	ID0	I	14	ID1	I
3	BIT_CLK	I/O	7	SYNC	I	11	C1A	—	15	GPIO_B	I/O
4	Vd	P	8	RESET	I	12	GND	P	16	GPIO_A	I/O

CSP1037 Serial Interface Signals

Table 2. CSP1037 Serial Interface Signal Descriptions

Signal	Description
BIT_CLK	Serial Port Bit Clock Output/Input. Controls the serial data on SDATA_IN and latches the data on SDATA_OUT. Output when configured as primary device. Input when configured as secondary device.
SDATA_IN	Serial Port Data Out. Serial communication and control data that is generated by the digital AC'97 controller and presented as an input to the CSP1037.
SDATA_OUT	Serial Port Data In. Serial communication and status data that is provided by the CSP1037 to the digital AC'97 controller.
SYNC	Frame Sync Input. Data framing signal that is used to indicate the start and stop of a communication data frame.
RESET	Reset Input (Active-Low). An active-low input that is used to reset all control registers to a defined, initialized state. Also used to bring the LU97 chip set out of sleep mode.

Pin Information (continued)

CSP1037 Miscellaneous Signals

Table 3. CSP1037 Miscellaneous Signal Descriptions

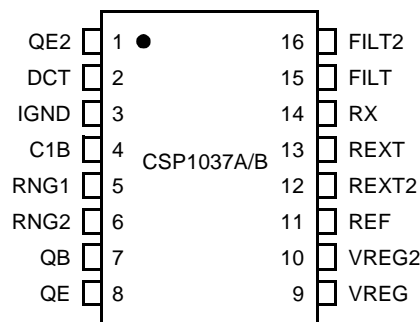
Signal	Description
ID0	Device ID Bit 0. Bit 0 of the device configuration.
ID1	Device ID Bit 1. Bit 1 of the device configuration.
AOUT	Analog Speaker Output. Provides an analog output signal for driving a call progress speaker.
C1A	Isolation Capacitor 1A. Connects to one side of the isolation capacitor C1.
MCLK/XIN	Master Clock Input/Crystal Input.
XOUT	Crystal Output.
GPIO_A	General-Purpose I/O A. Programmable via registers 4Ch—54h. Default input.
GPIO_B	General-Purpose I/O B. Programmable via registers 4Ch—54h. Default input.

CSP1037 Power Signals

Table 4. CSP1037 Power Signal Descriptions

Signal	Description
V _D	Digital Supply Voltage. Provides the digital supply voltage to the CSP1037. Nominally either 3.3 V or 5 V.
V _A	Analog Supply Voltage. Provides analog supply voltage for the CSP1037. Nominally 5 V.
GND	Ground. Connects to the system digital ground. Also connects to capacitor C2.

CSP1037A/B Pin Information



5-8165 (F)

Figure 3. CSP1037A/B Pin Locations, 16-Pin SOIC

Table 5. CSP1037A/B Pin Locations, 16-Pin SOIC

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	QE2	5	RNG1	9	VREG	13	REXT
2	DCT	6	RNG2	10	VREG2	14	RX
3	IGND	7	QB	11	REF	15	FILT
4	C1B	8	QE	12	REXT2	16	FILT2

Pin Information (continued)

CSP1037A/B Line Interface Signals

Table 6. CSP1037A/B Line Interface Signal Descriptions

Signal	Description
FILT	Filter. Sets the time constant for the dc termination circuit.
FILT2	Filter 2. Sets the time constant for the dc termination circuit.
RX	Receive Input. Serves as the receive side input from the telephone network.
DCT	dc Termination. Provides dc termination to the telephone network.
REXT	External Resistor. Sets the real ac termination impedance.
REXT2	External Resistor 2. Sets the complex ac termination impedance.
RNG1	Ring 1. Connects through a 2200 pF capacitor to the tip lead of the telephone line. Provides the ring and signals to the CSP1037A/B.
RNG2	Ring 2. Connects through a 2200 pF capacitor to the ring lead of the telephone line. Provides the ring and signals to the CSP1037A/B.
QB	Transistor Base. Connects to the base of transistor Q3.
QE	Transistor Emitter. Connects to the emitter of transistor Q3.
QE2	Transistor Emitter 2. Connects to the emitter of transistor Q4.
REF	Reference. Connects to an external resistor to provide a high-accuracy reference current.

CSP1037A/B Isolation Signals

Table 7. CSP1037A/B Isolation Signal Descriptions

Signal	Description
C1B	Isolation Capacitor 1B. Connects to one side of isolation capacitor C1.
IGND	Isolated Ground. Connects to ground on the line-side interface. Also connects to capacitor C2.

CSP1037A/B Miscellaneous Signals

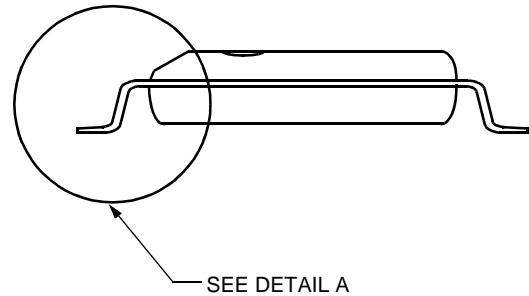
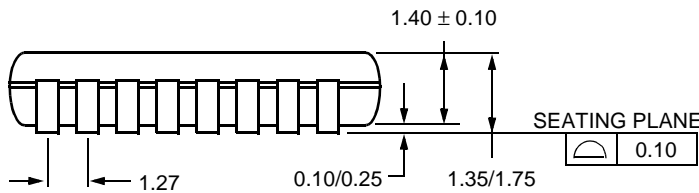
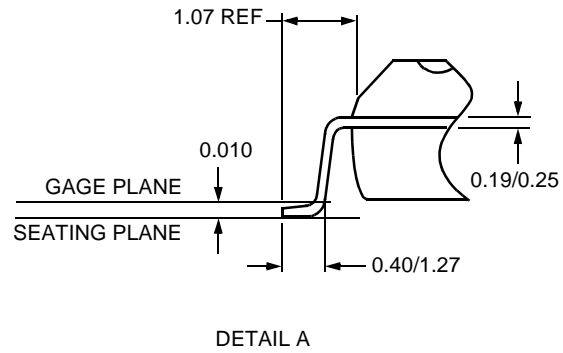
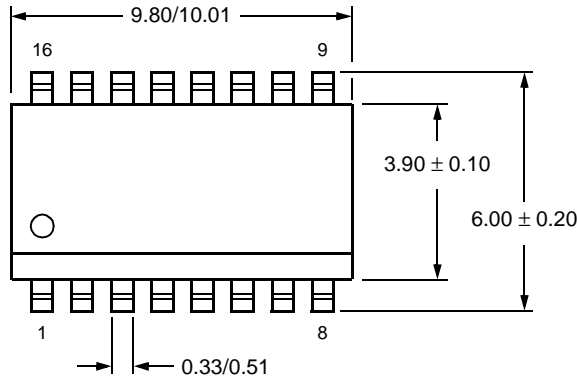
Table 8. CSP1037A/B Miscellaneous Signal Descriptions

Signal	Description
VREG	Voltage Regulator. Connects to an external capacitor to provide bypassing for an internal voltage.
VREG2	Voltage Regulator 2. Connects to an external capacitor to provide bypassing for an internal power supply.

Package Outline Diagram

LU97 16-Pin Small-Outline Package

Dimensions are in millimeters.



5-8994 (F)

Ordering Information

Table 9. LU97 Ordering Information

Device	Package	Comcode
CSP1037	16-pin, small-outline	108500117
CSP1037A	16-pin, small-outline	108500091
CSP1037B	16-pin, small-outline	108500109

Notes

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